THE BASE STATION TELEMETRY DATA PROCESSING SYSTEM FOR UNMANNED HELICOPTERS

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ABSTRACT

This paper discusses the design and implementation of the base station telemetry data processing system for the unmanned helicopter. The system designed is composed of code synchronizer, decoding and frame synchronizer as well as PCI bus interface. The functions of the system are implemented with very large integrated circuits and a standard PCI inserted card that is compact and easy to install. The result of flight performance tests shows that the system is reliable and can satisfy the requirements of telemetry system for unmanned helicopters.

KEYWORDS

Telemetry, Data Processing, Unmanned Helicopter, Telemetry Base Station

INRODUCTION

Nowadays unmanned air vehicles (UAV) are widely used in both military and commercial fields. The principal advantage of UAV is absence of risk for human lives and health. As one of them, the unmanned helicopter has more advantages: It can take off and land flexibly with no need for runway and it is also highly maneuverable, whereas it is more difficult to control because of more complex structure.

An UAV system typically comprises an airborne part with an appropriate payload and a base station. The telemetry and telecommand electronic system is one important part of it. The telemetry data is the only information source for base station to control the unmanned helicopter，and due to the special application conditions and the high maneuverability of the helicopter, it is very important to maintain a reliable telemetry data communication link between the helicopter and the base station. And as a part of it, the base station telemetry data processing system must be small and light while having reliable functions to meet the requirements of a mobile telemetry and remote command base station.

The system discussed in this paper comprises code synchronizer, frame synchronizer; frame cache memory and PCI bus interface. Amongst all of them are realized in Verilog HDL language with a Field Programmable Gate Array (FPGA), which can be reconfigurable to adapt to a changing

environment.

In this paper the structure of the base station telemetry data processing system for the unmanned helicopter is introduced and the design and implementation is discussed. The design of telemetry data code synchronizer block is described and a newer and faster algorithm for code synchronization is presented in the next section. Then the method of detecting telemetry data frame synchronization word is given and its validity is proved. The design of telemetry data frame synchronizer block and the cipher code translator is described. As practice has proved, with proper structure, light weight and good performance, the base station telemetry data processing system can completely meet the requirements of telemetry system for unmanned helicopters.

BASIC TELEMETRY SYSTEM OVERVIEW

The telemetry system for the unmanned helicopter is made up of airborne and ground section. A block diagram of the overall telemetry system can be seen in Figure 1.

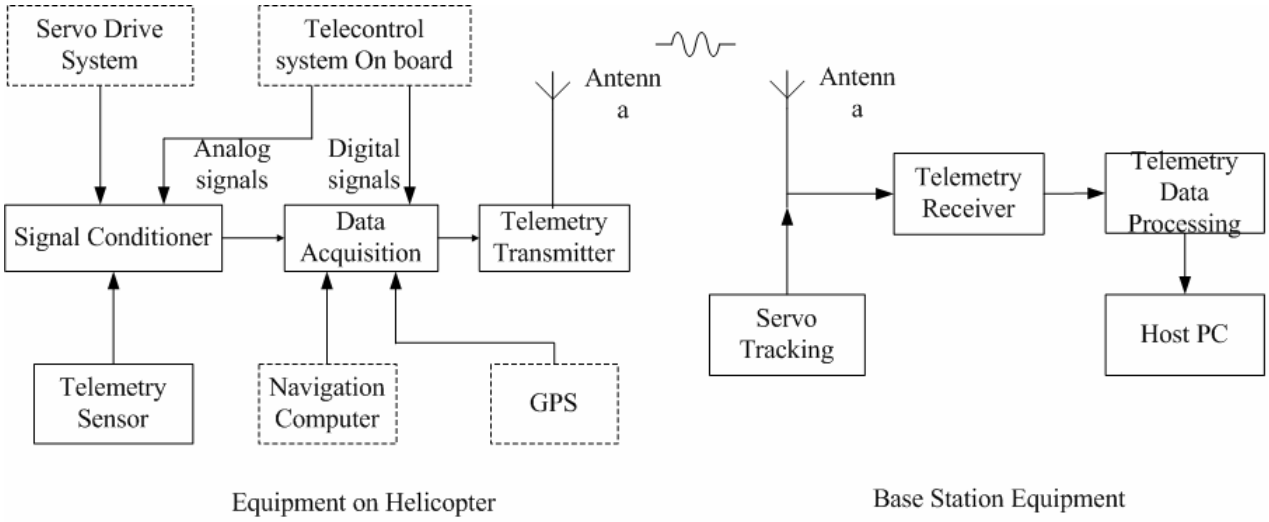

Figure1. Block diagram of telemetry system

In the airborne section the analog signals from telemetry sensors, servo drive system and telecommand system on board are assorted, transformed and amplified to low impedance voltage signals by signal conditioner to be gathered by data collector. The digital signals from Global Positioning System (GPS), navigation computer and telecommand system on board are sent directly to data collector, where all the signals are collected, encrypted, encoded and transformed into telemetry data frames. Then they radiate through the telemetry transmitter and the antenna.

The ground section is composed of antenna, servo tracking system, telemetry receiver and telemetry data processing system. The Base station telemetry system adopts wide beam antenna and its bi-axis servo tracking is digitally directed. Data processing section of the ground telemetry system comprises code synchronizer, frame synchronizer and decoder as well as PCI bus interface. These functions are implemented with very large integrated circuits and standard PCI inserted card that is compact and easy to install.

DATA PROCESSING SYSTEM

The base station telemetry data processing system is composed of code synchronizer, frame synchronizer， frame cache and PCI bus interface as showed in Figure 2. The functions of decryption, channel decoder and data check are realized with a software method in the host PC.

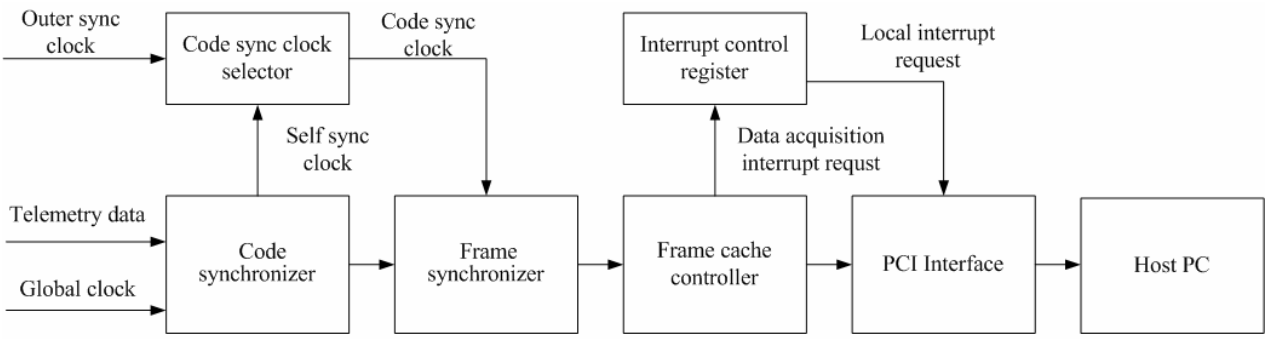

Figure 2 Block diagram of telemetry data processing system

CODE SYNCHRONIZER

The telemetry data received is a Pulse Code Modulation (PCM) bit stream, and the function of code synchronizer is to regenerate a clock timing signal for code regeneration and detection, even for frame synchronization. Most self-synchronization code synchronizers use digital Phase Lock Loop (PLL) to acquire the code synchronization clock. The digital PLL has many constructions, and one basic block diagram of digital PLL is shown in figure 3.

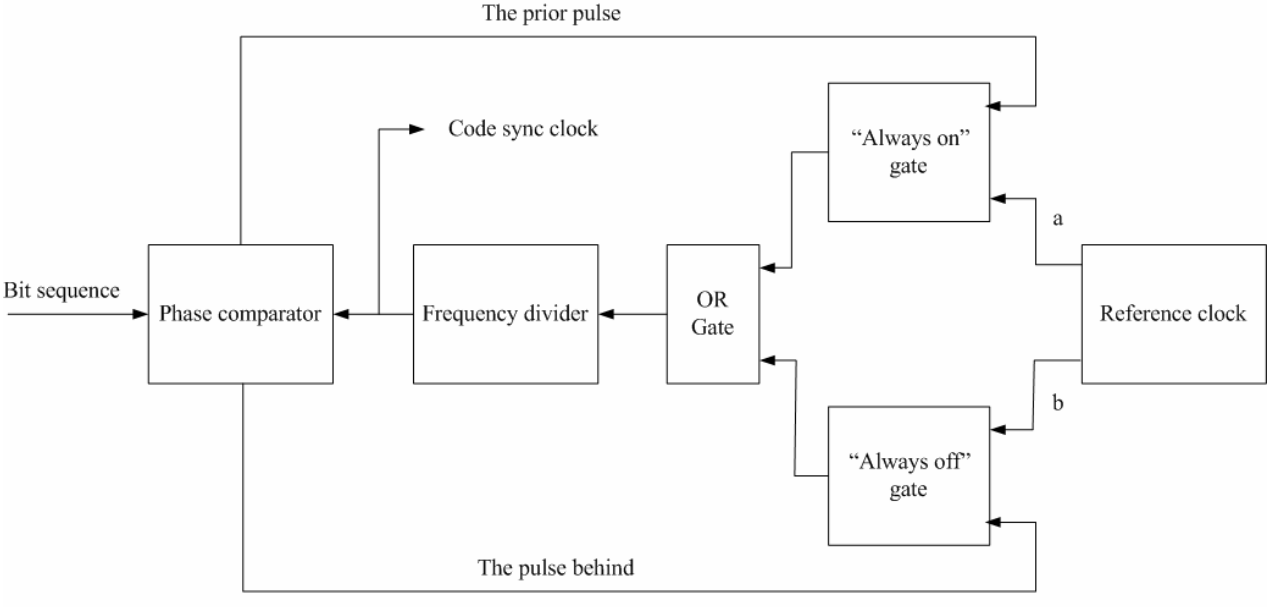

Figure 3 Block diagram of digital PLL

The reference clock generates two pulse sequences which have a period of T and have phase difference of T/2, ‘a’ and ‘b’ shown in figure 3. The sequence ‘a’ is added to frequency divider through “Always on gate” and OR gate, and the output of the frequency divider is what we need—— the code synchronization clock. On the same time, the code synchronization clock is compared with the received bit sequence in the phase comparator. If the code synchronization clock has a prior phase, the phase comparator output a “prior pulse” to close the “always on gate”, and deduct a pulse of sequence ‘a’, so the code synchronization clock is delayed by T. When the code synchronization clock has a later phase, the phase comparator output a “pulse behind” to open the “always off gate”, and add a pulse of ‘b’ to the input of frequency divider, so the code synchronization clock can advance by T. So after several adjustments, the code synchronization clock and the received sequence can be synchronized.

In order to reduce the synchronization time, we consider about the improved structure of digital PLL. The new structure of digital PLL is shown in figure4.

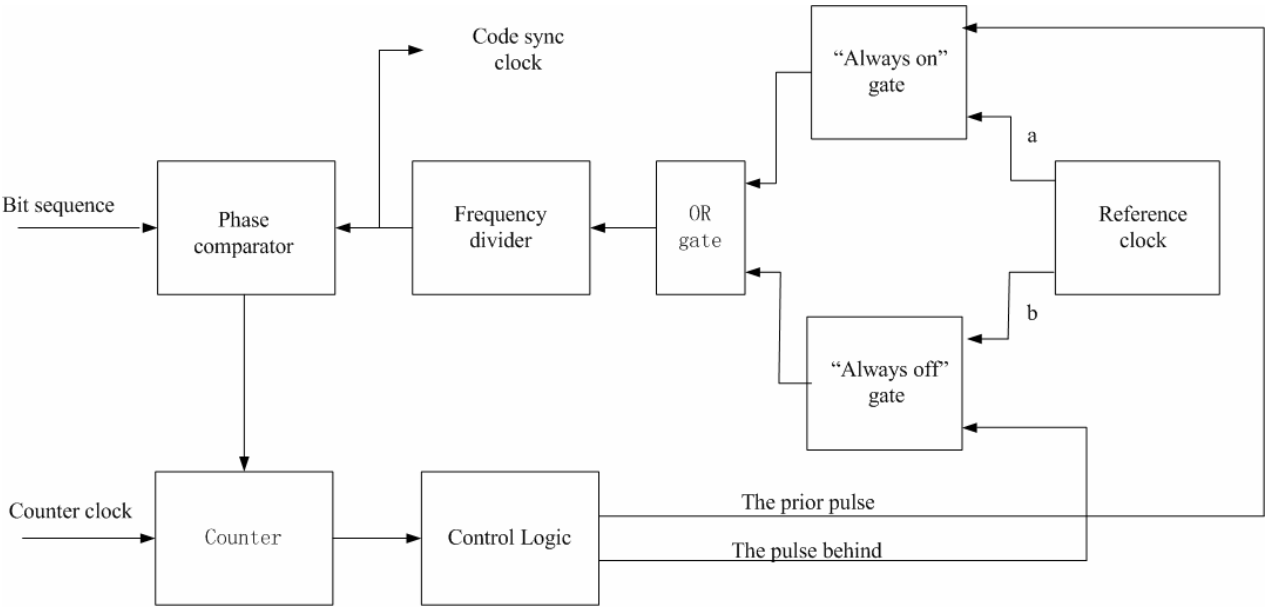

Figure 4 the Improved Structure of Digital PLL

In figure 4, the phase difference signal of phase comparator enables the counter, which counts the period of the phase difference signal. So the output of counter figures out the value of phase difference. Then the control logic outputs different control pulses according to the value of phase difference. As the result of it, the synchronization time is reduced greatly.

FRAME SYNCHRONIZER

In order to meet the rapid acquisition requisition of telemetry system, we select synchronization codeword to realize the frame synchronization. The synchronization codeword is sent as part of a message header and a matched filter correlator is used to search it in the data stream. The block

diagram of frame synchronization codeword detector is shown in figure 5.

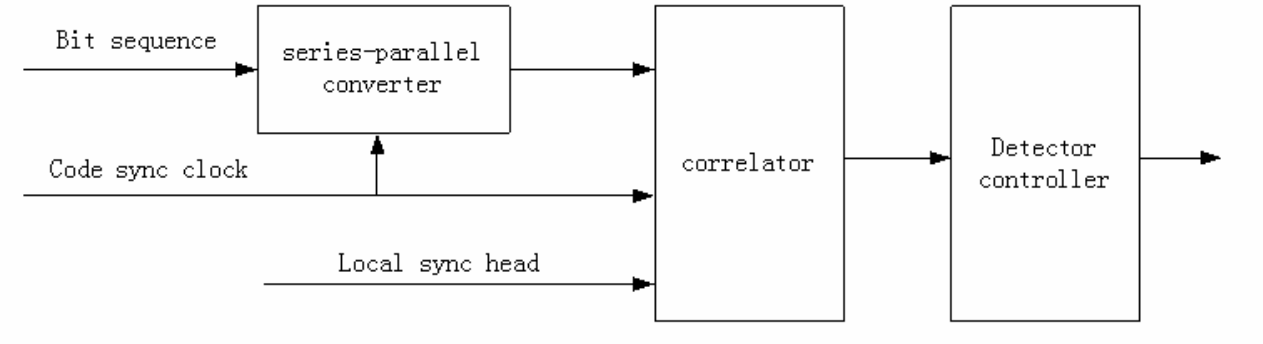

Figure 5 the Frame Synchronization Codeword Detector

The function of frame synchronizer is realized in Verilog HDL language, as the state convert diagram shows in figure 6.

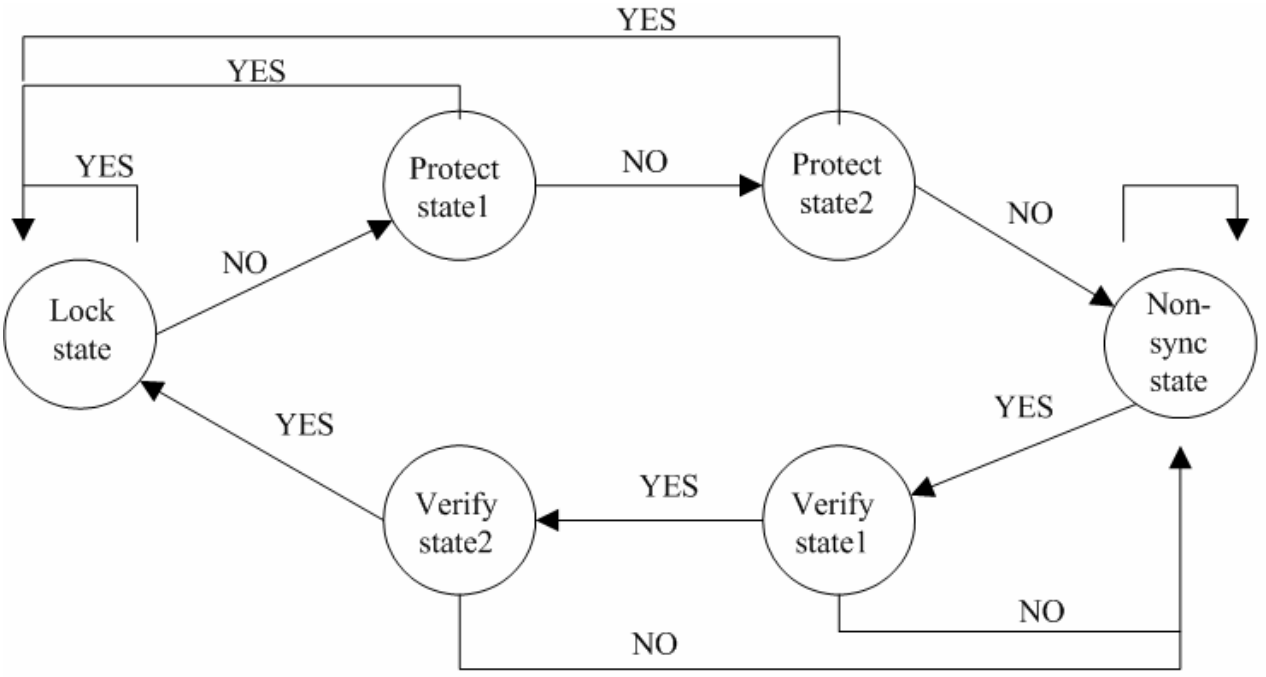

Figure 6 the State Convert Diagram

In addition, the telemetry system introduces the "once a key" sequence encryption algorithm which is quite simple and can proliferate a few errors. What is more, Channel encoding employs reduced cyclic code that can correct one error (8, 4) with simple algorithm for the reliability of telemetry data. So the telemetry data processing system has the corresponding decryption and channel decoder parts, which are realized with a software method in the host PC.

CONCLUSION

The telemetry data processing system designed is composed of code synchronizer, frame synchronizer, decoder as well as PCI bus interface. Amongst all of them, the code synchronizer is the basic component for code regeneration and detection, even for frame synchronization. With a new algorithm it can not only produce precise code synchronization signal but also synchronize fast. The functions of the system are implemented with very large integrated circuits and a standard PCI inserted card that is compact and easy to install. The result of flight performance tests shows that the system is reliable and the algorithm for code synchronization is faster than the algorithm used in the system before.

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