FFT Bit Templating – A Technique for Making Amplitude and Frequency Measurements of a BPSK Modulated Signal

Bruce Shockey
CMC Electronics Cincinnati
Mason, OH 45040

ABSTRACT

In many spacecraft receiver applications, the Fast Fourier Transform (FFT) provides a powerful tool for measuring the amplitude and frequency of an unmodulated RF signal. By increasing the FFT acquisition time, tiny signals can be coaxed from the noise and their frequency measured by determining which frequency bin the signal energy appears. The greater the acquisition time, the narrower the bin bandwidth and the more accurate the frequency measurement.

In modern satellite operations it is often desirable for the receiver to measure the frequency of a carrier which is modulated with BPSK data. The presence of the BPSK data limits the FFT acquisition time since the signal may switch polarities a number of times while the FFT samples are being acquired. This polarity switching spreads the signal energy into multiple frequency bins making frequency measurement difficult or impossible. The Bit Templating Technique, used for the first time in the CMC Electronics Cincinnati TDRSS / BPSK Spacecraft Receiver, collects the modulated waveform energy back into a signal bin so that accurate amplitude and frequency information can be calculated.

KEYWORDS

Bit Templating, Satellite Communications, Digital Signal Processing and Fast Fourier Transforms.

INTRODUCTION

In a coherent BPSK spacecraft receiver, the incoming signal must be heterodyned and/or derotated from the RF carrier frequency down to 0 Hz. To achieve coherency, the receiver will typically phase lock to the carrier in order to achieve optimal demodulator performance. Prior to phase locking, the receiver must measure the frequency of the noisy incoming signal and change the frequency of the VCOs or NCOs to bring the frequency of the signal to within the capture frequency range of the PLL. This is difficult for three reasons. First, due to the long distances involved in spacecraft communications, the Signal to Noise Ratio (SNR) may be low. In order to achieve phase locking the loop bandwidth of the PLL must be kept narrow to achieve the critical SNR needed to lock the loop. Second, the receiver center frequency is subject to variations due to widely varying temperature and prolonged service life, often in years. Finally, the receiver will experience a constantly changing frequency shift, both positive and negative, due to the Doppler effect created by the motion of the spacecraft in it's orbit relative to the fixed ground transmitter.

In many spacecraft applications, the frequency of the incoming signal (following heterodyning operations) is measured using the Fast Fourier Transform (FFT). The FFT converts an array of time domain samples into frequency domain information. The accuracy of the frequency domain information is directly proportional to the acquisition time. For example, if a 128 point FFT processes 128 time domain samples that were acquired over a 0.032 second time window, each FFT bin represents 31.25 Hz providing excellent frequency resolution. If a narrower bin bandwidth (bin-width) is needed, the acquisition time may be extended. For example, a 0.064 second acquisition time will produce a 15.625 Hz bin width.

Figures 1 – 3 show a few typical waveforms to help visualize the FFT process. Figure 1 shows 128 sinusoidal samples. Typically, these samples will be complex having both a real and an imaginary part. Only the real part of the signal is shown in this paper for ease of visualization but in practice, a complex signal is needed to distinguish between positive and negative frequencies. Figure 2 shows the same sinusoidal samples scaled by a gain control operation and corrupted by noise. The SNR shown in this graph is representative of the SNR that would be experienced at the input of the FFT. Figure 3 shows the FFT output after processing the signal shown in Figure 2. The DC bin is at the far left of the graph. The positive frequency bins start immediately to the right of the DC bin and are in ascending order. The negative frequency bins start at the far right side of the graph and are in ascending order from right to left.

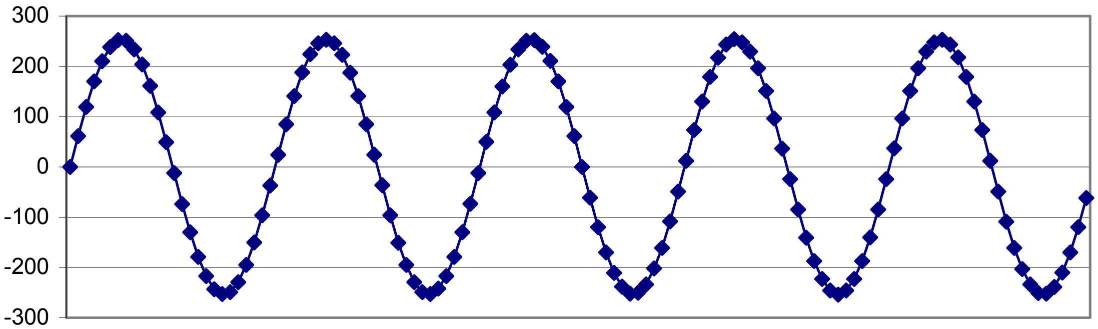

Figure 1. 128 Sinusoidal Signal Samples

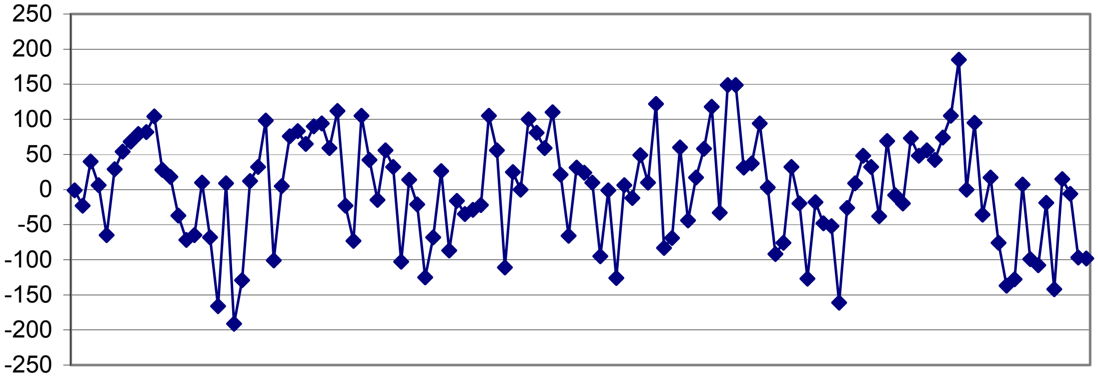

Figure 2. Sine Wave Incoming Signal With Noise

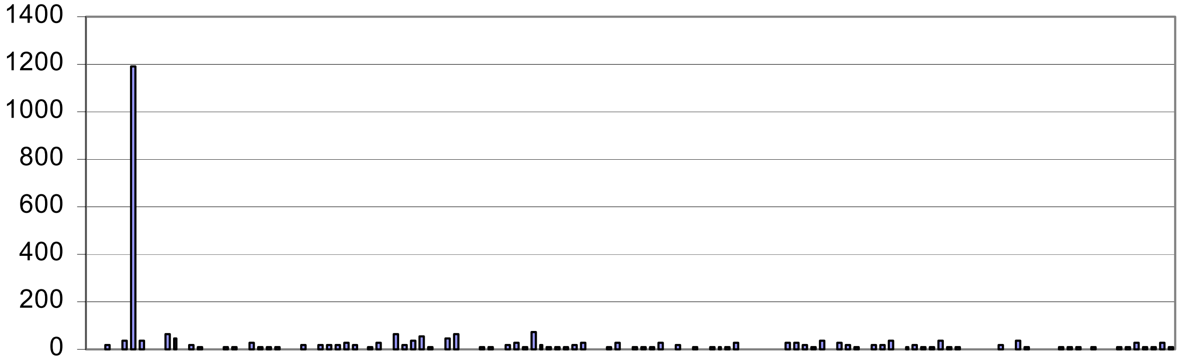

Figure 3. Post FFT Processing of the Figure 2 Waveform

The algorithm to determine the carrier frequency is very straightforward:

1. Determine the bin, which has the greatest magnitude.
2. Multiply the bin number (either positive or negative) by 1 / Tacq.

In this case the biggest magnitude is in positive bin 5. The sample time is Tsamp * 128 samples = 0.032 sec. Bin width = 1 / 0.032 = 31.25 Hz. Carrier Freq = 5 * 31.25 Hz = 156.25 Hz.

Problems of Determining the Carrier Frequency with BPSK Data Applied

The ability to resolve an incoming frequency into such fine increments provides a powerful design tool provided that the incoming signal is sinusoidal in nature – in other words, without BPSK data applied. When BPSK data is applied, the signal energy which once occupied a single frequency bin is now dispersed into several frequency bins making it much more difficult to determine the carrier frequency. The simple algorithm shown above for the sinusoidal case no longer applies. Figure 4 shows a noise free sinusoidal carrier modulated with 4 bits of 0,1,0,1 BPSK data. Figure 5 shows the FFT analysis of this waveform. Note that the signal energy is spread over several bins. The question is -- which spectral stick bin represents the correct carrier frequency. The answer is --

NONE! The carrier energy would all fall into frequency bin 5 (156.25 Hz) if the modulation were suddenly removed.

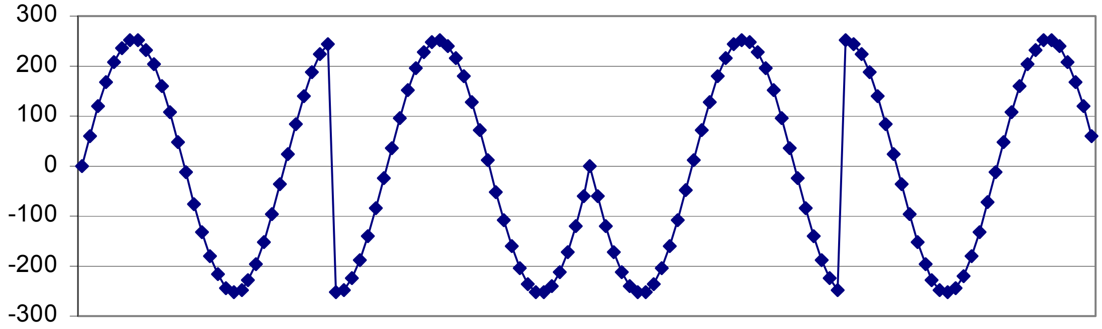

Figure 4. Time Domain Samples of Incoming Signal With 4 Bits of Alternating 1,0 BPSK Data

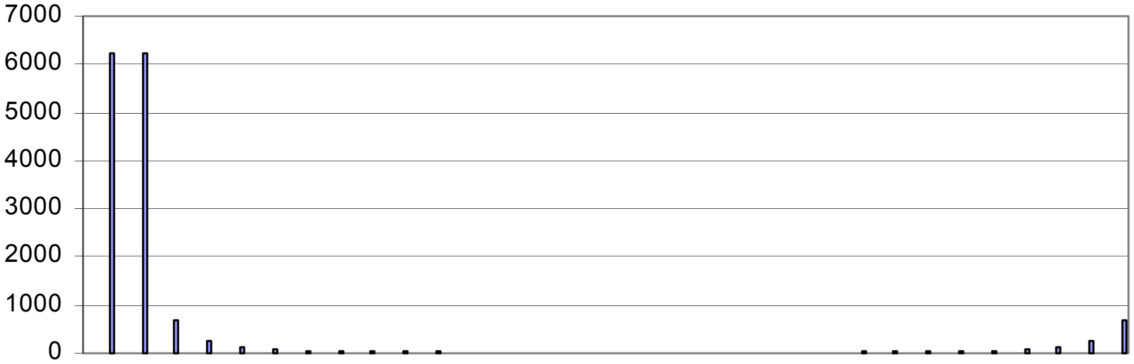

Figure 5. Frequency Domain Representation of Figure 4 Signal Using a 128 Point FFT

BIT Templating Technique

The bit templating technique attempts to solve the multiple frequency bin problem by flipping the polarity of the incoming time domain samples until they look like a sinewave again. Figure 6 shows our now familiar incoming BPSK modulated carrier. First, the incoming signal will be point-by-point multiplied by the bit template shown in Figure 7.   The product of this operation is shown in Figure 8. Finally, the FFT of the Figure 8 waveform is computed. The result of this computation is shown in Figure 9. Once again, the signal energy is re-collected into bin 5 and the simple bin number to frequency conversion can be easily made.

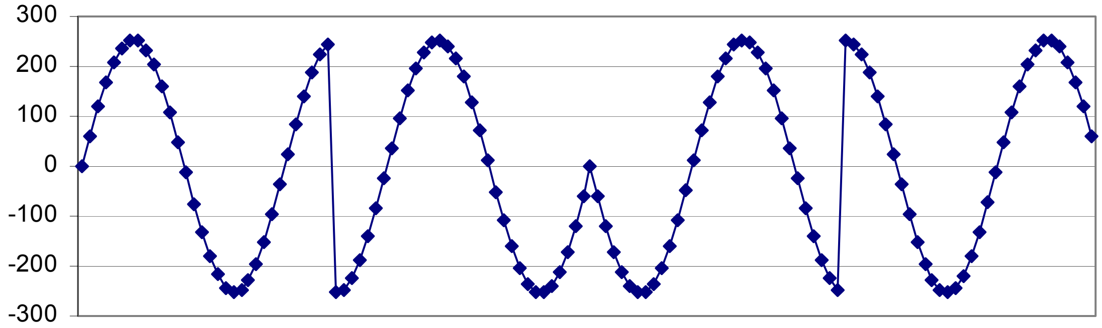

Figure 6. Time Domain Samples of Incoming Signal With 4 bits of 0,1,0,1 BPSK Data

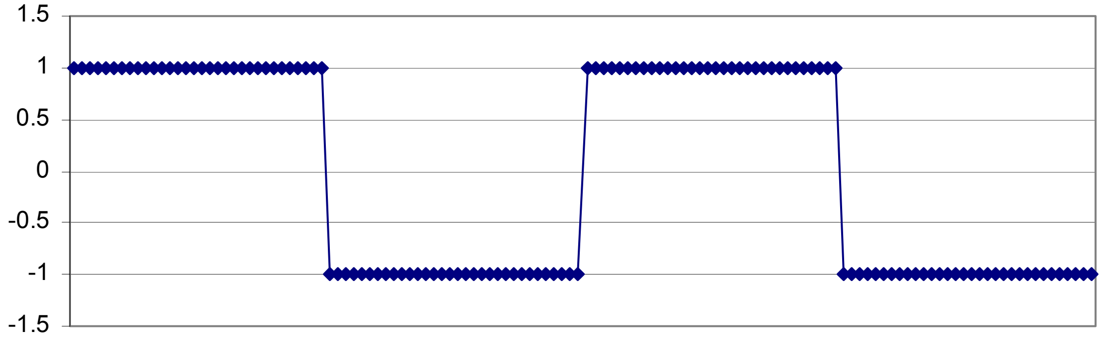

Figure 7. Bit Pattern 0,1,0,1 Bit Template

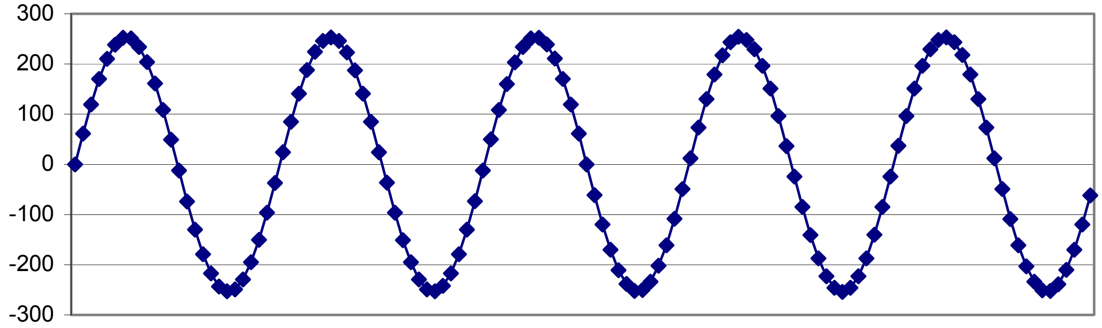

Figure 8. Product of the Time Domain Samples and the Bit

Figure 9. FFT of the Point-by-Point Time Sample * Bit Template Product

To extend the bit templating concept to a working design, several additions are needed. First we need supply a bit template for all of the possible bit patterns. Since there are 4 bits being represented, we have 16 possible bit combinations.

Some labor saving can be realized by remembering that the FFT is equally happy with a continuous sine wave that is "right side up" or "up side down". For example, with the familiar 0,1,0,1 BPSK incoming signal either a 1,0,1,0 bit template or a 0,1,0,1 bit template will work equally well. Both will yield a continuous time domain sinewave and an FFT with all the energy collected in a single bin. The table of bit template patterns required to "straighten out" the 16 incoming data patterns are shown in Figure 10.

0000	1111
0001	1110
0010	1101
0011	1100
0100	1011
0101	1010
0110	1001
0111	1000

Figure 10. Table of the 8 Template Data Patterns and Their Inverses

Also needed to make the bit templating concept a working design, is the ability to move the bit template over the incoming signal samples until the bit transitions of the template match the bit transitions of the incoming signal. This is accomplished by starting the bit template correlation at various offsets of the array of data samples. The algorithm is to take the bit template product, evaluate the FFT, and note the biggest bin magnitude. Then move to the next bit offset and repeat. The bit offset producing the biggest FFT bin magnitude is the "winner". It is recommended that the bit offset steps be 1/8 bit or smaller and span over the width of a bit. Larger bit offset increments have the possibility of dispersing the signal energy into multiple bins for certain bit offset relationships.

Calculation Engine

For the sample system that we have been discussing, there is a lot of computation that has to occur during the time that we will be acquiring samples (assuming a ping pong type acquisition/analysis system). There are 8 bit template patterns and 8 bit offsets to evaluate during the time that the next 128 samples will be acquired – 64 template products and 128-point FFT to compute in real time. In earlier days, attempting to crunch this much data in so short a time would have been impractical with microprocessor-based systems. Today, we have large FPGAs in which dedicated FFTs can be implemented in an endless variety of architectures, which can be adapted to fit any need. Furthermore, these FFTs can be implemented to execute their algorithms in parallel. This is not a technology of the future – this can be implemented with today's FPGAs.

Performance

The bit templating technique has been implemented for the first time in the TDRSS / BPSK spacecraft command receiver built by CMC Electronics Cincinnati in Mason Ohio. Both the TDRSS and BPSK operating modes make full use of the bit templating technique.

The bit templating technique used in the TDRSS / BPSK receiver is very similar to the technique discussed in the preceding paragraphs. The FFT is a 128 point FFT using a single 16-bit multiplier controlled by a dedicated state machine. The state machine analyses the results of the FFTs and calculates the resulting frequency offset. The digital design is implemented in a single Actel FPGA. This part, which is relatively small, was chosen for radiation hardness characteristics.

To demonstrate the capability of the bit template technique two graphs are shown in Figures 11 and 12. Figure 11 shows the probability of successfully determining the correct frequency bin as a function of signal to noise level with a sinusoidal, unmodulated carrier. Each data point represents 1000 simulated trials. This is the "best possible case". Figure 12 shows an identical configuration except that a 0,1,0,1 BPSK data pattern is modulated onto the carrier. A comparison of the two graphs shows that the difference in performance at low signal to noise ratios is less than 0.1 dB. This provides the receiver with the capability of acquiring either with or with out command data with nearly identical performance results.

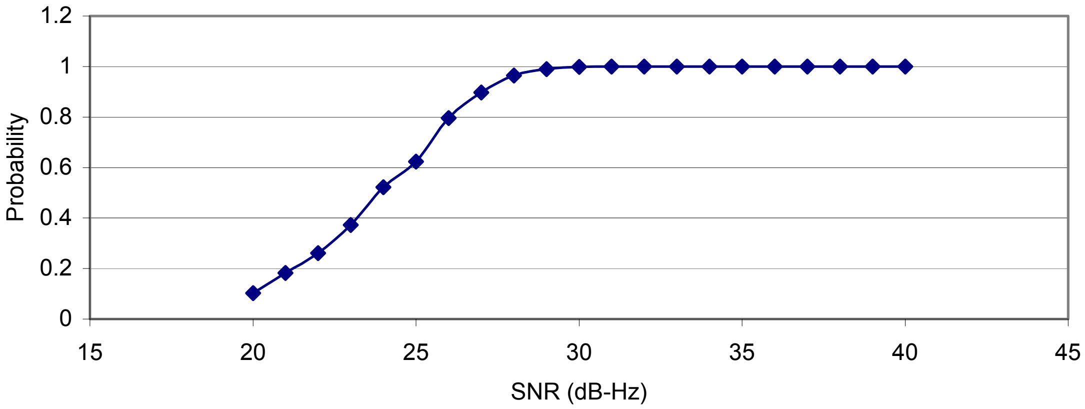

Figure 11. Bin Identification Performance Without Command Data

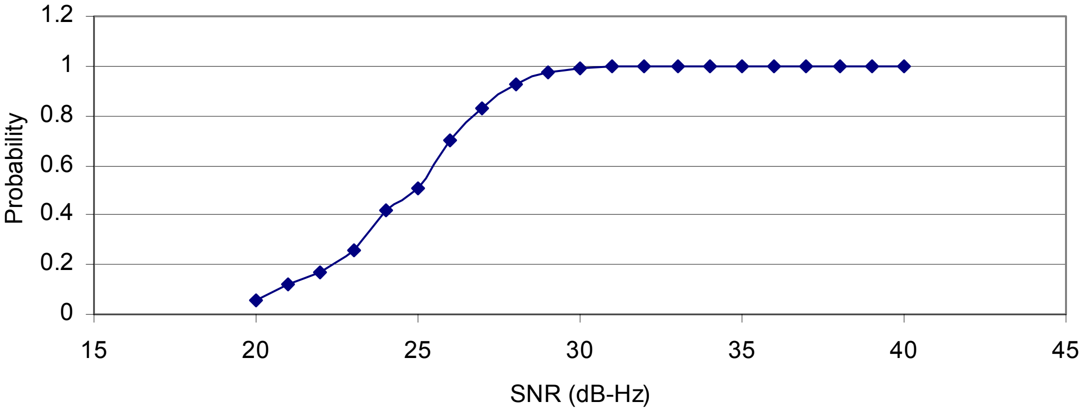

Figure 12. Bin Identification Performance With Command Data

POSSIBILITIES OF THE FUTURE

While the bit templating technique has been successfully implemented in the CMC Electronics Cincinnati TDRSS / BPSK spacecraft receiver, there are tempting design ideas for the future. As the bit template engine runs through the list of templates, one of the "waste by-products" are four bits of highly reliable command data taken in a very narrow bandwidth. Some possible implications are listed below.

1. No need to phase lock to the carrier – the command data is a by-product of the bit template operation.
2. No need to bit sync – bit sync is a by-product of the bit template operation.
3. Accurate receiver center frequency telemetry.
4. Reliable information needed to rapidly determine loss of signal

ACKNOWLEDGEMENTS

The author would like to gratefully acknowledge the assistance of Greg Casavant who implemented the digital design and whose ideas helped make the technique a working reality. The author would also like to acknowledge Carol Oelker and Mark Dapore for their help in producing and reviewing this paper.

REFERENCES

[1] Sklar, Bernard Digital Communications: Fundamentals and Applications, Prentice-Hall, Inc., Englewood Cliffs, NJ, 1988.