

A NEW FM SYSTEM WITH A NOVEL MODULATOR DESIGN YIELDING HIGH LINEARITY AND THERMAL STABILITY

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Summary Using two integrators operating in parallel, a high linearity FM modulator was designed. When one integrator is integrating, the other is being reset; thus, each integrator is only working at half the input signal frequency. In addition, feed forward voltage is applied to compensate for constant delay in the integrator and greatly increases the linearity at high frequency. A complete MODEM system of 1 megahertz bandwidth with a system linearity of $\pm 0.5\%$ and a thermal stability of $\pm 0.08\%/^{\circ}\text{C}$ was achieved.

Introduction The most difficult part of the design in a DC to high frequency FM system is the conversion of input signal to digital form. Many systems that use a blocking oscillator suffer thermal instability when operated at elevated temperature; those that use an amplifier integrator achieve limited range because of non-linearity at high frequency. This article describes a design concept which avoids the above limitations and has achieved an overall systems linearity of $\pm 0.5\%$ and overall temperature stability of $\pm 0.08\%/^{\circ}\text{C}$, with a bandwidth of 1 megahertz.

There is no description of the demodulator section because it is a conventional zero cross-over detector which is simple in operation. The MODEM system operates with the Mincom Series 110 Tape Recorder at a speed of 120 ips for a 1 MHz bandwidth.

Theory of Operation of a Conventional Integrator To see how we have resolved many of the the problems associated with a conventional integrator, we should begin by analyzing a simple integrator. Referring to Figure 1, and assuming an ideal amplifier of gain $A (= \infty)$ and infinite input impedance, then we can say $i_1 = i_2$, and its output is given by equation 1,

$$e_o(t) = \frac{-e_i(t) t}{R_i C} \quad (1)$$

(where t is time in seconds)

From equation 1, we have an ideal integrator which will provide an output voltage linearly proportional to the magnitude of input voltage and time.

If we connect a Schmitt Trigger to sense the output of the integrator and use the output of the trigger to initiate a constant discharge circuit (Q_D), then whenever the amplifier output reaches a preset level, the capacitor is discharged by constant coulomb Q_D . Thus, we have converted the input voltage $e_i(t)$ into an output waveform whose frequency is proportional to the magnitude of the input. Figure 2 shows the circuit and Figure 3 shows its ideal timing diagram.

In practice, the timing diagram is as shown in Figure 4. Normally, we would like the discharge time t_2 to be very short compared to t_1 , so that high frequency operation can be obtained with good linearity. The discharge time t_2 is limited by the time constant of the discharging circuit and the settling time of the amplifier. These circuit parameters represent the first limitation for high frequency operation of a conventional integrator.

There is a second serious limitation of a conventional integrator. This is due to the constant time delay of the system. t_3 in figure 4 represents the delay between the time the output of the integrator reaches e_R and the time the Schmitt Trigger output e_T rises to its operating level. t_4 is the delay between the time when the Schmitt Trigger output reaches its operating level and the time the I_D starts to discharge the capacitor. t_3 and t_4 constitute a source of linearity error because they are constant with frequency. At high frequency (i.e., short period), this fixed delay is a larger portion of the whole period.

Theory of Operation of Mincom Modulator The heart of the modulator consists of two IC integrators connected as shown in Figure 5.

Input signal e_i is fed into integrators IC1 and IC2 through R1 and R3. The outputs of the two integrators are coupled to comparators IC3 and IC4 through resistors R6 and R12. Resistors R7 and R13 are connected to a reference voltage where the triggering point of the comparators can be precisely set. IC5 and IC6 form an RS flip-flop which is set and reset by IC3 and IC4, alternately. The output of IC5 is used to drive switch driver 1 which in turn, drives transistor switch SW1; when SW1 is on, capacitor C1 is shorted out and IC2 stops integrating. Similarly, SW2 is driven by IC6 and shorts out C2 and stops IC2 from integrating.

IC3 and IC4 also drive IC7. The output of IC7 is already a usable waveform except that it is not a square wave. By going through flip-flop 2, its output, f_{out} , provides a symmetrical square wave and can be used to drive whatever circuit follows.

Assume that integrator 1 has been integrating and its output is shown as e_i in Figure 6. At a particular time t_3 , which depends on the amplitude of the input voltage e_i and the comparator reference voltage, comparator IC3 operates and its output e_2 resets FF I to the opposite state as shown by e_3 and e_6 . The fall of e_3 drives switch driver 1 which turns on SW1. This action initiates the discharge of C1. The discharge portion of e_i , which is the

time required to discharge C1, can be considered the settling time of integrator 1. This is shown as Δt_3 . Obviously, this discharge period must completely elapse before another integration is initiated. This portion of the discharge time is what limits the speed of most conventional integrators. As will be described below, our modulator avoids this limitation by using another integrator 2 while integrator 1 is being discharged.

While integrator 1 is being turned off by e_3 , integrator 2 is being turned on by e_6 . This process of alternating back and forth continues but at all times the turn around portion (Δt_6) of the output signal from the integrator is not used. Thus, by using another integrator, the error due to amplifier settling time is avoided. The time relationship of various points is shown in Figure 6.

From Figure 6, one can see certain delays in the system. The first delay is Δt_1 . Let us call this the turn-on delay for integrator 2. This is the time after integrator 1 reaches reference voltage V_{R11} until integrator 2 starts integrating. Δt_1 consists of delays in IC3, IC5, IC6, switch driver 2 and SW2. Similarly, delay Δt_2 is the time after integrator 2 reaches reference voltage V_{R21} until integrator 1 starts integrating again. Another delay is Δt_4 . This is the time difference between when integrator 2 reaches reference voltage V_{R21} and when integrator 2 starts being discharged by SW2. Delays Δt_1 and Δt_4 constitute the integration error of integrator 2.

Delays Δt_1 and Δt_4 are fixed because they are caused by charge storage of IC's and transistors. Because these delays are fixed, they cause a non-linearity in the output frequency for high input signal. By utilizing the property of the constant delays Δt_1 and Δt_4 and using a feed-forward voltage, the other limitation of a conventional integrator due to fiQ delays, error of integration is avoided. The voltages that are used to nullify the effect of these fixed delays are shown in Figure 5. RS, R8, R9 provides e_{i1} to compensate for integration error of integrator 1. Likewise, R5, R10 and R11 provides e_{i2} to compensate for integration error of integrator 2. The overall effect of these compensating voltages may be seen in greater detail by referring to Figure 7 and the following explanation. Since both integrators are symmetrical, only compensations for integration error ($\Delta t_1 + \Delta t_4$) of integrator 2 are shown:

- e_R = The reference voltage to which integrator 2 would integrate if there were no delays $\Delta t_1 + \Delta t_4$.
- e_{R1} = Actual reference voltage at which integrator 2 triggers.
- e_{R21} = Equivalent reference voltage error due to delay Δt_1 when integrator 2 begins to discharge.

e_{R22} = Equivalent reference voltage error due to delay Δt_1 .

$$e_{R2} = e_{R21} + e_{R22}$$

$$e_{R2} = e_R - e_{R1}$$

$$1/2 T_c = \Delta t_1 + \frac{e_{R1}c}{I} + \Delta t_4$$

$$\text{where } I = \frac{e_i}{R} \text{ and}$$

R is the value of R_1 or R_3 and c is the value of C1 or C2.
 e_i is the, value of the input voltage as shown in Figure 5.

$$\begin{aligned} \text{Let } T_p \text{ (total delay)} &= \Delta t_1 + \Delta t_4, \\ \text{then it follows that } 1/2 T_c &= T_p + \frac{e_{R1}}{e_i} RC \end{aligned} \quad (2)$$

From Equation 2, the $1/2 T_c$ period includes a fixed delay T_p . To eliminate this term, the values of resistor R5, R8, R9, R10 and R11 are calculated so that feed-forward loop provides the following relationship:

$$\begin{aligned} e &= \frac{e_i}{RC} T_p \\ \text{or} \\ T_p &= \frac{e}{e_i} RC \end{aligned}$$

Substituting for e_{R2} ,

$$T_p = \frac{e_R - e_{R1}}{e_i} RC \quad (3)$$

Combining Equation 3 with Equation 2, we obtain:

$$1/2 T_c = \frac{e_R - e_{R1}}{e_i} RC + \frac{e_{R1}}{e_i} RC = \frac{e_R}{e_i} RC$$

The modulator frequency is, therefore

$$f = \frac{1}{T_c} = \frac{e_i}{2e_R RC}$$

Thus, by using feed-forward voltage to control the trigger points in the comparators, the effects of the fixed delays on the output frequency have been eliminated.

Stability of frequency with temperature is achieved by using stable IC's.

Conclusion The limitation on the performance of a conventional FM/Modulator has been overcome by two approaches:

- a. The limitation due to the settling time of an amplifier is resolved by using two integrators. This enables one integrator to start integrating while another one is being discharged. This effectively makes each integrator work at half the input frequency.
- b. The non-linearity at high frequency is overcome by supplying a feedforward voltage that is superimposed on the reference voltage to the input of comparators. The feed-forward voltage adjusts the trigger point of the comparators so that the effects of fixed delays are nullified.

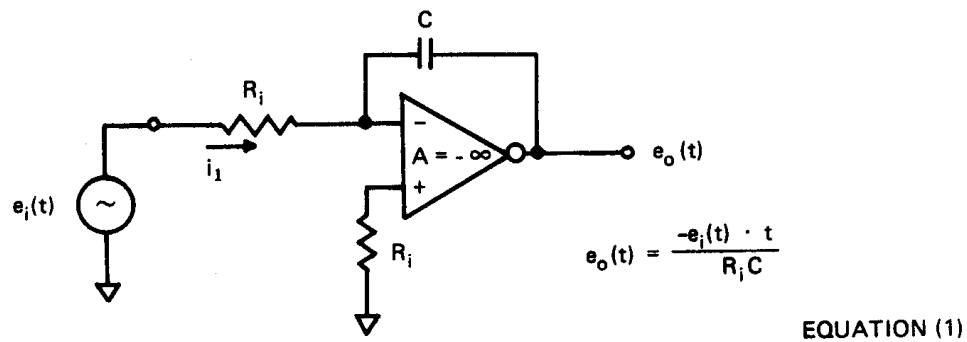


Figure 1. Circuit Diagram of an Ideal Integrator

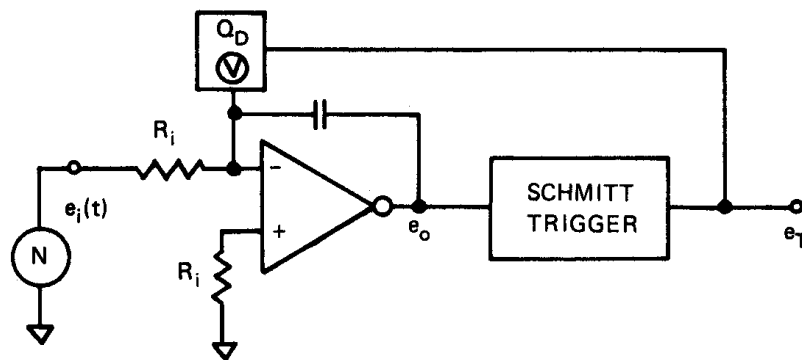


Figure 2. Circuit Diagram of a Conventional Integrator Used to Convert Input Voltage Frequency

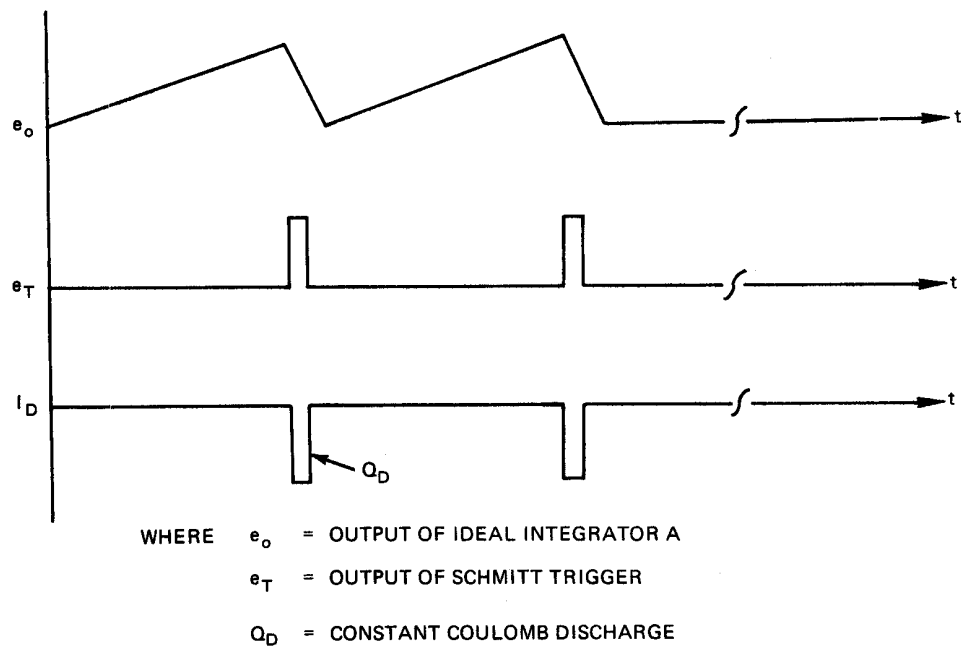
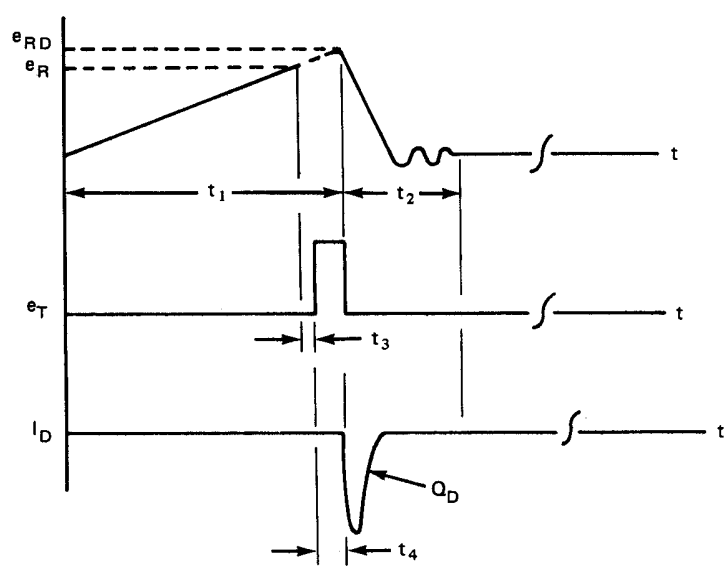


Figure 3. Timing Diagram of an Ideal Modulator



WHERE t_1 = INTEGRATING TIME
 t_2 = DISCHARGE AND SETTLING TIME
 e_R = VOLTAGE LEVEL AT WHICH COMPARATOR BEGINS TO OPERATE
 e_{RD} = ACTUAL POINT AT WHICH INTEGRATOR IS DISCHARGED BECAUSE OF $t_3 + t_4$

Figure 4. Practical Timing Diagram for Figure 3

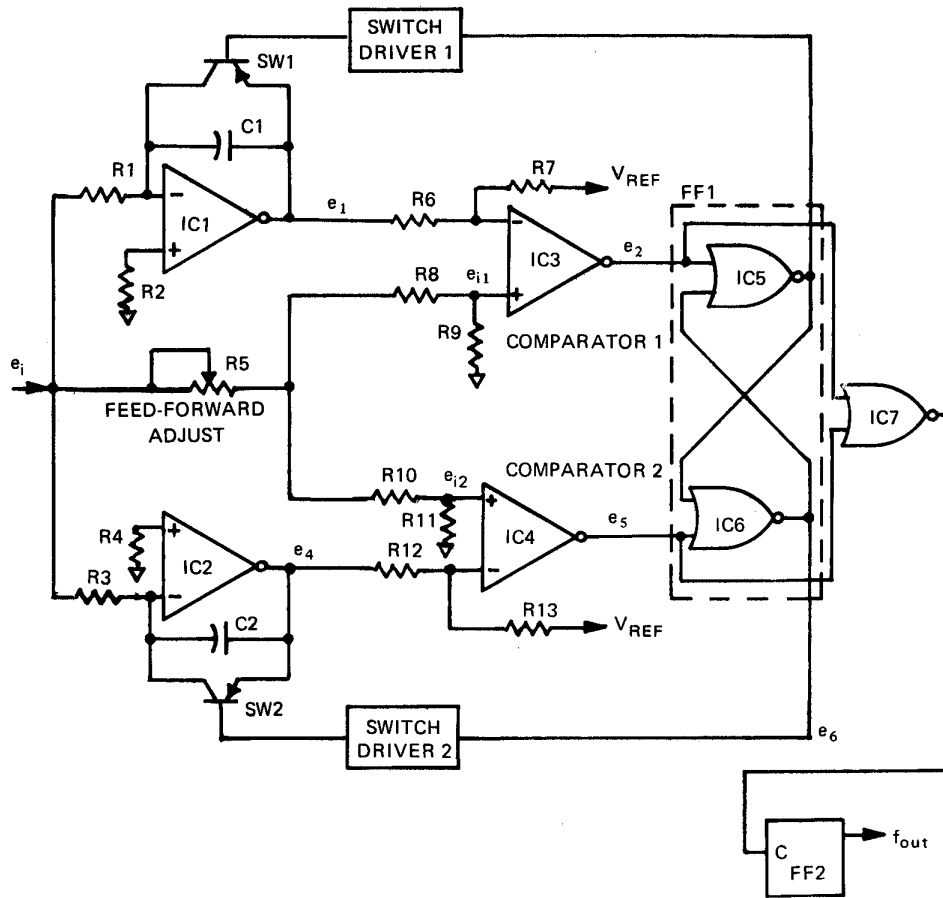


Figure 5. Block Diagram of 3M Mincorn Modulator

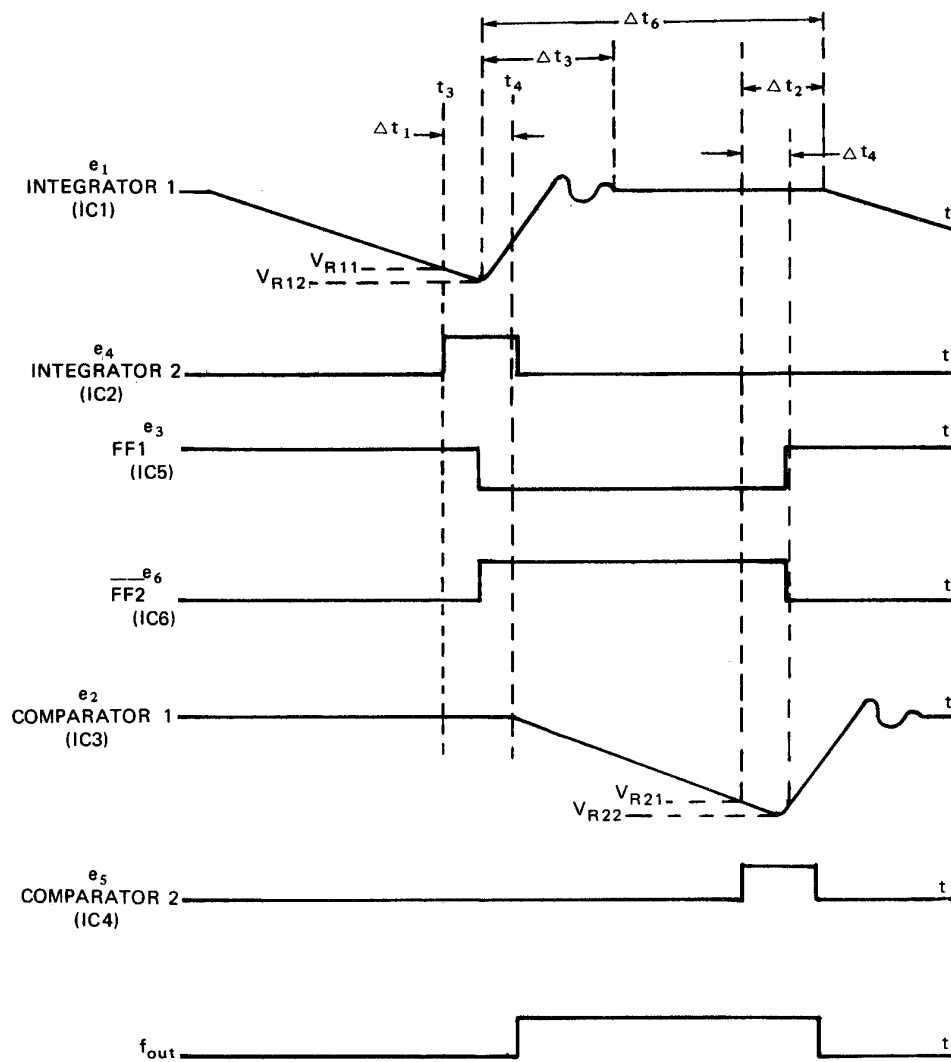


Figure 6. Timing Diagram of 3M Mincom Modulator

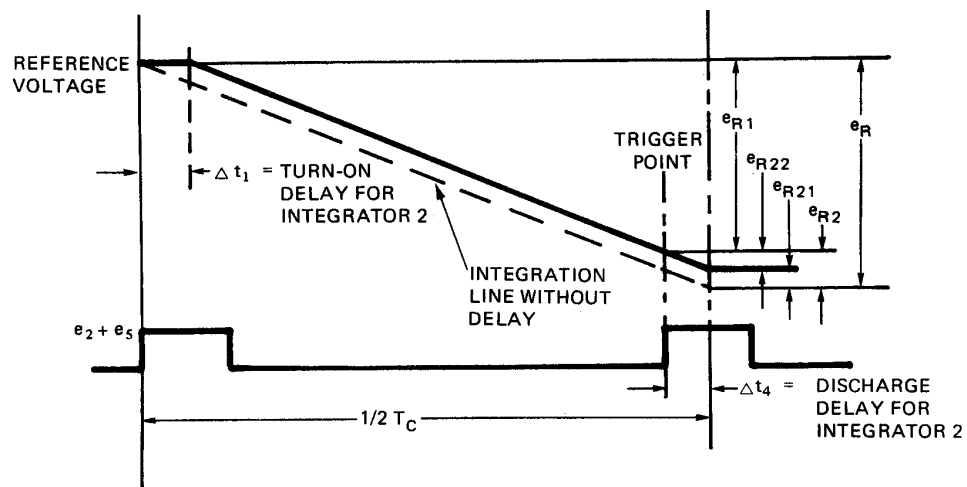


Figure 7. Effect of Feed-Forward Voltage on Compensating for Fixed Delays