A NEW TYPE OF PSK ANTI-AMBIGUITY SYSTEM FOR SATELLITE APPLICATIONS

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Summary In coherent PCM-PSK links the problem of solving the phase ambiguity in the reconstruction of the subcarrier has been traditionally solved by making use of the knowledge of some part of the transmitted message or by employing MARK-type codes.

After a brief discussion of these well-known methods a new approach is proposed which makes use of an auxiliary non-ambiguous PSK demodulator based on the estimation of the sign of the message transitions.

It is shown that no particular requirements on the noise performance of this auxiliary demodulator is needed to ensure acceptable overall performance of the antiambiguity system. A particularly simple hardware implementation is indicated and experimental results are presented for cases of practical interest.

1.1 General The absence of a component at the sub-carrier frequency in a binary PSK signal precludes the use of a conventional phaselock loop to re-establish a reference for demodulation purposes. Two methods are currently used for generating a reference sub-carrier from the received signal even when the residual sub-carrier component is not available. The first is called the “squaring loop”.

The received signal is band-pass filtered, squared to remove the modulation and the resultant double frequency component is tracked by a conventional PLL. Frequency dividing the output of the VCO by two, a coherent signal is available at the sub-carrier frequency.

A direct consequence of the frequency division by two, however, is that the phase of the reconstructed sub-carrier is 180° ambiguous with reference to the “true” sub-carrier phase.

An alternative method often makes use of the “quadrature-channel phaselock loop” (QCPLL) called also “Costas loop” (Fig. 1.1.1).

In the absence of noise, let the input signal be

$$e_1(t) = \sqrt{2}\, A\, \delta(t) \cos(\omega_o t + \theta_1) \tag{1}$$

where $\delta(t)$ conveys the binary information and is equal to +1 or -1 with equal probability in each bit interval.

The output of the VCO is

$$e_2(t) = \sqrt{2} \cos(\omega_o t + \theta_2) \tag{2}$$

The filtered signals in the in-phase and quadrature channels are, respectively

$$e_3(t) = A\, \delta(t) \cos \phi(t)$$
$$e_4(t) = A\, \delta(t) \sin \phi(t) \tag{3}$$

where $\phi = \theta_1 - \theta_2$ is the reference phase error.

The product of these two signals gives the VCO control voltage

$$e_5(t) = \frac{1}{2} A^2 \sin 2\phi(t) \tag{4}$$

since $\delta_2(t) = 1$, and is independent of the modulating signal $\delta(t)$, allowing proper operation of the tracking loop.

It appears from (4) that the error voltage is a sinus function of the double of the phase error, therefore resulting in a 180° phase ambiguity in the reconstructed sub-carrier.

With both systems, synchronous demodulation of the incoming PSK signal is accomplished by multiplication with the reconstructed sub-carrier. As a result of the phase ambiguity of the latter the output of the demodulator will be either the original PCM message or its complement.

2.1 Conventional anti-ambiguity systems Let us consider first the “mark” code. With it, the binary information representing the message in “level” form is coded in such a way that a change from “one” to “zero” or viceversa represents a “one” in the original message, while no change indicate a zero. In this way, the “mark” message could be complemented without affecting the correct decoding of the original message, and, in the case of PSK, the resulting ambiguity will be suppressed. This method, however, although attractive for its simplicity, presents the following drawbacks:

a) In the presence of noise the bit-error rate is twice that of conventional “level” codes, because a single bit error in the detection process causes two consecutives bits in error after decoding. This loss of performance could often be significant, especially in case of satellite links.

b) Bit errors, although randomly distributed, always appear in groups of two. If a coding is used which permits detection of all single errors.its effectiveness will be destroyed. The same applies for coding which provide single error correction capability.

As an example, the ESRO PCM Telecommand Standard makes use modified (12,8) Hamming code for the command words (correction is one bit) and of a “two-out-of-four” code for the Mode words capability is one hit). In this case, the possibility of using code to solve the PSK ambiguity is clearly ruled out.

A second and widely used method is to compare a part of the message for which “a priori” knowledge is available (usually the synchronization codes) with the expected one. A bit-by-bit comparison allows to decide whether an inversion in the message has taken place.

The major disadvantage of such a method is that once a message inversion has occurred, one has to wait until the next synchronization code is received.

Since very little of the information capacity of the channel is usually allocated for the transmission of the synchronization codes the average response time of such a system could be exceedingly long. Again, for satellite link, a fast correcting action to a sub-carrier phase inversion is often a very desirable feature.

2.2 Proposed anti-ambiguity system

2.2.1 Principle of operation The basic philosophy here consists in comparing the output of a conventional synchronous PSK demodulator (ambiguous) with the output of a special, non-ambiguous, PSK demodulator. As it will be shown later, the actual performance of this special demodulator (in terms of output S/N ratio) does not need to match that of the synchronous one: in fact it could even be much worse. It is this last consideration that makes such an approach feasible.

Let us suppose for the moment that such a non-ambiguous demodulator is available, then the block-diagram of the anti-ambiguity system will look like the one of Fig. 2.2.1. The outputs of demodulators A and B are added “modulo 211 and the results of this comparison provides the information about the “true” or “complement” state of demodulator A output in the form 0 a “high” or “low” D.C. level.

The integrator which follows the “modulo 2" adder is used to reduce the amount of noise (mainly contributed by demodulator B) superimposed to the D.C. signal before attacking the decision circuit. The integration time constant directly affects the performance of the system because

a) it sets the time necessary to take a correcting action after a change in the output of the “modulo 2" adder has occurred.

b) in the presence of additive noise it determines the rate at which false corrections due to noise occur (i.e. complementing demodulator A output when this is in the “true” state).

The output of the integrator is fed to the decision circuit which is basically a threshold circuit whose output controls the sign of demodulator A output.

It is clear from the foregoing discussion that the key element in the system is the non-ambiguous PSK demodulator B. Its principle of operation is described in the following section.

2.2.2 Non-ambiguous PSK demodulator A direct, non-ambiguous PSK demodulator can be achieved according to the following principle of operation. The PSK signal (B in Fig. 2.2.2) is delayed of one half subcarrier period to give the signal C. B and C are then added together. This simple arrangement provides, at the output of the adder, a signal (D) which contains all the information necessary to the non-ambiguous reconstitution of the PCM message. In fact, referring to the timing diagram of Fig. 2.2.2, where for convenience a square-wave PSK has been drawn, we see that at each beginning of a bit we have:

a) a positive pulse of half sub-carrier period duration for “01” transitions in the PCM message.

b) a negative pulse of the same duration for “10” transitions.

c) zero for no transitions.

In order to reconstruct the original PCM message in its “level” form a simple “set-reset” logic will store the information at the output of the adder until the next change of bit value in the PCM message occurs.

Analitically, the demodulator operation can be described as follows: Let the input PSK signal be expressed by

$$e_1(t) = \delta(t) \sin \frac{2\pi}{To} t = \delta(t) \sin \omega_o t$$

where To is the sub-carrier period and $\delta(t) = \pm 1$ conveys the binary information associated with the PCM message.

The delayed PSK is expressed by

$$e_2(t) = \delta\left(t - \frac{To}{2}\right) \sin \omega_o \left(t - \frac{To}{2}\right) = -\delta\left(t - \frac{To}{2}\right) \sin \omega_o t$$

Let us consider now the sum of $e_1(t)$ and $e_2(t)$ during the genetical bit-interval of duration T_B

$$\left[e_1(t) + e_2(t)\right]_o^{T_B} = \left[e_1(t) + e_2(t)\right]_o^{To/2} + \left[e_1(t) + e_2(t)\right]_{To/2}^{T_B}$$

Remembering that the delay of 1/2 To causes the overlap in time of the first half sub-carrier cycle at the beginning of each bit with the last half sub-carrier cycle of the preceeding bit, let δ_n be the binary value associated with the n^{tn} bit and $\delta_{n-1}$the binary value of the $(n-1)^{th}$ bit. According to the values of δ_{n-1} and δ_n. the sum of $e_1(t)$ and $e_2(t)$ yields

$$\left.\begin{array}{ll} e_3(t) = 2 \sin \omega_o t & \text{for } \delta_{n-1} = -1 \text{ and } \delta_n = +1 \\ e_3(t) = -2 \sin \omega_o t & \text{for } \delta_{n-1} = +1 \text{ and } \delta_n = -1 \\ e_3(t) = o & \text{for } \delta_{n-1} = \delta_n \end{array}\right\} \quad o < t < \frac{To}{2}$$

$$e_3(t) = o \qquad \text{for any } \delta_{n-1} \text{ and } \delta_n \qquad \frac{To}{2} < t < T_B$$

We can see that the beginning of each bit is marked by:

a) a positive half sub-carrier period for “01” transition

b) a negative half sub-carrier period for “10” transition

c) zero for absence of transitions

As previously shown the information contained in $e_3(t)$ is sufficient to allow non-ambiguous reconstruction of the PCM message.

2.2.3 Hardware implementation In view of a possible application for satellite telecommand PSK demodulators a prototype of an anti-ambiguity system has been built following the guidelines indicated in the preceeding sections.

In the solution proposed an effort has been made in order to keep the amount of hardware to a minimum to satisfy stringent requirements on weight and power consumption.

The system is shown in block-diagram form in Fig. 2.2.3, where the main PSK demodulator (called “demodulator A” in Section 2.2.1) is of the squaring loop type.

The anti-ambiguity system, shown in the box with dashed lines, requires only the input PSK signal and a signal at twice the sub-carrier frequency ($2x\ f_o$) readily available from the squaring loop.

The demodulator of the anti-ambiguity system follows closely the model of Fig. 2.2.1. However, since it employs digital rather than analog techniques, the adder of Fig. 2.2.1 has been replaced by the two comparator gates A and B; these provide pulses on two separate lines to set and reset the memory flip-flop, corresponding to “01” and “10” data transition respectively. In practice, the function of gates A and B and of the memory flip-flop are assured by a single J-K type flip-flop. The time delay is achieved by means of a shift-register. A complete circuit diagram of the anti-ambiguity system is shown in Fig. 2.2.4

3.1 Measured performance The tests carried out on the system described in the preceeding sections were intended to determine the influence of modulation parameters and of the integrator time constant on the system response time to a sub-carrier phase inversion and to establish the average rates of false corrections in the presence of noise.

Sub-carrier/bit-rate ratios of 4 up to 32 were used, the PCM code being split-phase level.

Results are indicated in Fig. 3.1.1 and are fairly independent from the value of the integrators time constant. The system was tested with S/N ratios down to 0 dB in a band equal to twice the sub-carrier frequency, the phase of the reconstituted sub-carrier being switched alternatively between 0° and 180°. Test results indicate that the response time rises fairly smoothly from T_{Ro} in the noiseless case up to $2\ T_{Ro}$ at 0 dB, indicating that no threshold effects occur.

As regards the average rates of false corrections due to noise results are shown in the curves of Fig. 3.1.2.

The integrator time constant was chosen so to have T_R equal to 2,4 or 8 bits. Each family of curves corresponds to a given T_R, and the single curves are related to different sub-carrier/bit rate ratios. These curves show that very good performance in terms of false correction rates are obtained in conjunction with response times of very short duration.

From the curves above two other sets of curves can be derived, which can prove useful for the design of such a system. The first (Fig. 3.1.3.) relates the error-rate to the time delay TR for a given signal-to-noise ratio; the second (Fig. 3.1.4) is useful to determine the minimum TR allowed for a given error-rate and for a given signal-to-noise ratio. These curves are valid with good approximation for sub-carrier/bit-rate ratio up to 16. For the ratio 32 the sets of curves of Fig. 3.1.5 and Fig. 3.1.6 have been derived.

Conclusion A system has been described which, it is believed, will provide substantial advantages over the more classic PSK anti-ambiguity methods.

In particular, no restrictions are to be imposed on the PCM coding and no “a priori” knowledge of the content of some part of the message is required.

The system is ideally suited for low to moderately high sub-carrier/ bit-rate ratios. For ratios greater than 32 good performance in very noisy conditions will require a rather large time constant, thus reducing the system response time to a sub-carrier phase inversion. In the vast majority of space applications, however, ratios greater than 32 are very seldom used. For the same reason, the system is particularly well adapted to function with split-phase codes.

Further, it has been demonstrated that the systems can be built with a limited number of integrated circuits and components making it suited for spacecraft applications.

Finally, it provides flexibility of use since it is very easy to adapt it to the requirements of a particular application by changing the value of a single time constant.

It is worth mentioning at this point that apart from the on-board applications, the system can also be useful for any type of ground PSK equipment either as an ambiguity resolver, as described in this work, or as a direct PSK/PCM converter in all applications (e.g. check-out equipment) where noise performance in not a critical requirement.

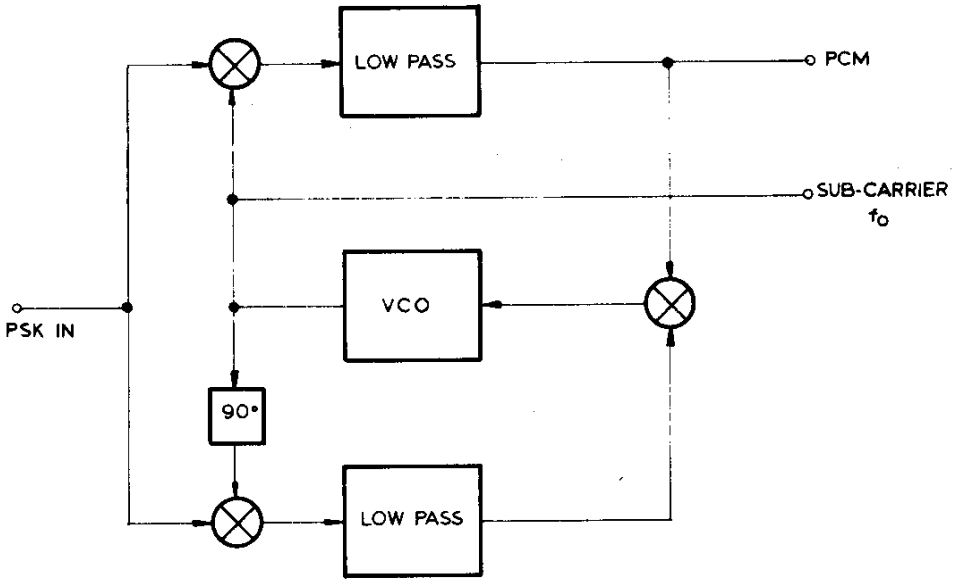

FIG. 1.1.1 QCPL LOOP

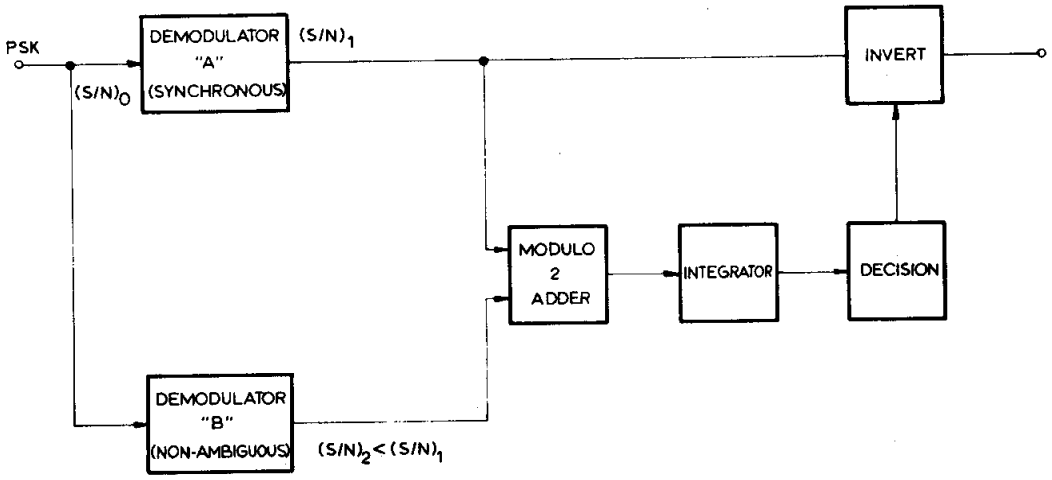

FIG. 2-2-1 ANTI-AMBIGUITY SYSTEM PRINCIPLE BLOCK DIAGRAM

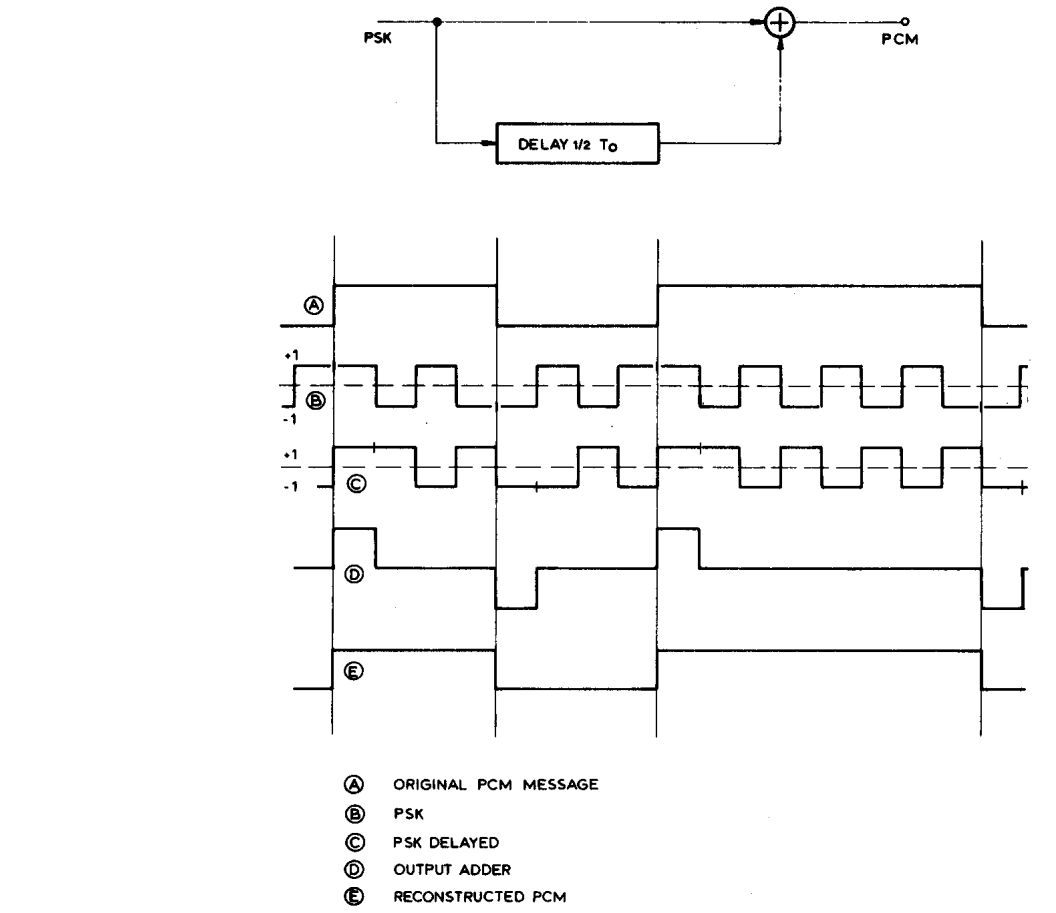

FIG. 2.2.2.

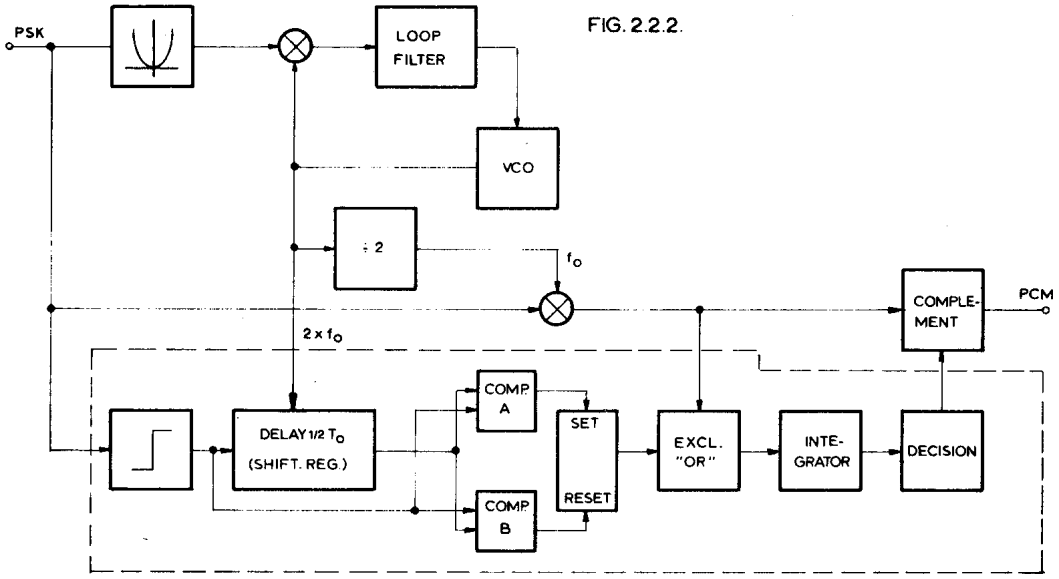

FIG. 2.2.3 ANTI -AMBIGUITY SYSTEM BLOCK DIAGRAM

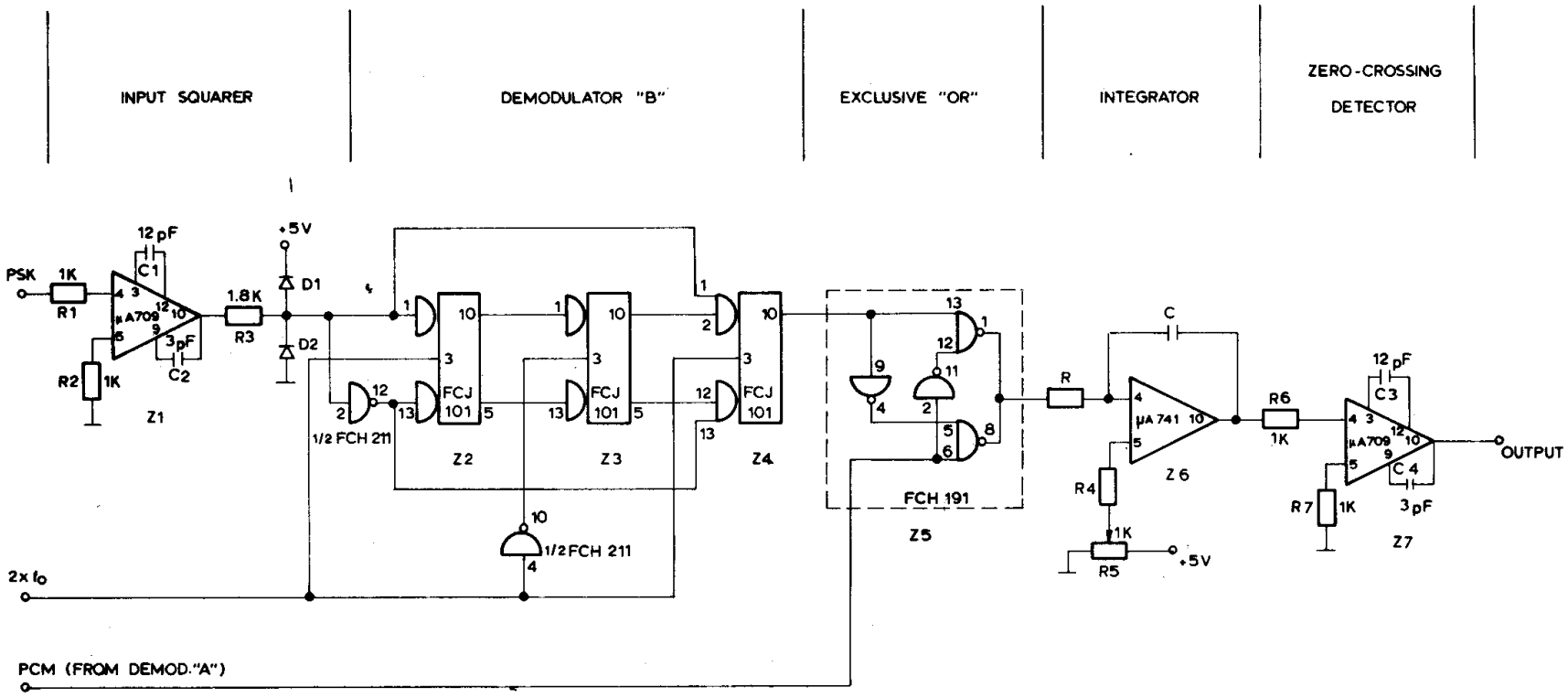

FIG. 2.2.4. CIRCUIT DIAGRAM

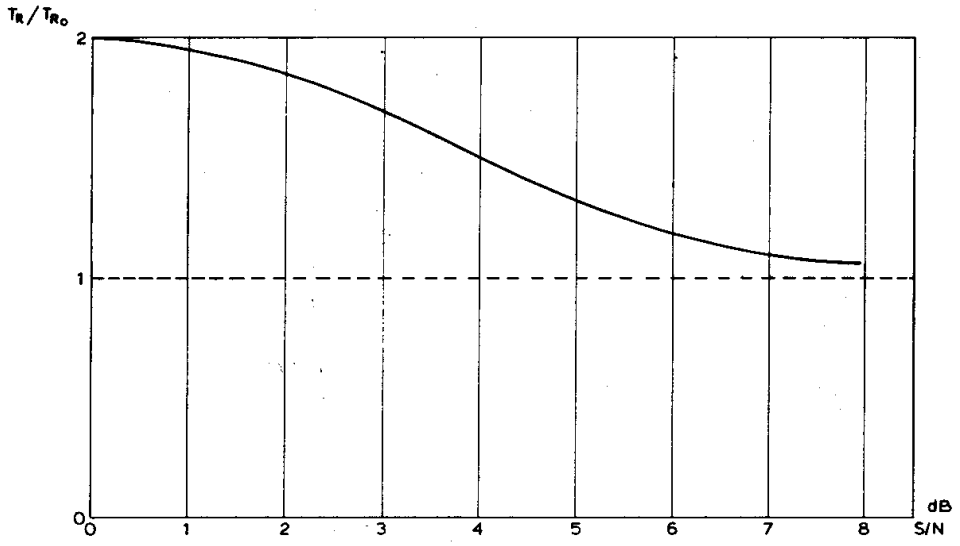

FIG. 3.1.1 SYSTEM RESPONSE TIME WITH NOISE

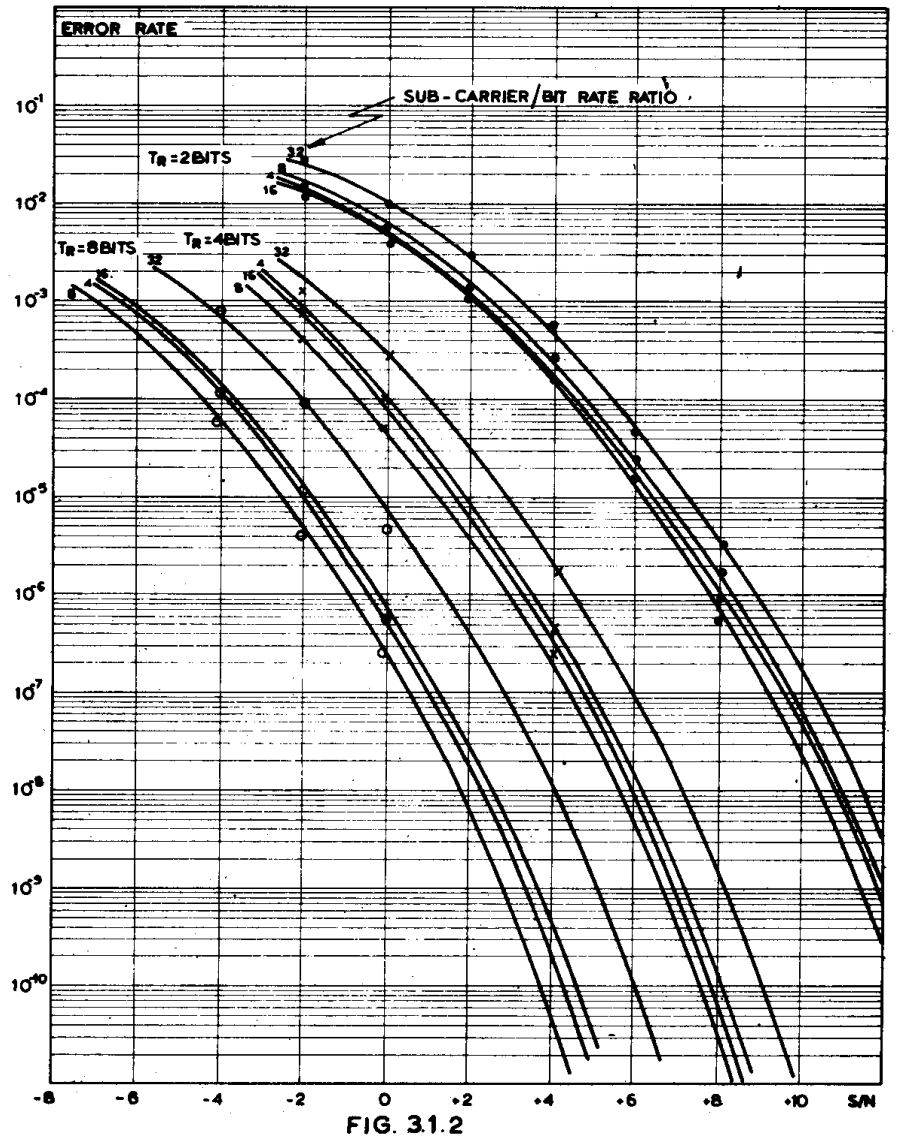

FIG. 3.1.2

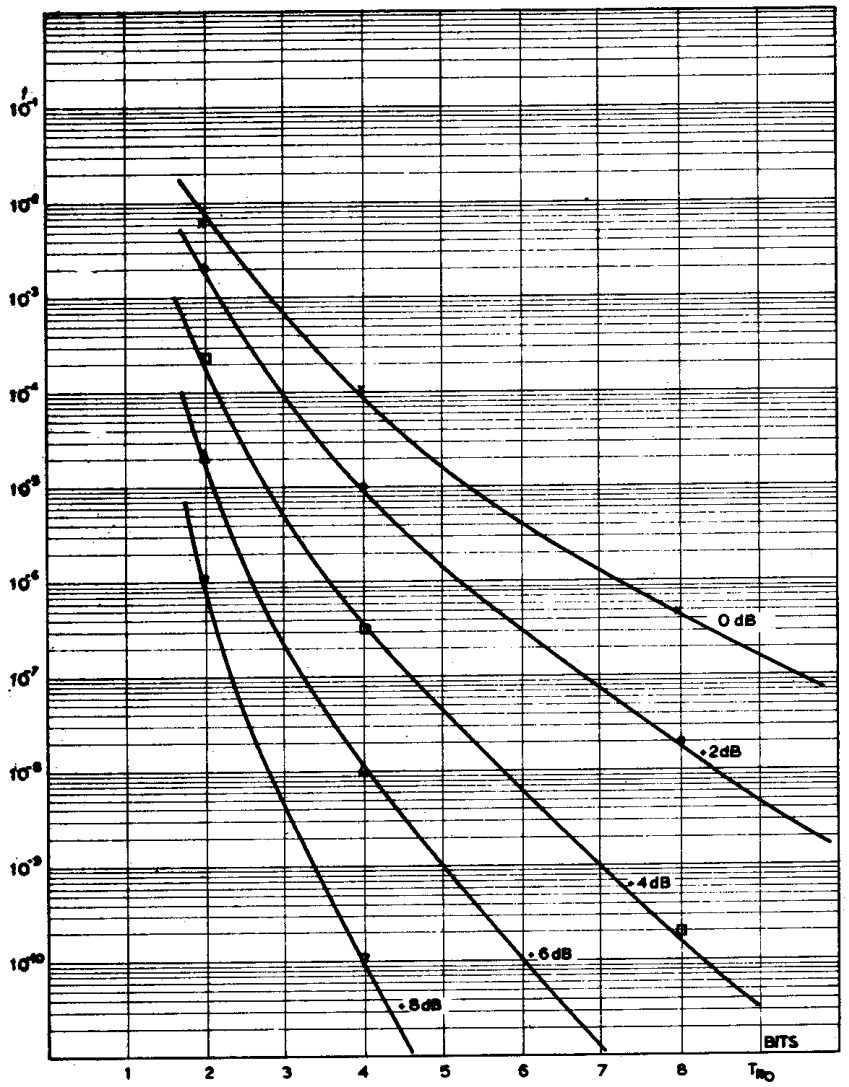

FIG. 3.1.3

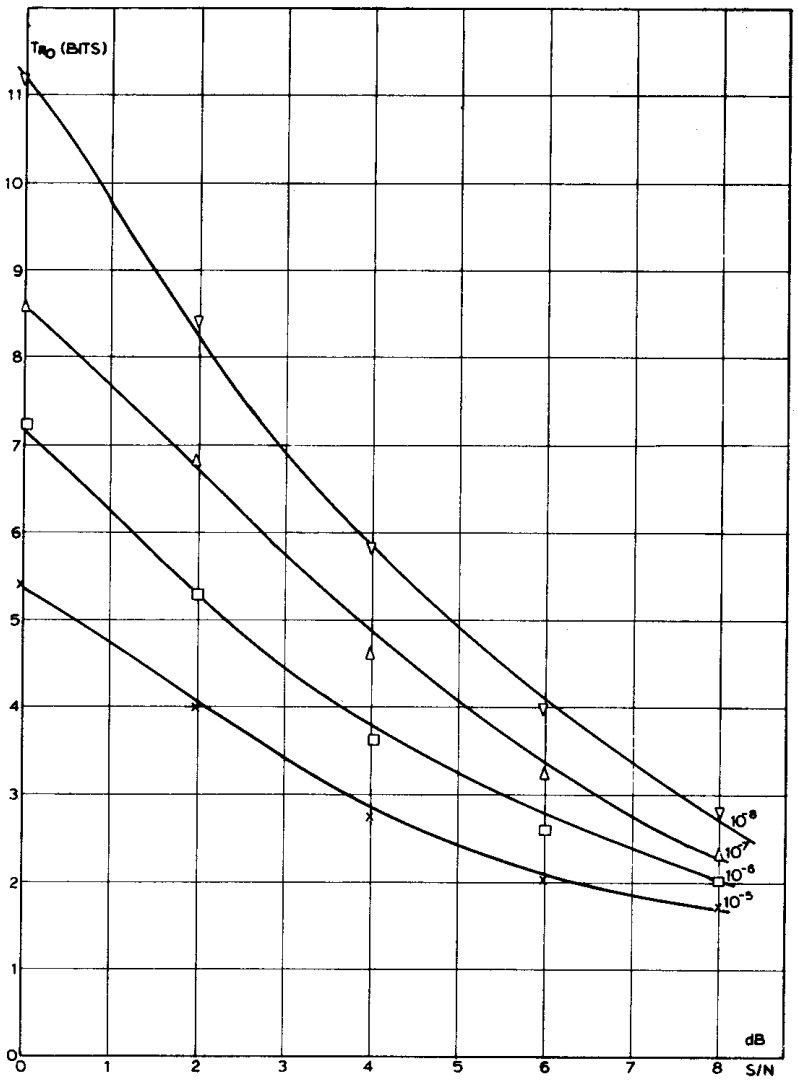

FIG. 3.1.4

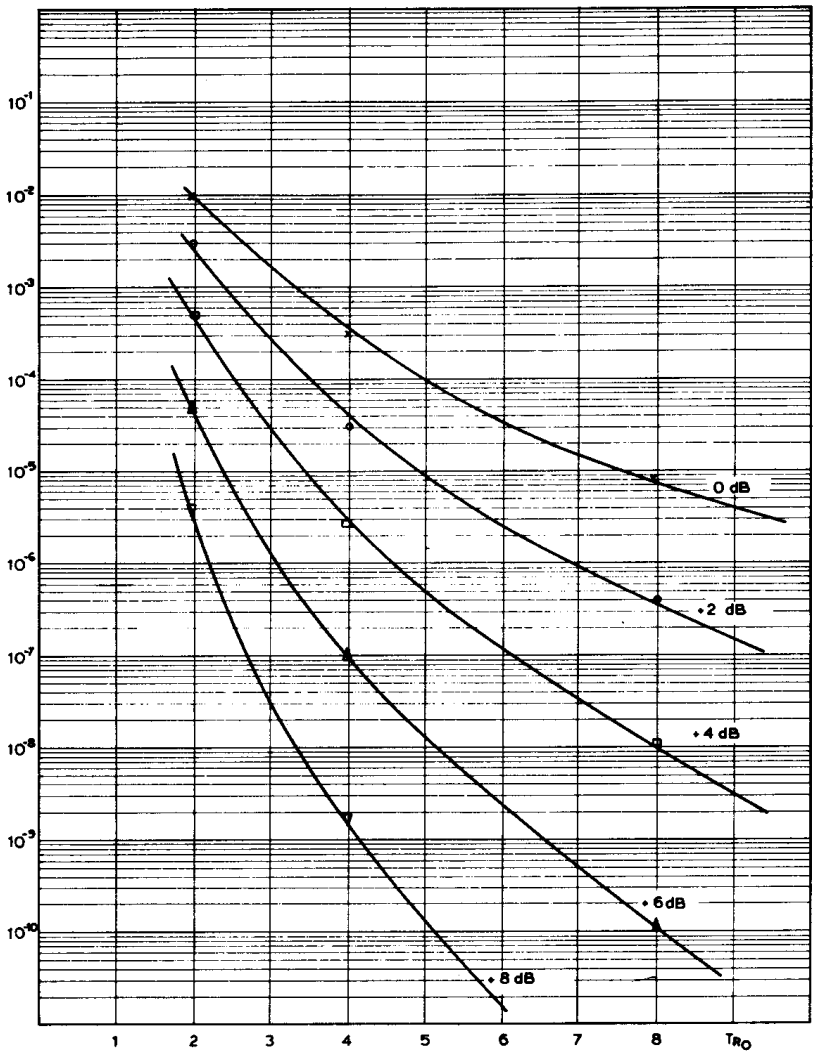

FIG. 3.1.5

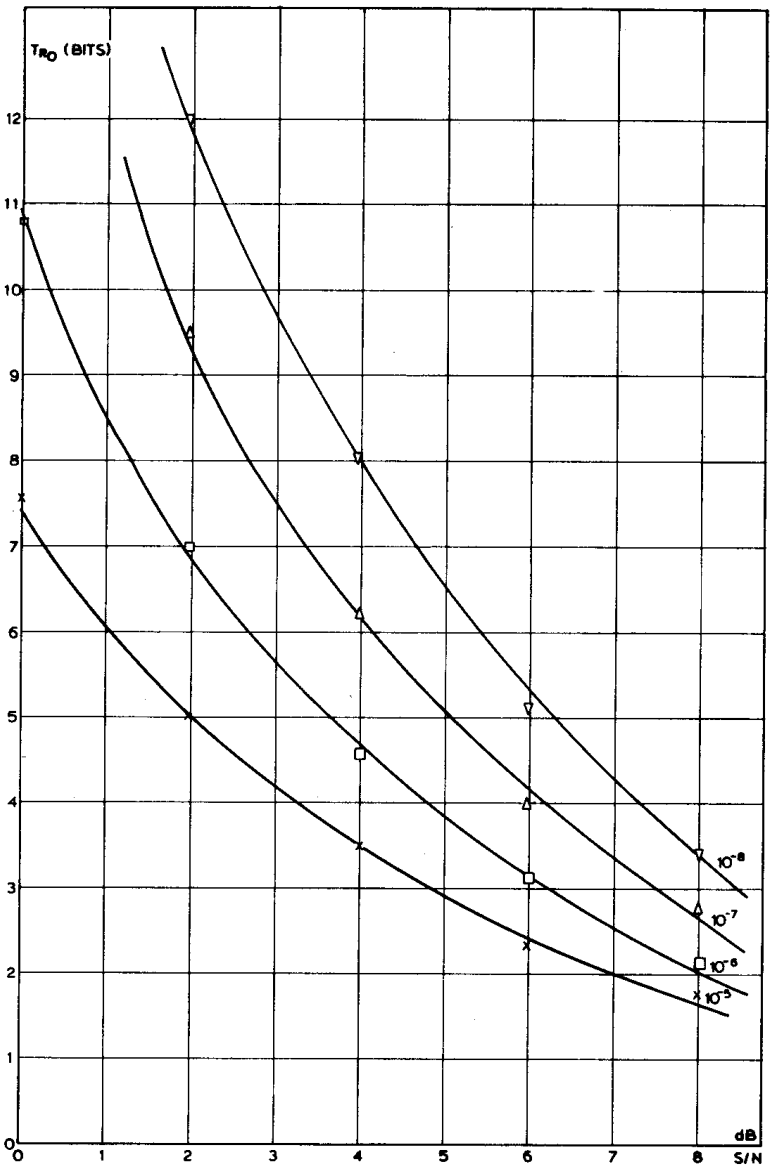

FIG. 3.1.6