

# MULTIMEGABIT OPERATION MULTIPLEXER SYSTEM

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**Summary** The Multimegabit Operation Multiplexer System (MOMS) is a high data rate PCM telemetry unit capable of sampling and encoding 60 scanning radiometer and 4 vidicon channels at 250 kilosamples/second and 5 megasamples/second, respectively. This sampling capacity plus the 7-bit quantization requires a total throughput rate of 40 megasamples/second and 280 megabits/second. To produce these rates efficiently, the system was divided into a pair of identical 140-megabit blocks. A low-power 20-MHz analog multiplexer and analog-to-digital converter were developed together with a video sample-and-hold that features an aperture time error of less than 50 picoseconds. Breadboard testing of these basic building blocks confirmed the design prediction that the total system would consume 27 watts of power. Two 140-megabit output ports are suitable for quadrature modulation.

**Introduction** As a result of the increasing use of imaging sensors for earth resource missions, a need has been created for efficient processing of wideband data. A typical multispectral scanner contains several channels, each with bandwidths ranging from 50 kHz to 1 MHz. Typical vidicon channels use bandwidths of 2 to 5 MHz. To sample and encode this type of data a PCM telemetry system may easily be required to produce serial data streams in the several hundred megabit/second class, with encoder throughput rates of 10 to 40 megasamples/second.

High power and large size are inherent in the techniques conventionally used to multiplex and encode analog data at these rates. Since these factors are no longer acceptable, the primary objective of the MOMS program was to develop a system that would accommodate the required data rates while satisfying the constraints imposed by the spacecraft environment. One requirement was to design a high data rate PCM telemetry system that would sample 60 channels of scanning radiometer-type data at 250 kilosamples/second and 4 channels of vidicon data at 5 megasamples/second. By adding overhead to handle synchronization patterns and minor frame identification, an overall throughput rate of 40 megasamples/second would be required. Because each sample was to be quantized to 7 bits, a bit rate of 280 megabits/second resulted.

This paper describes the unique design approaches to the multiplexer, sample-and-hold, and analog-to-digital converter that resulted in a total system power requirement including the internal power supply losses - of only 27 watts at 280 megabits/second.

**System Description** Figure 1 is a block diagram of MOMS showing that the system has been divided into two identical blocks operating at 140 megabits/second each. Two output bit streams are provided in serial NRZ-L format, phased for use with quadrature modulation techniques, yielding 280 megabits/second of data. The system is made up of a single power supply and crystal oscillator, two 32-channel analog multiplexers, two 7-bit analog-to-digital converters, and two blocks of programmer logic for system timing. Since the two halves are identical, only half a MOMS - a single 140-MHz block - will be discussed.

The analog multiplexer is arranged in a 16 X 5 matrix with two levels of gating. The first tier is formed of subgroups of 5 channels each and addressed at a 1.25-MHz rate. It accepts the signals from the Source A radiometer channels. These sources are driven from 1000-ohm impedances and have a  $\sin x/x$  frequency response with the first null at 80 kHz. Ten Source A channels are compressed, prior to encoding, by a square root function generator. The second tier of gating, which is addressed at a 20-MHz rate, accepts the outputs of the first tier. Two vidicon channels, dc to 2.5-MHz bandwidth, are sampled by the second tier, having been preconditioned by a video sample-and-hold. Since a 16:1 difference in address rates exists, the first tier is referred to as the low-speed multiplexer and the second tier as the high-speed multiplexer.

The key to the MOMS design is the high-speed, low-power, 7-bit analog-to-digital converter. A two-stage serial/parallel design is utilized, resulting in a total conversion time of 30 nanoseconds and consuming only 3.0 watts. This low power and high speed is made possible by using a new comparator that consumes 80 milliwatts and switches in 5 nanoseconds with 5 millivolts of overdrive. This device represents a significant speed/power improvement over previous designs.

Multiplexer sequencing and A/D converter timing are controlled by the programmer logic, which has been implemented with a current feedback logic that is a major factor in realizing these data rates at low power. By using this new technology, it is possible to achieve a 2 nanosecond/2 milliwatt logic gate which represents an order of magnitude improvement over the closest commercially available logic element<sup>2</sup>. The programmer supplies the serial NRZ-L output Format at 140 megabits/second,

A format for one 140-MHz MOMS block is shown in Figure 2. As illustrated, the system as presently configured has a prime sample rate of 1.25 megasamples/second and a word rate of 20 megawords/second. There are only supercommutated and subcommutated

channels; the broadband Source B video inputs consume 50 percent of the format. MOMS may accept prime channels by feeding inputs directly into the second multiplexer tier, or all subcommutated channels may be used if the Source B inputs are eliminated.

**Analog Multiplexer** The analog multiplexer is organized in the two-tier arrangement depicted in Figure 3. The final tier, the high-speed multiplexer, is made up of eight switches sequenced every 50 nanoseconds. Not all this time is allowed for multiplexer settling time, since the analog-to-digital converter must also complete its cycle within this time period. Two decisions are required to encode seven-bit resolution and the multiplexer must have settled to a small percentage of its final value before the first decision is made in the A/D converter. The time allotted for the multiplexer to settle to 0.1 percent of its final value; and for the first A/D decision to be made within the same accuracy is 28.57 nanoseconds. The low-speed multiplexer, which accepts the bulk of the channels, is divided into 6 subgroups staggered by 50 nanoseconds. This technique permits the selected low speed switch to be ON for 750 nanoseconds before its output is picked up by the final tier. The multiplexer subsystem incorporates both a sample-and-hold and a data compression amplifier. The sample-and-hold accepts signals from a 75-ohm vidicon source that has a bandwidth from dc to 2.5 MHz. Due to the high input rate, aperture time error becomes a significant problem. At full-scale input and maximum frequency, the peak rate of change of Source B data is 1 bit/nanosecond. The sample-and-hold, however, reduces this time error to less than 50 picoseconds. The data compression amplifiers supply a square root compression on 10 Source A data channels through a three-segment approximation to the square root function.

In order to feed signals from multichannel sources into a single A/D converter every 50 nanoseconds, a high-speed analog switch had to be developed. The conventional approach to this problem is to use a quad-diode bridge built with hot carrier diodes and driven from a balanced, floating pulse transformer. In order to build an efficient multiplexer, several switches must be tied to a common buss and the voltage at that point must be able to change the full-scale range in the permitted time. Since many connections are made at a single point, the capacitance of the buss increases in proportion to the number of channels; the current to charge the capacitance and the power required must increase for a fixed settling time. Preliminary design showed that 385 milliwatts for each high-speed channel would be required if a quad-bridge multiplexer were used.

To obtain an efficient high-speed multiplexer system for space applications, the charging current of the multiplexer output capacitance must be minimized. The location in the multiplexer required to change full-scale voltage must be one of minimum capacitance, yet the point where the switches are common must not need to change large potentials. The apparent paradox may be solved by the approach shown in Figure 4.

Assume switch SW1 is closed and SW2 through SW8 are open. In this case, a high-gain differential amplifier is made up of an input stage A1, gain stage Q1, and impedance buffer Ao. Negative Feedback is used to close the loop gain to unity, with the output following the input to A1. If SW1 were opened and SW2 closed, the loop would now be closed about A2 and the output would slew to the value of Input 2 to settle out at a rate determined by the response of the amplifier. In this approach a single input stage is used for each channel to be multiplexed. These stages are switched to the input of common base amplifier Q1; thus, the paradox requirements are answered. The point in the circuit where the switches are common does not change full-scale voltage. The collector junction of Q1 is the only point that must change full scale and so appreciably affect response time. The capacitance is minimum at this location.

By implementing the high-speed multiplexer in this manner a total dissipation of only 642 milliwatts is required for 8 channels. If the quad-diode approach had been used, over 3 watts would have been used. Furthermore, the individual input stages isolate the driving source from switching transients that would reduce response times. There is no requirement for expensive, large, magnetic components. When compared to the quad-diode approach, the programmable amplifier multiplexer has improved accuracy, since the overall feedback reduces the error sources to the errors of a single amplifier. This approach also lends itself to monolithic or hybrid technologies.

A photograph of the response of the high-speed multiplexer is shown in Figure 5. The delay time is approximately 5 nanoseconds from the leading edge of the command clock, and the multiplexer has settled to within 0.1 percent of its final value when the first A/D converter decision is made at 28.57 nanoseconds. The multiplexer has a gain-bandwidth product of 66 MHz and a slew rate of 300 volts/microsecond.

The MOMS low-speed multiplexer has adequate time for settling to permit the use of field-effect transistor analog switches if the radiometer outputs were of low impedance. Historically, the major problem area in a multiplexer is the interface with the experimenters. As a channel is selected, the entire output capacitance of the multiplexer input tier is placed across the transducer output impedance. Capacitance at the source, resulting from the wiring harness, must accept charge transferred from the multiplexer, a fact that may result in significant error. For a high-data-rate system where the input tier must settle in less than a microsecond, the error becomes appreciable and is compounded by the experimenter's output amplifier which must respond to the charge transfer

For the MOMS low-speed multiplexer address rates (1.25 MHz) consideration must be given to providing a separate buffer amplifier at the input to each channel in order to provide switching transient isolation. Rather than using a complete amplifier on each input, the programmable amplifier multiplexer approach used in the high-speed section offers

lower power and excellent isolation. This amplifier may be built at lower power than its high-speed counterpart. A curve showing the worst-case calculated charge transfer error of the low-speed multiplexer is given in Figure 6. The solid line represents the calculated error versus source capacitance for a 1000-ohm source resistance; the broken line is the measured data. For any value of source capacitance, the error due to charge transfer will be less than 0.025 percent of full scale. This figure represents an order of magnitude improvement over conventional multiplexers operating with realistic values of impedance and in the same time frame.

**Sample-and-Hold** The Source B vidicon input characteristics preclude the use of an “online” analog-to-digital converter due to the peak error resulting from aperture time. The MOMS A/D converter has an aperture time of 21.43 nanoseconds, the time between the two A/D decisions. For 2.5-MHz input rates the error would be 16.8 percent; therefore, a sample-and-hold is required to precondition the input signal and reduce the aperture timing ambiguity prior to encoding.

Two general classes of sample-and-holds were considered for the MOMS: the open-loop and closed-loop approaches shown in Figures 7 and 8, respectively. In the open-loop approach an amplifier, A1, isolates the source from the sample gate and storage media. Another amplifier, A2, buffers the capacitor, C1, and isolates it from the load. In this approach the gain, offset, and linearity errors of each amplifier are additive. The closed-loop approach outlined in Figure 8 uses negative feedback around the entire sample-and-hold. The read-in amplifier has high open-loop gain, and the errors due to offset and gain of the switch and A2 are reduced by the gain of A1. For accuracy, the latter approach was selected.

Source B channels must be sampled at 5 megasamples/second; the timing was arranged such that the sample-and-hold would track the input for 150 nanoseconds and hold for 50. A unique approach to implementing the sample-and-hold enabled the stable realizations of the closed-loop approach with the overall amplifier having a gain-bandwidth product of 150 MHz. The storage media was included in a current-to-voltage conversion stage within the read-in amplifier, resulting in virtually a single-pole, open-loop amplifier. A driver, void of transformers, was used to switch from sample to hold mode in a balanced fashion. The complete circuit operates at a closed-loop gain of +3 and consumes 425 milliwatts. More conventional approaches using open-loop configuration and transformer drives could consume four times this power. The photograph in Figure 9 shows a 2.5-MHz input sinusoid sampled at 5 megasamples/second. The effective aperture time is less than 50 picoseconds.

**Analog-to-Digital Converter** The MOMS requires that a 7-bit A/D conversion, and high-level analog multiplexing be performed at a 20-MHz rate under such conditions that

the input could change full scale between conversion cycles. A single voltage comparison for each of the 127 quantizations levels would provide the fastest and most straightforward technique, but since 127 comparator amplifiers would be required, the all-parallel approach is impractical. A scheme of conversion - referred to in technical literature as subranging - serially performs two parallel decisions. It may be implemented with medium complexity and high speed. The MOMS A/D converter decides the three most significant bits with a 7-comparator parallel decision 28.57 nanoseconds after the multiplexer switches. Based upon the first-tier decision, the reference is adjusted to a 15-comparator second tier with the four least significant bits decided 21.43 nanoseconds later. The reference is adjusted by means of a digital-to-analog converter.

Figure 10 shows the basic operation of the A/D converter. Comparator amplifiers A1 through A7, biased at multiples of 1/8 full scale, make up the first tier. The unitary outputs of the comparators are converted to binary by the conversion logic. They also drive the digital-to-analog converter biasing the second tier. The second tier includes A8 through A22 and the 15-bit unitary-to-binary conversion logic. The first tier actually tracks the output of the multiplexer as the multiplexer settles to its final value. By using a unitary D/A converter rather than a binary one, the time required to map logic codes (5 to 10 nanoseconds) does not take away critical settling time. Each comparator in the first tier is internally latched 28.57 nanoseconds after the encode cycle starts. The second-tier comparator outputs are clocked into storage resistors 21.43 nanoseconds later, and the unitary-to-binary conversion is then completed.

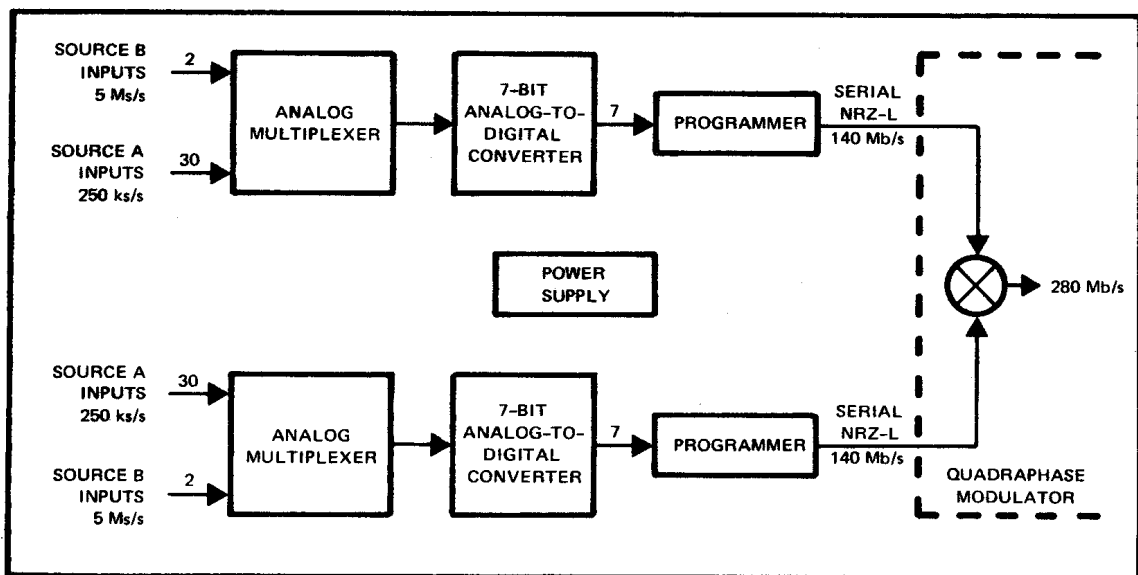
The key to realizing a low-power serial/parallel encoder is the comparator amplifier. The two types designed for MOMS differ only by the fact that one version contained a circuit that would latch the output on command. This circuit, shown as a block diagram in Figure 11, was used in the first tier and had an 87 milliwatt power dissipation. Removal of the latch circuitry, A4 and A5, for use in the second tier reduces power to 54 milliwatts. Both comparators responded in 5 nanoseconds for a 5-millivolt overdrive; the latch circuit had a response of 2.5 nanoseconds. Photographs of these responses are shown in Figures 12 and 13, respectively. In order to obtain this speed - power performance transistors with extremely small geometry were used. This selection led to a problem of thermal hysteresis due to the imbalance in power dissipation in the differential input stage of the comparator. Since the power dissipation depends on the input signal to the comparator, dynamic crosstalk (in a multiplexed system) results.

The complete MOMS A/D dissipated 3 watts, including code conversion logic. To the authors' knowledge, this figure represents the lowest power figure available for a 7-bit, 20-MHz converter. The static performance over a 70°C temperature range was better than  $\pm 1/4$  bit, and dynamic crosstalk was no more than  $\pm 1/2$  bit when operated with the multiplexer.

**Conclusions** The primary concern of the MOMS program was to develop and demonstrate the basic building blocks needed to produce a high-bit-rate PCM telemetry unit for space applications. Unique low-power circuit designs resulted in a system that operates at a total bit rate of 280 megabits/second and consumes only 27 watts. Significant circuit developments were an 80-milliwatt/channel, 20-MHz analog multiplexer; a 425-milliwatt sample-and-hold with less than 50 picoseconds aperture ambiguity; and a 3-watt, 140-megabit/second 7-bit analog-to-digital converter.

## References.

1. W. T. Burton, Jr. et al., "Multi-Megabit Operation Multiplexer System (MOMS)," Final Report.
2. J. S. Gray, "Recent Advances in High Bit Rate Technology," Microwave System News, January 1973.



**Fig. 1 - Block Diagram of the MOMS High Data Rate PCM**

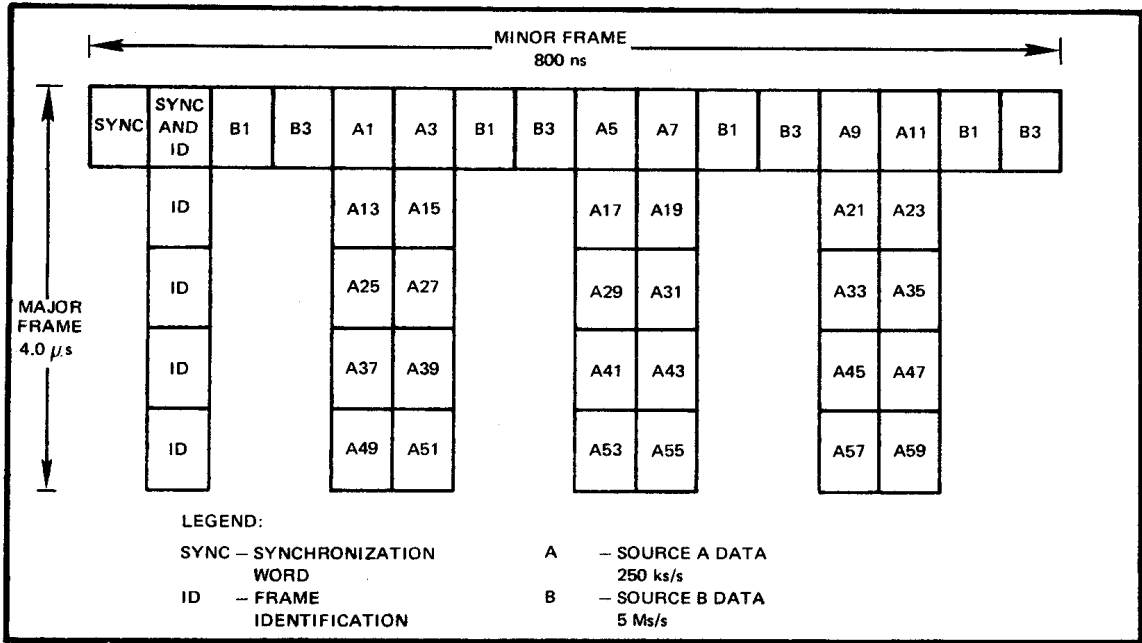


Fig. 2 - The Format for a 140-Mb/s MOMS Block

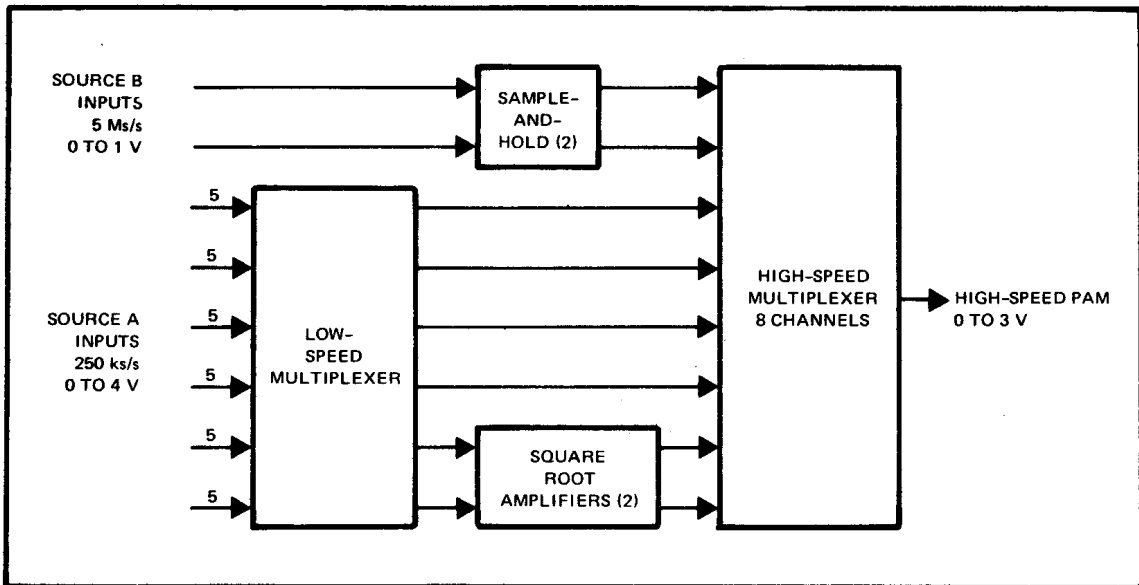
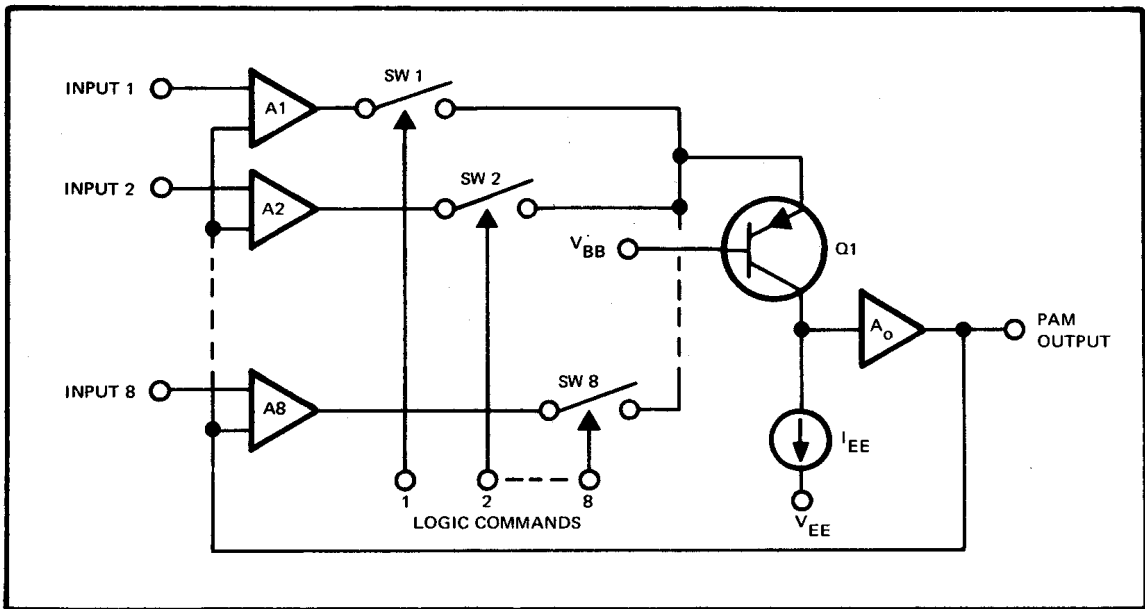
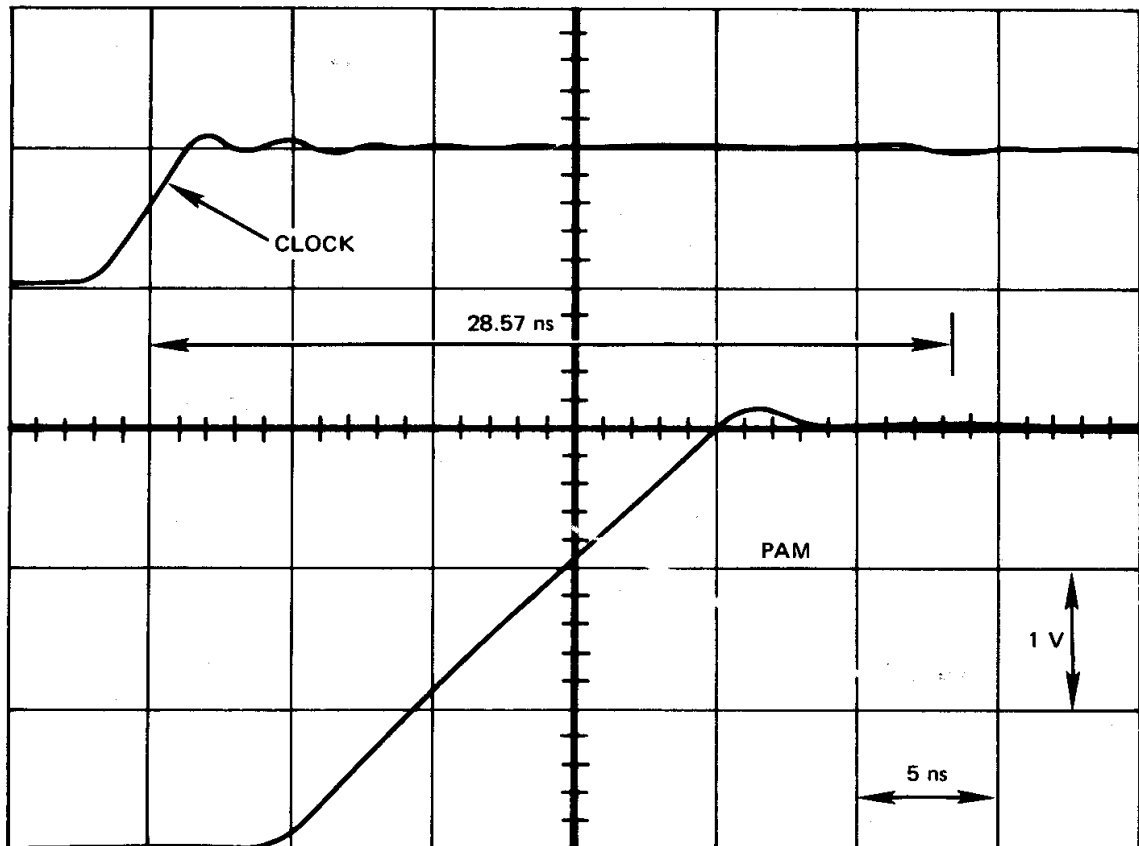


Fig. 3 - Multiplexer Subsystem

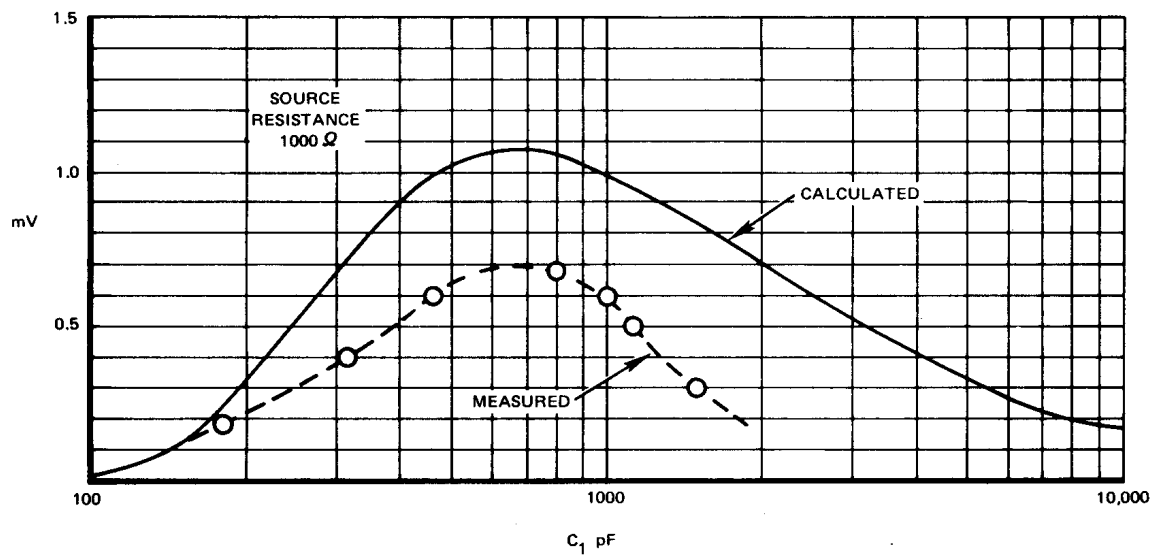




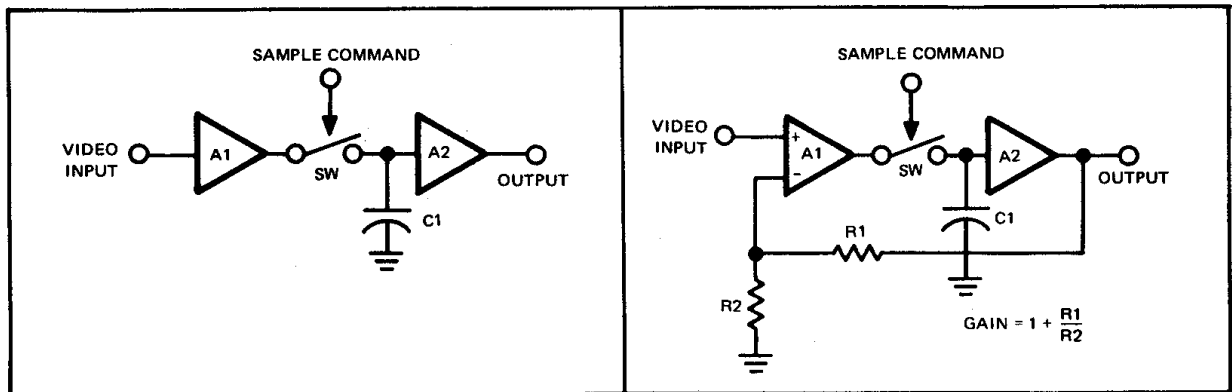
**Fig. 4 - Programmable Amplifier Multiplexer**



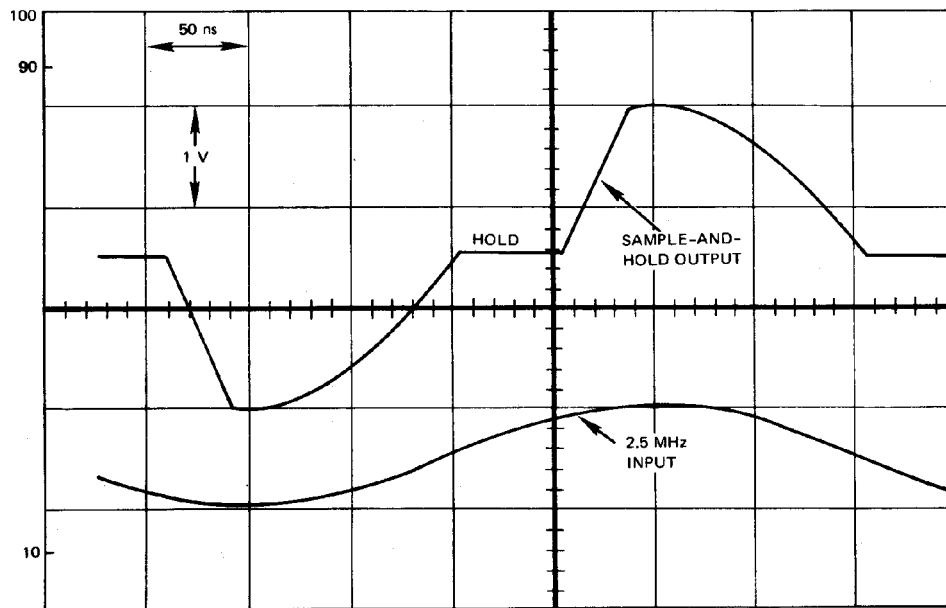
**Fig. 5 - High-Speed Multiplexer Response**



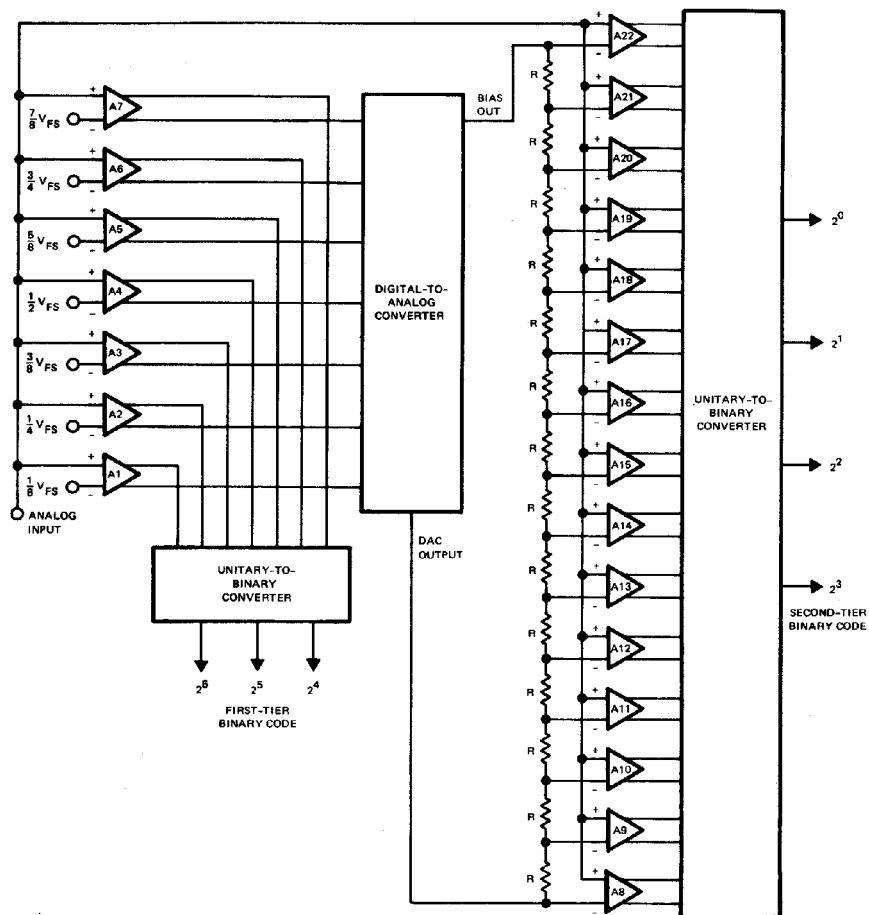
**Fig . 6 - Charge Transfer Error Versus Source Capacitance for the Low-Speed Multiplexer**



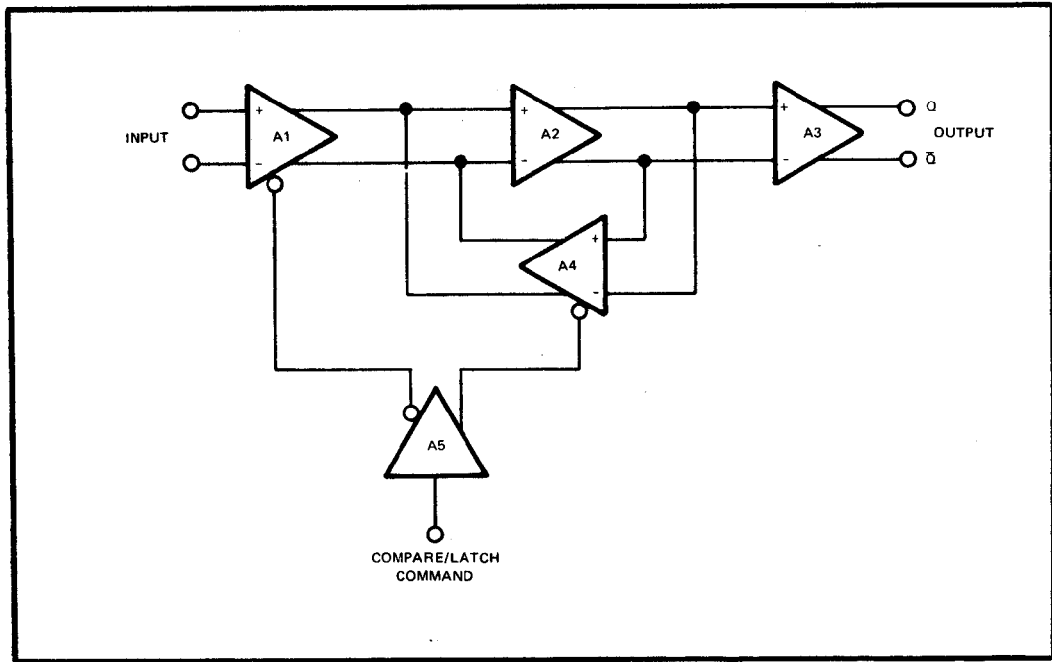
**Fig. 7 - Open-Loop Sample-and-Hold      Fig. 8 - Closed-Loop Sample-and-Hold**



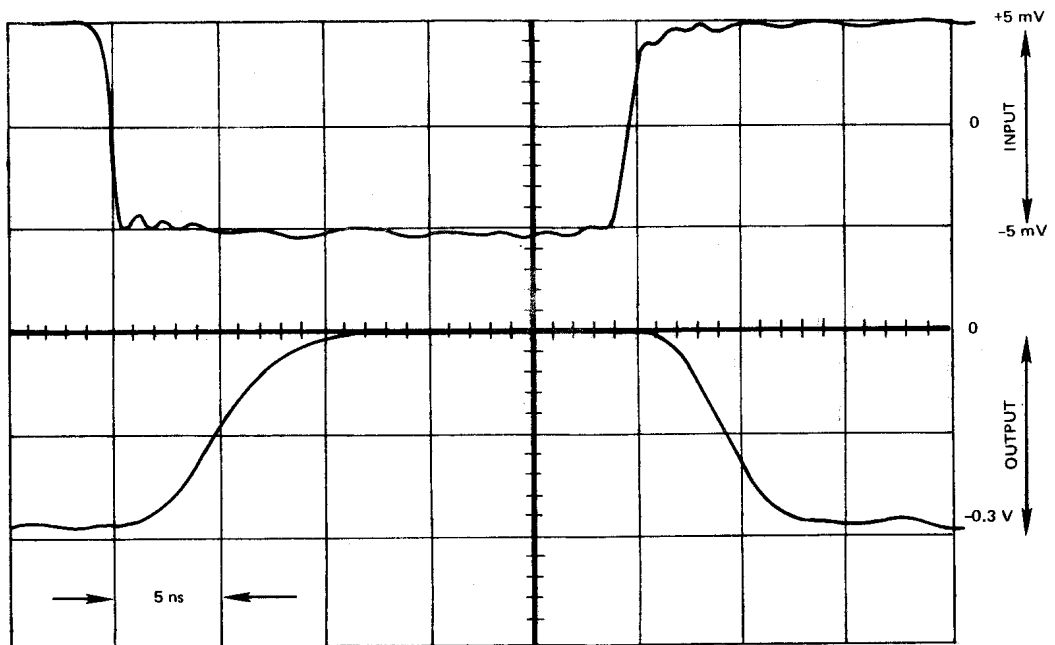
**Fig. 9 - MOMS Sample-and-Hold Operation at 5 Ms/s and 2.5-MHz Input Signal**



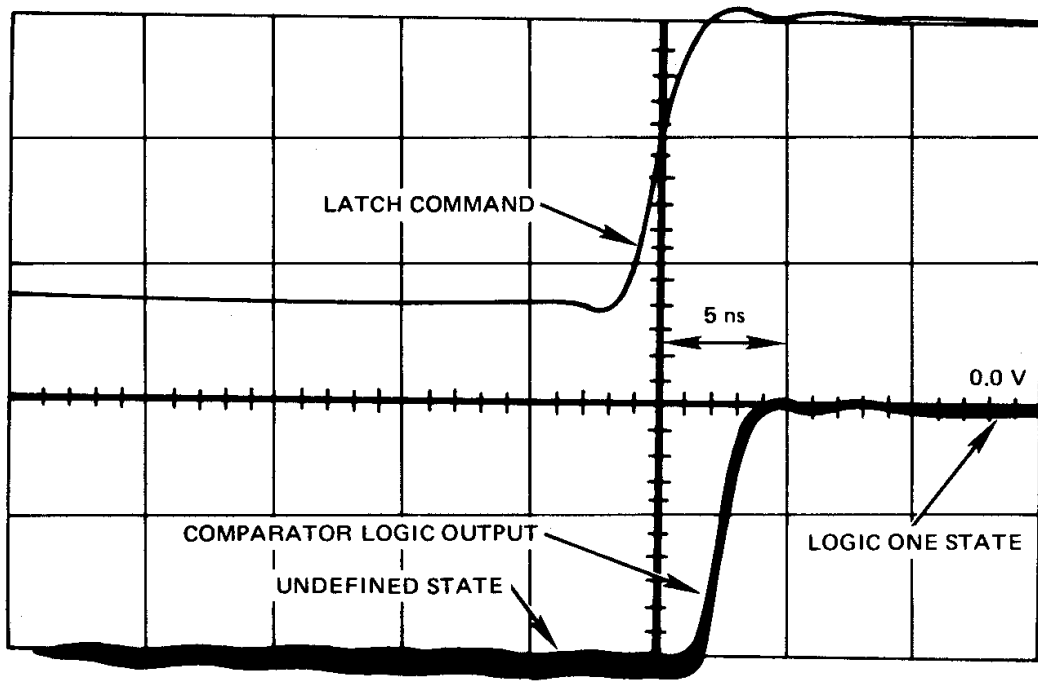
**Fig. 10 - MOMS Analog-to-Digital Converter**



**Fig. 11 - MOMS Comparator Amplifier, Block Diagram**



**Fig. 12 - MOMS Comparator Small Signal Step Response Logic Output, Normal Operating Conditions**



**Fig. 13 - MOMS Comparator Latch Response**