A DISTRIBUTION CONTROL UNIT FOR SATELLITE-SWITCHED COMMUNICATIONS

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Summary Traffic estimates for the next generation of commercial communications satellites strongly indicate the desirability of using highly directive multibeam antennas to increase channel capacity. This antenna configuration allows multiple access via space division and frequency sharing through the isolation inherent in the directive multibeam antenna. Coupling this technique with a satellite-borne programmable communications distribution subsystem results in a highly efficient system. The distribution subsystem, consisting of a distribution control unit (DCU) and microwave switch matrix (MSM), is introduced into the satellite communications equipment prior to the output amplifiers and enables interconnection between all earth terminals accessing the satellite. Data on the traffic flow allocation required to provide service is stored in an onboard memory and is used to directly control MSM operation.. Flexibility to adapt to changes in traffic flow patterns is achieved through ground command of the onboard memory contents. A detailed description of the DCU and a general discussion of the space segment are provided.

Introduction Future high-capacity communications satellites will probably employ highly directive antennas to generate narrow or spot beams. This will permit frequency reuse through spectrum sharing and will significantly increase the e.i.r.p. of the satellite. To permit earth stations illuminated by one beam to communicate with earth stations in other beams, it is necessary to interconnect the beams in the satellite. one method especially applicable to TDMA transmissions is cyclical interconnection of the beam signals in rapid sequence by using a satellite-borne distribution subsystem controlled by a highly stable onboard sequencer. Earth stations in the network would then synchronize their transmissions to the satellite-generated switching sequence, and would thus use TDM/ TDMA for communicating with other stations. The space segment of this system, called the distribution subsystem (Fig. 1), consists of a microwave switching matrix (MSM) and a distribution control unit (DCU). These two elements operating together perform the programmed switching operations necessary to interconnect the communications beams accessing the satellite.

The space-borne distribution subsystem is introduced into the conventional transponder equipment prior to the output power amplifiers. In system operation the n up-link beam's and n down-link beams are interconnected in a programmable frame by the MSM under control of the DCU. Data on traffic flow required to allocate capacity is stored in a small memory in the DCU and used to directly control operation of the MSM. Flexibility to adapt to changes in traffic flow patterns is achieved through ground control of the DCU memory contents. Complete or partial restructuring of the switching frame for changes in traffic can be set up in a few seconds and initiated without disrupting normal traffic flow.

Distribution Subsystem Requirements The onboard distribution subsystem causes up-link signals to be switched among the down-links on a time-division basis. A matrix array approach to signal switching makes it possible for each input to reach any output. To simplify matrix design and to eliminate switching of local oscillators, all signal inputs to the matrix are to be at the same frequency.

The basic frame period is subdivided into a number of time intervals during which input/ output connections remain fixed. Signal switching is accomplished between these intervals. Since each up-link signal is to be capable of reaching all down-links simultaneously, the number of switching intervals is generally required to be at least equal to the number of signal inputs to the matrix. Actually, the number of switching intervals is much greater since traffic patterns among earth stations are not balanced; therefore certain interconnections must consist of multiple switching intervals.

Switching on a time-division basis in which the shortest time interval is a few microseconds requires rapid switching to eliminate costly guard time; thus, a solid-state switch must be used. Also, the switches must be lightweight, which is another feature of solid-state switches. Based on these considerations, PIN diodes have been chosen as the switching device.

In addition to the switch matrix, the distribution subsystem must contain a device to control switch positions within the matrix. This device must be capable of providing switching signals on a time-division basis by establishing a frame period of 750 μsec, subdivided into "frame units" of equal length, and it must maintain the switching pattern from frame to frame.

Design Approach Selected Once the concept of onboard switching[1] had been developed and its potential advantages established, various technical problems were solved. Important among these are control of matrix switching and establishment of system synchronization.

On-line control of matrix switching from the ground requires a relatively complicated receiver onboard the satellite since bit errors cannot be tolerated and has been ruled out by power and reliability constraints. In addition, it is recognized that a distribution pattern will require updating at most only a few times each day; thus, it has been decided to place a memory device onboard the satellite to store the repetitive frame pattern, which also helps to reduce the earth station burden.

Initial loading of the onboard memory and changes of its content are controlled from the ground. Also, memory patterns are originated on the ground. Since a memory pattern will require changing only a few times each day, the typical command link is quite satisfactory for the update task. Actually, there are two memory units onboard the satellite; one is the operating memory, which controls the MSM, and the other is a buffer memory, which receives update patterns from the satellite command system.

A signal input to the MSM is switched among the down-links on a time-division basis; hence, it is necessary for each station to time its transmission to arrive at the satellite in phase with the switching of the matrix. System synchronization is achieved by using a technique proposed by Shimasaki[2] in which each station independently synchronizes with an autonomous system clock located onboard the satellite.

Time window gating is the basis of this technique. Specifically, each frame is divided into time intervals, termed frame units, which are the shortest programmable increments of time for MSM switching purposes. The 750-µsec frame period is divided into one hundred twenty-four 6-µsec programmable frame units for communications transmission, and one 6-µsec synchronization interval. During the synchronization frame unit, each station can receive its own transmission, which is referred to as loop-back. That is, the switches within the MSM are positioned so that each up-link signal will be routed to its corresponding down-link rather than to another system member’s down-link. Therefore, if a characteristic signal transmitted by a station is timed to arrive at the satellite during the loop-back interval, it will be returned to that station and detected. If it is incorrectly timed, the characteristic signal will arrive at the satellite at some time other than during the loop-back interval, and therefore it will not be returned to the station that sent it.

For initial synchronization [2] a search procedure is followed, in which the station periodically rephases its characteristic signal until it is detected. Proper placement of this characteristic signal with respect to the loop-back slot establishes the correct timing for each subsequent data burst.

DCU Design Description The DCU contains the autonomous system clock and associated timing circuits, operating memory, MSM interface, buffer memory, and T&C interface, as shown in Fig. 2. The three modes of DCU operation are normal, update, and

operating memory verify. DCU mode selection is by command. The system clock, operating memory, and MSM interface function in all three modes, while the T&C interface and buffer memory are needed only during update and operating memory verify operations.

The DCU is basically a fixed-function, digital device designed to control the status of the MSM. The dynamic switching of the matrix is organized into repetitive frame intervals of 750 μsec, and the switching pattern within each frame is determined by the contents of the operating memory. As stated previously, the 750-μsec frame is divided into one hundred twenty-four 6-μsec programmable frame units for communications, and one 6-μsec synchronization interval to allow for terrestrial equipment synchronization.

A high-stability crystal oscillator within the DCU is the autonomous system clock that provides the central timing reference for the system by timing the MSM switching.

Control of the MSM switch connections is accomplished by decoding a binary word which causes each switch junction to be either open or closed. The control word is read from the operating memory into a holding register (part of the MSM interface) whose output is decoded.

The MSM is to be operated under the restriction that the input/output connections must be one-to-one; ie., each input must be connected to only one output and each output must be connected to only one input during any single frame unit. Hence, for an n x n MSM, where n is the number of input/output ports, the control word is organized into subwords each composed of k bits. Each k-bit subword is the code for connecting an input to any of the n outputs. Therefore,

$$k \geq \log_2 n$$

and the total code word length is nk bits. The most efficient coding results when $\log_2 n$ is an integer.

Consider a 16-input/16-output MSM in which each input is connectable to any output with the restriction that the connections must be one-to-one. A four-bit word is required to select one of the 16 possible output lines for each input; hence, a total of 16 x 4 or 64 bits are necessary to position the MSM switches for each frame unit. Since there is a total of 124 data frame units per frame, 7,936 bits must be stored in the operating memory for the MSM control.

Data is output to the MSM interface buffer from the control memory at the rate of one 64-bit word every 6 μsec. The parallel data word is used in four-bit subwords by a 1-of-16

decoder for each row to determine which one of the 16 outputs will be connected to the row input. The operating memory outputs a data word every 6 μsec for 124 consecutive frame units; at the 125th frame unit, no word is read from the operating memory, but instead the hardwired loop-back code is strobed into the holding register. The 125th frame unit is the synchronization interval during which the MSM configuration causes each up-link signal to be returned to the corresponding down-link. At the end of the 125th frame unit, the same 124data words are again read out of the operating memory during 124 consecutive frame units, and then at the 125th frame unit the hardwired code is read out. This operation is repeated continuously.

Because traffic patterns change as a function of time of day and perhaps as a result of special events, the distribution of frame units among the various users will require updating so that the system can adapt to traffic needs. Update patterns are originated on the ground and sent to the onboard DCU via the command link. Upon command, the DCU is placed in a mode to receive a serial bit stream from the command decoder.

To ensure its correct reception at the satellite, the update pattern, as received, is stored in a buffer memory, where it remains until it is verified and commanded to be transferred into the operating memory. Verification of the received pattern is initiated by command and accomplished via the telemetry link. The receipt of a verify command causes the telemetry encoder to be placed in an interrupt mode, in which it serially reads out the buffer memory content. Update and verify operations are accomplished through the T&C interface, where the necessary serial-to-parallel and parallel-to-serial conversions required for reading and storing update patterns, are made.

In normal operation, a word read from the operating memory is written back into the memory. To transfer buffer memory content into the operating memory, the corresponding buffer memory location is written into the operating memory as it is read out. Since each memory location is read out every frame, the transfer is accomplished in a single frame period and is achieved without interrupting traffic flow. To verify operating memory content, each word read from memory is written simultaneously into the operating and buffer memories. At the end of a frame period, the buffer memory has been loaded and is ready for its contents to be read out via telemetry.

References

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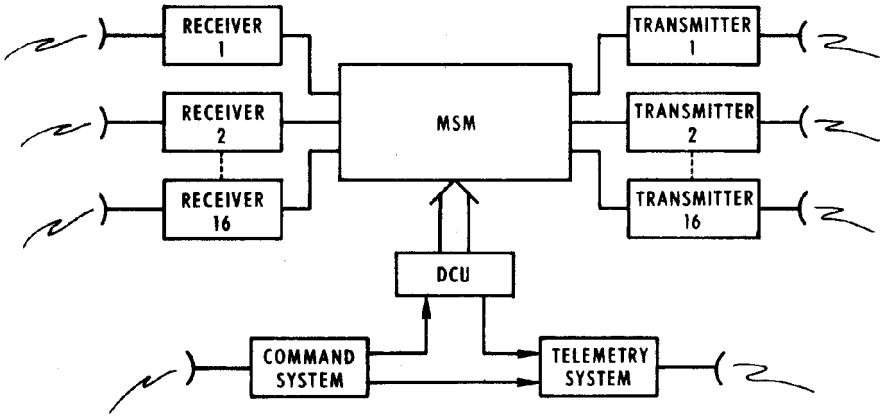

Fig. 1 - Onboard Distribution System Block Diagram

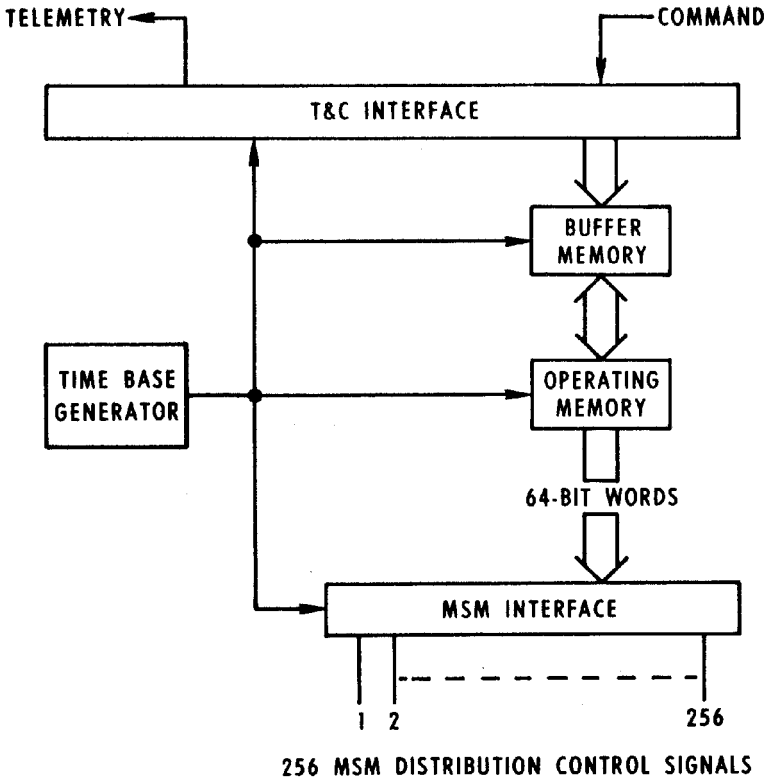

Fig. 2 - DCU Block Diagram

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