

AN ALL DIGITAL PHASE LOCKED LOOP

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Summary An All Digital Phase Locked Loop for FM Demodulation is presented. The system operates synchronously and performs all required digital calculations within one sampling period, thereby performing as a real time special purpose computer. The signal to noise ratio is computed for frequency offsets and sinusoidal modulation and experimental results verify the theoretical calculations.

Introduction At the present time, digital phase locked loops are being employed only for carrier phase tracking of received signals, thus generating a signal suitable for synchronous demodulation. When used for FM demodulation, phase locked loops employ analog circuitry in the construction. However, analog implementation has the following disadvantages:

1. Since the voltage controlled oscillator (VCO) present in all phase locked loops must change frequency in response to a phase input, the circuit becomes an integrator. Analog integrators are always “leaky”, i.e., do not respond to a DC input in a linear fashion.
2. The phase detector and amplifiers insert inaccuracies and spurious poles in the closed loop system. The inaccuracies are due to the multiplication that is needed in phase detection. Also, analog multipliers are extremely sensitive to DC drift or any offset erroneously appearing on the multiplier inputs.
3. The saturation of components in the phase locked loop is extremely common when the input carrier-to-noise ratio is low enough so that noise spikes appear. When this type of input is present, the loop must tolerate the condition where the signal “rides” on the noise rather than the noise on the signal. If the VCO saturates due to a noise spike, all previous information stored during the integration procedure is lost. Therefore, when the spike is no longer present, the loop reverts to a transient state where signal acquisition begins as if there was an inception of system power.
4. When an attempt is made to augment an analog loop to a higher order system, stray capacitance inserts additional poles and the system has a tendency to become unstable when noise is present.

To avoid these problems, the phase locked loop described in this paper is designed with all digital circuitry. Along with digital adders, multipliers, scalers and filters, a digital voltage controlled oscillator algorithm is also designed. The problems mentioned above are eliminated; however, new phenomena common to digital system become apparent. These include roundoff and overflow errors taking the form of quantization noise.

Digital VCO Algorithm

If the VCO in the phase locked loop is an analog type oscillator, its output can be described as

$$v(t) = B \sin \left[\omega_o t + G_v \int_0^t v_{in}(\tau) d\tau \right] \quad (1)$$

where

$$\begin{aligned} v_{in}(\tau) &= \text{VCO input} \\ G_v &= \text{VCO gain} \\ \omega_o &= \text{carrier frequency} \end{aligned}$$

After sampling and replacing the integration by summation (1) becomes the expression for the VCO output at the k^{th} sampling instant:

$$v(kT) = B \sin \left[\pi k/2 + G_v \sum_{n=0}^k v_{in}(nT) \right] \quad (2)$$

If a sinusoidal VCO waveform were used, a binary multiplication of input and VCO voltages would be necessary. This computation is longer than the sampling period and hence the loop could not operate in real-time. The multiplication can be avoided by using a square wave VCO waveform:

$$v(kT) = \text{Sq} \left[\pi k/2 + G_v \sum_{n=0}^k v_{in}(nT) \right] \quad (3)$$

where

$$\text{Sq}(x) = \begin{cases} +1, & 0 \leq x < \pi \\ -1, & \pi \leq x < 2\pi \end{cases}$$

and

$$\text{Sq}(x) = \text{Sq}(x + 2\pi)$$

Now the multiplication is by ± 1 ; i.e., either the input signal passes unchanged or the input signal is inverted, a process easily accomplished using a bank of “exclusive or” gates.

The computation of $S_q(x)$ is accomplished by dividing the binary scale into intervals of length π . Then by examining one bit of the VCO output word the particular π interval in which the argument of $S_q(x)$ falls is easily determined by the value of that bit (1 or 0). Note that the periodicity of the $S_q(x)$ corresponds to the periodicity of binary numbers. Hence, the VCO integrator never saturates but is allowed to overflow.

The gain of the VCO, G_v , is determined by which bit is selected to determine the π intervals. For example, if +5 volts is encoded as the maximum positive binary number in the ten bit word (111111111), the selection of the second most significant bit to represent a π interval results in a VCO gain of $\pi/2.5$ rad/volts; the selection of the third most significant bit to represent a π interval results in a VCO gain of $\pi/1.25$ rad/volt; etc.

Experimental Results

The Digital Phase Locked Loop described by the block diagram in Fig 1 was constructed with the use of DTL logic elements. The sampling rate was fixed at 50 kHz thereby allowing sufficient time for processing. The implemented system was tested for modulation indexes, β , of 3 and 10 for frequency offsets (DC outputs) and sinusoidal modulation.

Response to Frequency Offsets

In the steady state, the Digital Phase Locked Loop tracks any frequency input that will produce an error less than $\pi/2$ (greater values yield instability). Therefore, frequency offsets of up to 675 Hz (instead of 300 Hz as for sinewave modulation) were used in the experimentation.

The loop was tested with $\beta = 3$ and $\beta = 10$ for a frequency offset and the following fixed parameters:

$S = 10^{-2}$ volts	$T = 20 \times 10^{-6}$ seconds
$G_v = \pi/2.5$ rad/volt	$B_{IF} = 2(\beta + 1) f_M$
$1/2^n, + 1/16$	$S_i = 2$ (Volts) ²
$\Delta f = 675$ Hz	$f_M = 67.5$ Hz, 225 Hz

The output signal-to-noise ratio versus carrier to noise ratio is plotted along with the theoretical results in Fig 2. Note the high correlation between the theoretical and experimental curves. As expected, at higher carrier-to-noise ratios the output signal-to-noise ratio approaches a constant, since the quantization noise dominates. Note at very high input carrier-to-noise ratios, the experimental results show a higher output signal-to-noise ratio than the theoretical prediction. This phenomenon is caused by the deterministic

nature of the input signal. The development of quantization noise performance assumed a random input which is the case when noise is added to a signal. However, in the absence (or near absence) of input noise, the output signal-to-noise ratio will be governed by the system noise.

The PLL is usually tested using either sinusoidal modulation or a fixed frequency offset. Since the system is quantized, a slowly varying sinusoid (the frequency of the sinusoid is typically much less than the bandwidth of the loop) will dwell on the same quantization level for many sampling periods. Therefore, the use of an input frequency offset simulates the sinusoidal signal. Furthermore, a frequency offset simulates an M-ary FSK system.

Response to Sinusoidal Modulation

When the FM carrier is modulated with a sinusoid, the output signal-to-noise ratio obeys the same formula for a frequency offset except that the deviation, Δf , becomes the rms deviation, $\Delta f/\sqrt{2}$.

The output signal-to-noise ratio of the loop is shown in Fig 3. As is seen, close correlation exists between the analytical and experimental results. Again, at very high carrier-to-noise ratios, the output signal-to-noise ratio is dominated by system noise as for frequency offsets.

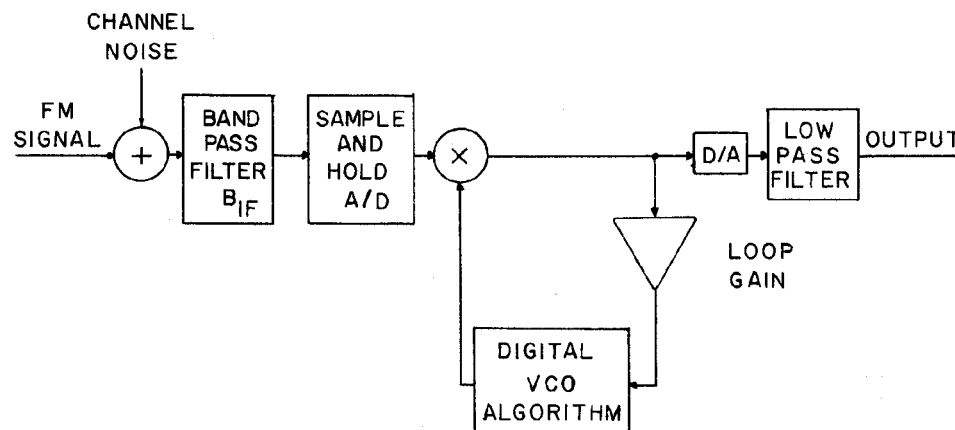


Fig 1 Block Diagram of the First Order Digital Phase Locked Loop

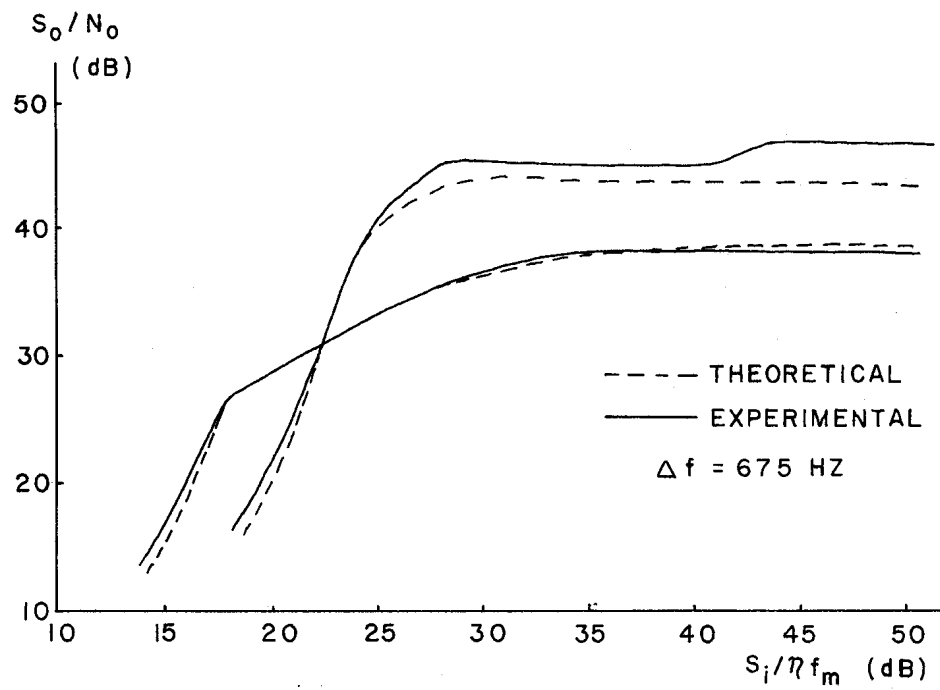


Fig 2 Digital Phase Locked Loop Response to a Frequency Offset

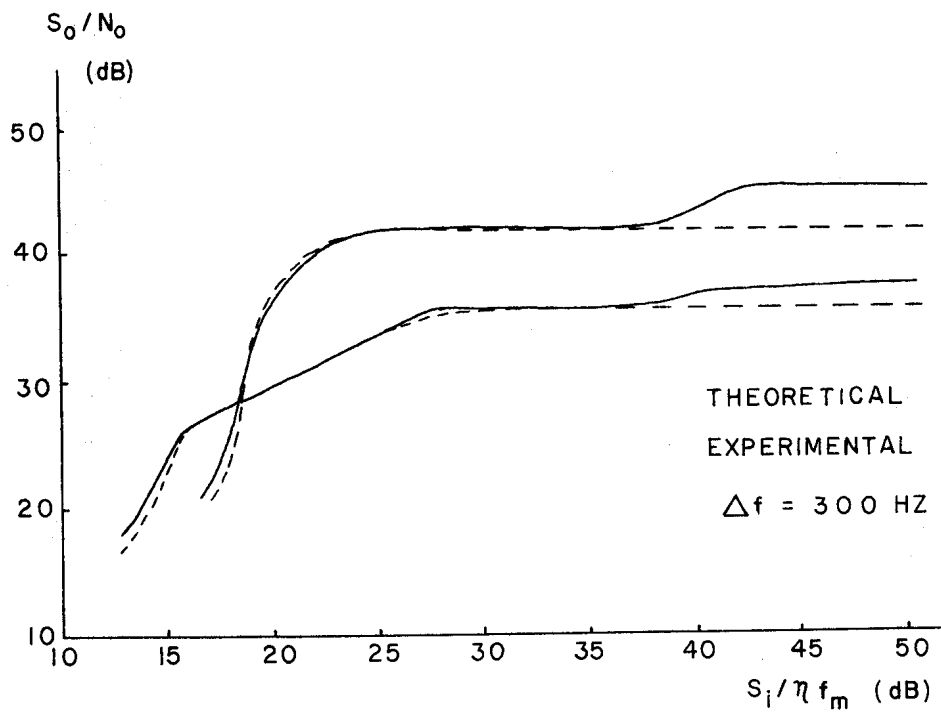


Fig 3 Digital Phase Locked Loop Response to Sinusoidal Modulation