ALL-DIGITAL COHERENT DEMODULATOR TECHNIQUES

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Summary This paper discusses all-digital techniques for receiving and coherently detecting moderate data rate (less than 1 Mbps) PSK signals in real time. A receiver employing synchronous bandpass sampling and A/D conversion of the IF signal is described. Sampler synchronization, bit synchronization, and data detection are performed by a special-purpose digital processor. Analytical methods are developed for predicting receiver performance, and experimental data is presented to indicate the degree of agreement that one might expect.

Introduction The rapid advances in applying MSI and LSI techniques to digital integrated circuits are making it feasible to use digital processing techniques in signal processing areas which have been restricted previously to analog circuitry.

The use of digital circuitry (where technologically and economically practical) has many inherent advantages; including ease of fabrication, a minimum of adjustments, absence of drift, increased reliability, etc.

The purpose of the effort reported in this paper was to develop techniques for coherent demodulation of biphase PSK (BPSK) signals using real-time digital processing. The major goals were to:

- sample and A/D convert directly at the IF frequency
- provide all-digital carrier tracking, bit synchronization, and matched-filter detection
- operate at data rates high enough to be useful for voice communications ($R_d \geq 2400$ bps)
- keep complexity to a minimum

Block diagrams of the conventional analog receiver and the digital receiver are shown in Figure 1.

The analog Costas loop ordinarily used for carrier recovery is functionally replaced by a digitally phase-locked synchronous sampler. The bit synchronizer and the data detection filter are implemented as digital processing algorithms.

Coherent demodulation was achieved by developing a synchronous sampler and an A/D converter which are digitally phase locked in a manner similar to the Costas loop. The "heart" of the phase-locked loop (PLL) is a programmable digital number controlled oscillator (NCO, implemented by loading a high-speed counter with a variable count. The result is a practical coherent demodulator for IF frequencies of a few megahertz.

A rather sophisticated bit synchronizing algorithm employing a phase-locked in-phase and mid-phase integration was chosen for implementation. The algorithm lends itself to digital implementation, provides near-optimum operation at low E/N_o ratios, and is much less sensitive to data transition patterns than most synchronizers.

An experimental receiver operating at 19.2 kbps was constructed and is described below. Results were very satisfactory, and it appears that the techniques discussed are practical for data rates up to 1 Mbps.

While the discussion presented below deals specifically with digital demodulation of PSK signals, it should be kept in mind that the ideas and analysis techniques generally are applicable to other types of modulation.

Digital I-Q Carrier Reconstruction The first step in coherent detection of a BPSK signal is to generate a phase-coherent reference carrier, thus enabling translation of the data modulation to baseband. This function may be performed by using the digital equivalent of the analog inphase-quadrature (I/Q) phase-locked loop (or Costas loop) as shown in Figure 2.

Operation may be described rather briefly as follows. Let the input be a sinusoid of the form

$$v_i(t) = Ad(t) \sin(\omega_i t + \theta_i) \tag{1}$$

where

A = signal amplitude
$d(t) = \pm 1$ is the data stream
ω_i = carrier frequency in rad/sec
θ_i = input carrier phase

When the loop is in lock, the I-Channel is sampled in-phase with the IF signal at intervals of some multiple of 2π radians. The sampled output is of the form

$$v_2(t_k) = Ad(t_k) \sin [\phi_\epsilon(k)]$$

where $\phi_\epsilon(k)$ is the sampler phase error at time t_k. Similarly, the Q-Channel is sampled $\pi/2$ radians later and produces a sampled output of the form

$$v_3\left[t_k + \frac{\tau_i}{4}\right] = Ad\left[t_k + \frac{\tau_i}{4}\right] \cos [\phi_\epsilon(k)]$$

The above samples are multiplied together to form the loop error signal

$$v_4(k) = \frac{A^2}{4} \; d(t_k) \; d\left[t_k + \frac{\tau_i}{4}\right] \sin [2\phi_\epsilon(k)]$$

The IF frequency is chosen to be considerably higher than the data rate ($R_d = 1/T_d$) so that $\tau_i << T_d$ and d(tk) = d[t_k + (τ_i/4] almost all of the time. Thus,

$$v_4(k) = \frac{A^2}{2} \sin [2\phi_\epsilon(k)] \qquad (2)$$

i.e., the loop error signal is just the sampled form of the loop error signal in an analog loop.

The error signal is passed through a digital loop filter, the output of which adjusts the NCO frequency so that the phase error is reduced.

NCO The use of IF sampling pulses rather than sinusoids has a significant impact on the generation of the carrier reference. Ordinarily, a sinusoidal reference requires a rather complicated digital NCO. However, an NCO for generating timing marks may be implemented rather simply by modifying the basic programmable divide-by-N circuit of Figure 3.

A suitable NCO is shown in Figure 4. Operation is as follows. The counter is preset to count N and counts down to zero. This approach is used (as opposed to an “up-counter”) because the delay in recognizing the zero state is constant for any count. The zero state generates the I pulse. The Q pulse is generated p counts later and the counter is reset to N for the beginning of the next period. Note that this NCO configuration has an inherent stability equal to that of the input clock.

Detailed Operation The loop equations will now be derived in order that performance may be predicted. Let the I-Channel sample times be expressed as

$$t_k = k \; N_1 \; T_c + \Delta T_k$$

where T_c = clock period and $\omega_i N_1 T_c = 2\pi$.

and $\omega_i N_1 T_c = 2\pi$

The Q-Channel sample times are $t_k + pT_c$ where $\omega_i\, p\, T_c = \pi/2$. Thus, for the input of Eq. (1),

$$\begin{aligned} v_2(k) &= Ad(t_k)\cos\left[k\omega_i N_1 T_c + \omega_i \Delta T_k + \theta_i(t_k)\right] \\ &= Ad(t_k)\cos\left[\omega_i \Delta T_k + \theta_i(t_k)\right] \end{aligned} \tag{3}$$

and

$$\begin{aligned} v_3(k) &= Ad(t_k + pT_c)\cos\left[\omega_i \Delta T_k + \omega_i pT_c + \theta_i(t_k)\right] \\ &= Ad(t_k + pT_c)\sin\left[\omega_i \Delta T_k + \theta_i(t_k)\right] \end{aligned} \tag{4}$$

Multiplying the above samples together and assuming that $d(t_k) = d(t_k + pT_c)$ gives

$$v_4(k) = \frac{A^2}{2}\sin 2\phi_\epsilon \tag{5}$$

where

$$\phi_\epsilon = \omega_i \Delta T_k + \theta_i(t_k)$$

The sample, $v_4(k)$, is processed by the loop filter, F(z), to form $N_\epsilon(k)$. Thus, the NCO output phase may be expressed as

$$\omega_i \Delta T_k = \omega_i \Delta T_{k-1} + N_\epsilon(k-1)\, T_c \omega_i \tag{6}$$

Equations (5) and (6), in conjunction with the block diagram of Figure 2, lead to the baseband model of the loop shown in Figure 5.

The similarity between the model of Figure 5 and the model for the conventional analog loop [Ref. 1] is rather striking. Note that the digital NCO appears in the baseband model as a digital integrator, just as the VCO appears as an analog integrator in the baseband model of the analog loop.

The digital carrier tracking loop performance is different from the analog loop primarily because of

(1) sampling,
(2) quantization, and
(3) round-off.

Sampling causes the loop baseband response to be periodic (as is true of all digital filters) as shown in Figure 6. Thus, it may be inferred that the sampling rate should be greater than the one-sided IF bandwidth plus any carrier frequency uncertainty in order to avoid degradation in the noise performance (the sampling rate must of course, be considerably high than B_L, but this condition is usually implied by the other considerations). The digital

bit synchronizer and the data filter also impose conditions on the minimum sampling rate. These conditions will be discussed later. Note that the sampling rate is a subharmonic of the input frequency; i.e., samples are spaced some integral number of periods of the input sinusiod. The sampling rate, as a result, is not strictly fixed; however, variations will be small for most applications and can be considered constant.

The usual concept of PLL noise bandwidth may be applied to the digital loop, given that the above sampling rate requirements are met and the quantization effects are neglected for the moment, by considering that $z \approx 1 + ST$ for $|ST| << 1$ and, thus, transforming the baseband model from the z-plane to the s-plane (and linearizing) as shown in Figure 7, where K_g is the gain constant of the A/D converter (quantizer) and T_s is the sampling period.

Amplitude quantization is not particularly critical to loop operation (although several bits may be required for efficient data recovery). The effects of one-bit quantization on PLL operation are discussed on Ref. 2. Typical degradation in loop SNR are shown to be less than 1 db.

Frequency quantization is an important consideration in the design of the digital loop; especially since this quantity can be the limiting factor in the performance of a practical implementation. Frequency quantization arises because the NCO as shown in Figure 8 only operates at discrete frequencies. The loop tracks the input signal of frequency f_i by switching between frequencies f_0 and f_1 such that the average frequency of operation is f_i. Between samples, the phase error changes in a linear manner at a ratel proportional to the difference between the input frequency and the NCO frequency. Since the loop averages two frequencies, one of which could be q_f Hertz from the input frequency, a phase change of

$$\Delta\phi = 2\pi q_f T_s$$

can occur between samples., The quantization increment, q_f, can be expressed as

$$q_f \approx \frac{f_0}{N_1} = \frac{f_0 T_c}{T_s} \tag{7}$$

where f_0 is the NCO center frequency. The phase error which may occur due to frequency quantization is, thus,

$$q_f \approx \frac{f_0}{N_1} = \frac{f_0 T_c}{T_s} \tag{8}$$

which suggests that

$$\Delta\phi = 2\pi f_0 T_c \tag{9}$$

for small tracking errors ($\Delta\phi \leq 7$ deg.).

The above condition, while necessary, does not guarantee proper loop operation. For example, a frequency step of $\Delta f = 0.5\ B_L$ will cause a phase error of about 40 deg. in a second-order analog loop with g = 0.707, while a step of $\Delta f \approx B_L$ will cause the loop to slip cycles [Ref. 1]. Thus, it would seem wise to choose the NCO quantization increment to satisfy

$$q_f < 0.5\ B_L \tag{10}$$

to inusre the desired operation. This condition is intuitively satisfying when one thinks of the loop as a narrowband tracking filter centered around the VCO operating frequency. Coarse frequency quantization will lead to an effective B_L larger than that predicted by the linear model, and to poor phase tracking.

Bit Synchronization Bit synchronization in the all-digital receiver implies the grouping together of all samples from a single data bit for processing by the digital data filter. The synchronizer algorithm performs operations equivalent to the near-optimum synchronizer described in Refs. 2, 3 and 4. A functional block diagram of the synchronizer is shown in Figure 9. Briefly, its operation is as follows. When the loop is near lock, the in-phase integrator and SGN(x) operation perform matched-filter data detection. The mid-phase integrator performs an integration over some interval less than one bit and is centered on the data transition; thus, it generates a number proportional to the phase error. The detected data stream is routed to a logic box that compares successive bits to determine if a data transition occurred, and, if so, whether it was positive or negative. The phase error signal generated by the mid-phase integrator is multiplied by +1, -1, or 0, depending on the nature of the transition as determined from the detected data stream. The multiplier output is processed by the loop filter and is used to control the NCO.

Phase Detector In the digital synchronizer, the in-phase (IP) and mid-phase NP integrators are approximated as fummations; for example,

$$\int_0^T \chi(t)\ dt = \sum_{k=0}^{K} \chi(t_k)$$

where K is the number of samples per bit.

This, along with the resulting phase detector characteristics, is illustrated in Figure 10. The phase detector accepts data with random transition patterns. The staircase phase detector characteristics, as shown in Figure 10(b), assumes a data waveform. (of amplitude A) with zero rise time. In practice, the bandlimited input signal results in a nearly smooth characteristic.

The same type of NCO is used for the bit synchronizer as was discussed in connection with the carrier tracking loop.

Baseband Model A baseband model for the bit synchronizer may be derived in the same manner as discussed for the carrier tracking loop. The result is shown in Figure 11 and is seen to be very similar to the model of Figure 5.

The baseband model may be transformed from the "z-plane" to the "s-plane" when $\omega_L << 1/T$, as shown in Figure 12, where

K = number of samples per bit
T = data bit period
T_c = clock period
λ = normalized timing error

and $g(\lambda) \approx AT$, $S_n(f) \approx N_o T/4$, when the input data transitions are random with probability 1/2.

The bit synchronizer performance is analyzed extensively in Refs, 2, 3, and 4 using the model of Figure 12.

Loop Bandwidth Actual loop bandwidths differ from those calculated using the linearized continuous models of Figures 7 and 12 due to

1) delay in the loop
2) difference in amplitude response between analog and digital loops

the one-sided loop bandwidth of the digital loop may be defined as

$$\overline{B}_L = \frac{\frac{1}{2\pi T}\int_0^{\pi} |L(e^{t\omega T})|^2 \, d\omega T}{|L(o)|^2}$$

where T is the loop sample time. The increase in loop bandwidth of a second-order digital loop over that of a second-order analog loop with no delay was calculated with the assistance of a digital computer. The results are presented in Figure 13 for a loop with delay of m samples and a design damping factor of $\xi = .707$. Note that in the case of the bit synchronizer T is the data bit period, while in the case of the carrier tracking loop, T is the input sampling rate.

The loop bandwidth of the loop with a one-sample delay (m=1) increases significantly over that of the design reference for $B_L T > 0.1$ and the loop becomes unstable for $B_L T = 0.75$.

The condition for loop stability when m = 1 (as in Figures 5 and 11) may be shown to be

$$B_L T < \frac{4\xi^2 + 1}{4} \quad \text{for } 0 < \xi < 1$$

$$\text{stable} \qquad \text{for } 1 < \xi$$

where ξ is the design damping factor and B_L is the design loop bandwidth based on the continuous loop with no delay.

Data Detection The bit synchronizer in-phase integrator acts as a synchronized integrate-and-dump filter for the input data stream as shown in Figure 14.

The digital filter differs from the analog matched filter in that

(1) the integrator is approximated as a sum.
(2) there is noise fold-over due to the non-rectangular IF filter, and
(3) the filter input is quantized.

Approximating the integrate-and-dump filter by a sum-and-dump filter results in a transfer function of the form

$$H_D(z) = \frac{z^K - 1}{z^{K-1}(z-1)} \tag{11}$$

with amplitude response

$$|H_D(j\omega)| = \left| \frac{\sin \frac{\omega T}{2}}{\sin \frac{\omega T}{2N}} \right| \tag{12}$$

as compared with the analog filter response

$$|H_A(j\omega)| = \left| T \frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \right| \tag{13}$$

The degradation in filter output SNR due to both the mismatched filter function and the noise “fole-over” caused by sampling is computed in Ref. 5 for a first-order IF filter. The results are shown in Figure 15 with IF bandwidth as a parameter. A similar result for a

rectangular IF filter may be derived as follows. Consider the sampling to be done at baseband as shown In Figure 16 where $H_p(j\omega)$ is a rectangular low-pass filter and $H_D(j\omega)$ is the digital integrate-and-dump filter. The output voltage may be expressed as

$$V_o(T) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F\{Ad(t)\}\, H_p(j\omega)\, H_D(j\omega)\, e^{j\omega T}\, d\omega$$

where F{Ad(t)} denotes the Fourier transform of the input.

The output due to a single input bit is (intersymbol interference is neglected):

$$V_o(T) = \frac{2A}{\pi} \int_{0}^{\pi BT} \frac{\cos x/k \sin^2 x}{x \sin x/k}\, dx$$

The output power due to noise may be computed using the relationship

$$\sigma_n^2 = \frac{1}{2\pi} \int_{-\infty}^{\infty} s_n(f)\, |H_p(j\omega)\, H_D(j\omega)|^2\, d\omega$$

and so

$$\sigma_n^2 = \frac{N_o 2}{\pi T} \int_{0}^{\pi BT} \frac{\sin^2 x}{\sin^2 x/k}\, dx$$

giving a detection filter output SNR_o of

$$SNR_o = \frac{V_o^2(T)}{\sigma_n^2} = \frac{2A^2T \left[\int_{0}^{\pi BT} \frac{\cos x/k \sin^2 x}{x \sin x/k}\, dx \right]}{\pi N_o \int_{0}^{\pi BT} \frac{\sin^2 x}{\sin^2 x/k} dx}$$

Degradation from ideal may be expressed as

$$\Gamma = \frac{SNR_o \text{ (digital)}}{A^2 T/N_o}$$

This quantity is plotted in Figure 15 with $2\pi BT = \omega_{LP}T$ as parameter.

One may conclude that most receivers will require something over five samples/bit for efficient detection.

As estimate of the effects of amplitude quantization can be derived from the work of Ref. 6. Four bits of quantization is adequate to hold degradation in probability of error to a few tenths of a db.

Experimental Receiver An all-digital receiver was implemented at Philco-Ford to demonstrate the techniques discussed above. A data rate of 19.2 kbps was chosen for the experimental unit. Receiver parameters are summarized in Table I.

Table 1. Summary of Receiver Parameters

R_D	= 19.2 kbps
f_i	= 1.92 NHz
$1/T_s$	= 84 x 10^3 samples/sec
$1/T_c$	= 2.16 MHz
K	= 20 samples/bit

The input signal (1.92 MHz) is sampled at a rate of 384 x 10^3 samples/sec; i.e., every fifth cycle. Each sample is quantized to 5 bits; although, only 4 bits are used in the carrier tracking loop. The carrier loop frequency and phase quantization increments are, respectivelu, q_f = 8 kHz and $\Delta\phi$ = 7.5 deg. The second-order carrier tracking loop was designed with B_L = 15 kHz. The bit synchronizer receives 20 samples/bit, each quantized to 5 bits. The NCO clock frequency is 300 x R_D = 5.76 MHz. The frequency and timing quantization increments are, thus, q_f = 64 Hz and $\Delta T/T$ = 0.33%, respectively. The mid-phase integrator sums 8 samples. A first-order loop was implemented with a design bandwidth of $B_L \approx$ 800 Hz.

The digital functions were implemented on standard 4 1/4-inch square plug-in cards capable of holding a maximum of 24 integrated circuits. A total of 8 cards was used; one card for the sample-and-hold circuits, one for the A/D converter, and three each for the carrier tracking loop and bit synchronizer. Approximately 130 IC's were used.

A photograph of the digital receiver is shown in Figure 17. The three cards on the right generate test signals and are not part of the receiver.

Test Results Measurements of the carrier tracking loop phase jitter are plotted in Figure 18 and are compared with the theoretical performance of a loop with B_L = 15 kHz. The measured performance is very close to the calculated performance at low ratios of P_s/N_o, but remains constant at $\sigma\phi$ = 14 deg. for high P_s/N_o . The minimum expected phase error due to frequency quantization is computed from Eq. (8) as 7.5 deg. The additional error may be attributed to the loop's difficulty in tracking frequency steps of the magnitude af $\Delta f \approx 0.5\ B_L$.

The bit synchronizer timing jitter is plotted vs E/N_o in Figure 19. Note that, once again, good agreement is obtained at low E/N_o while at high E/N_o the timing jitter becomes nearly constant at about $\sigma\lambda = 4\%$. This value is considerably high than that which can be attributed to quantization effects in the bit synchronizer and would seem to be due largely to the noise introduced into the baseband signal by the carrier tracking loop jitter.

Error rate results are plotted in Figure 20. There is considerable degradation from coherent detection due to the wide carrier tracking loop employed, but little degradation due to the bit synchronizer and data filter.

Conclusions This paper describes techniques suitable for real-time coherent demodulation of PSK signals using a special-purpose digital processor. The feasibility of the digital equivalent PSK receiver has been demonstrated experimentally.

Although the techniques described were developed primarily for future application, the state-of-the-art in integrated circuit speed, variety of functions available, and cost are such that the digital equivalent techniques described are presently competitive with analog circuitry (on a size, weight, and cost basis) for many practical data rates.

The synchronized bandpass sampler is an interesting and useful equivalent to the analog phase-locked demodulator. However, hybrid loops employing analog mixers will,probably be more useful for near-future applications.

The digital bit synchronizer performed well and has inherent desireable characteristics which will make it a candidate for immediate application in some areas. It is very attractive for low- and moderate-bit rates where drift, oscillator instability and component size are a problem.

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References

(1) F. M. Gardner, “Phaselock Techniques”, John Wiley & Sons, Inc. New York, N.Y.; 1966.

(2) W. T. Hund and T. O. Anderson, “Digital transition tracking symbol synchronizer for low SNR coded systems”, International Conference on Communications, Boulder, Colorado, Catalog No. 69C29-COM; June 1969.

(3) M. K. Simon, “An analysis of the steady-state phase noise performance of a digital-data transition tracking loop”, International Conference on Communications, Boulder, Colorado, Catalog No.69C29-COM; June 1969.

(4) W. C. Lindsey and R. C. Tausworthe, “Digital data-transition tracking loops, JPL Space Programs Summary, pp. 37-50, Vol. III; April 1968.

(5) F. D. Natali, “Comparison of analog and digital integrate-and-dump filters”, (Correspondence) Proc. of the IEEE, Vol. 57; October 1969.

(6) Goddard Space Flight Center”, Quarterly progress report, April to June 1966”, Report No. 8 pp. 3-13.

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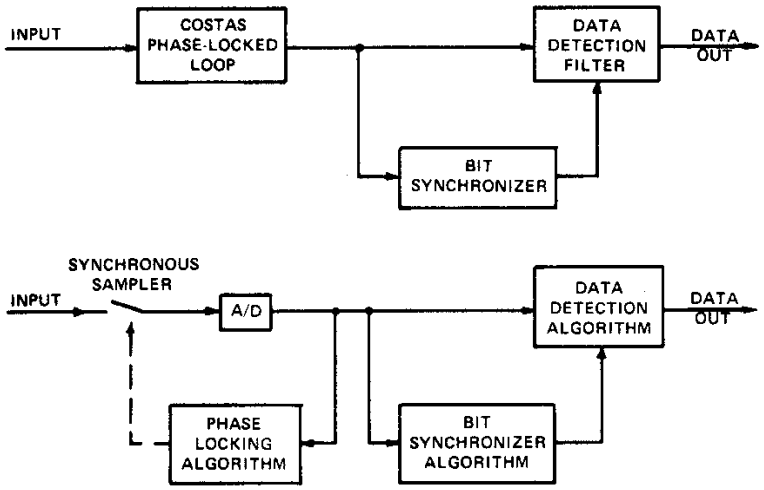
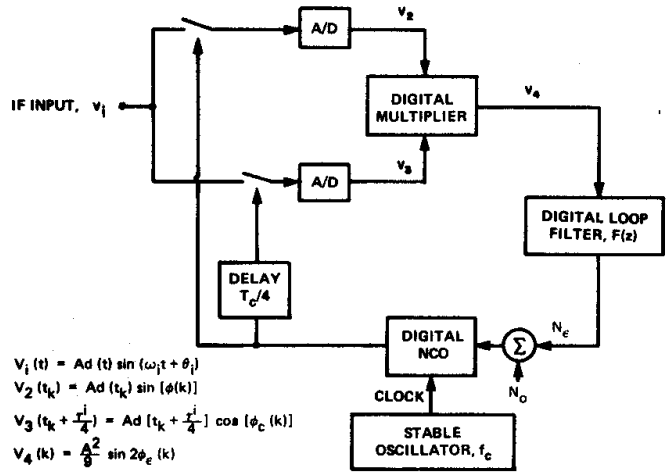
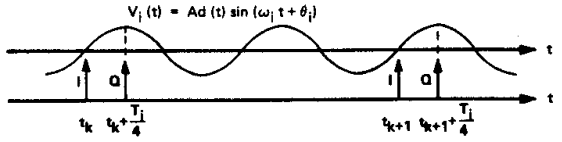


Figure 1 Conventional Analog PSK Receiver and Equivalent Digital Receiver



(a) Block diagram of the digital phase-locked loop



(b) Synchronous sample times

Figure 2 Digital Equivalent of the Costas Loop

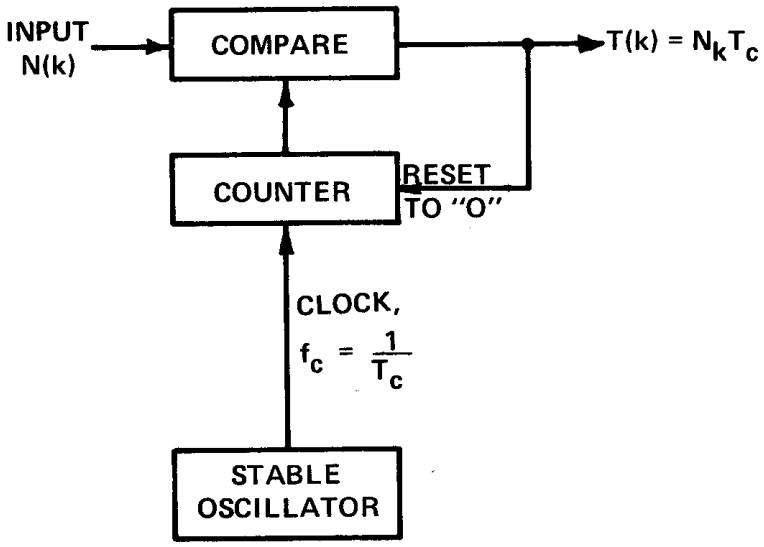


Figure 3 Programmable Divide-by-N Circuit

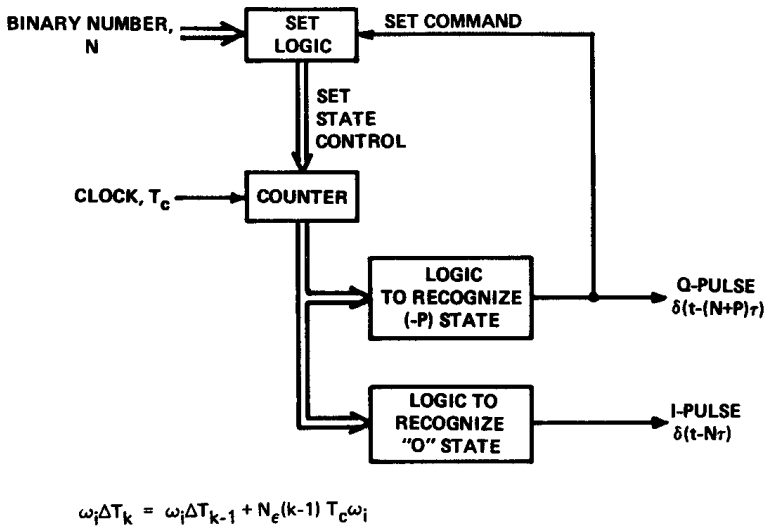


Figure 4 A Practical NCO

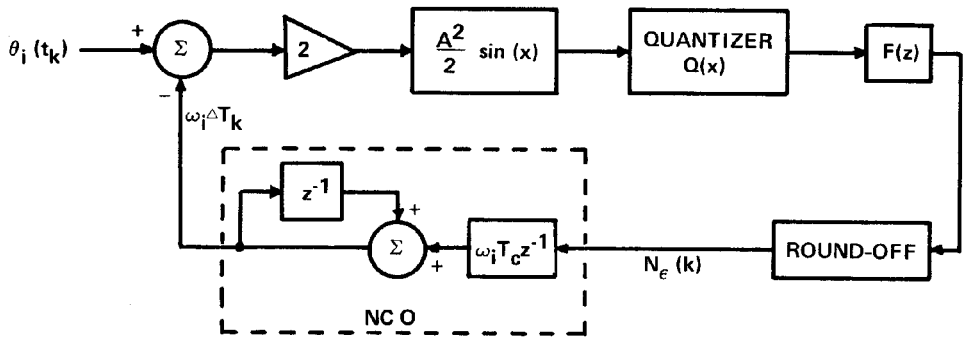


Figure 5 Baseband Model of Digital PLL

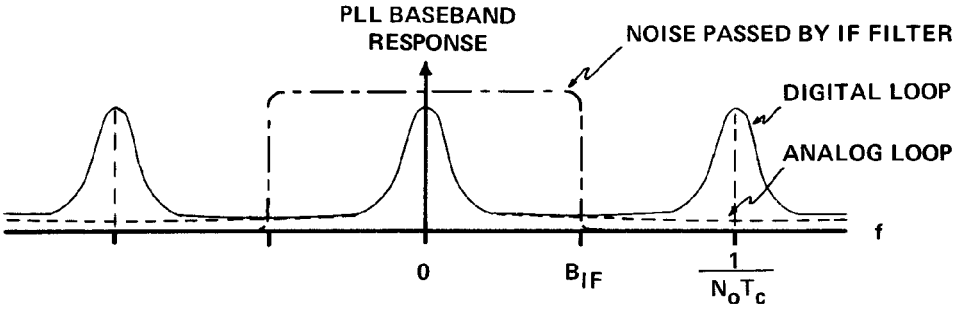


Figure 6 Baseband Response of Analog and Digital PLL's

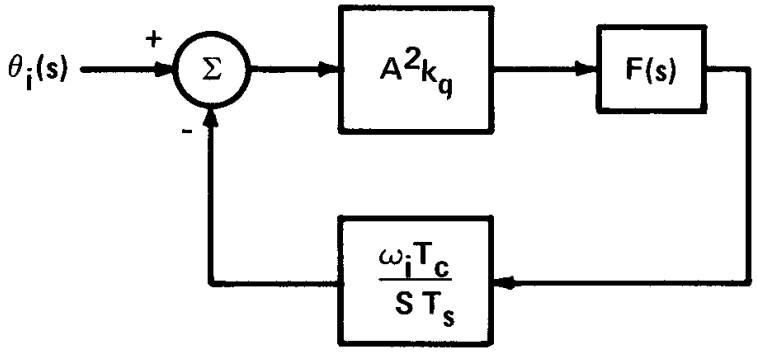
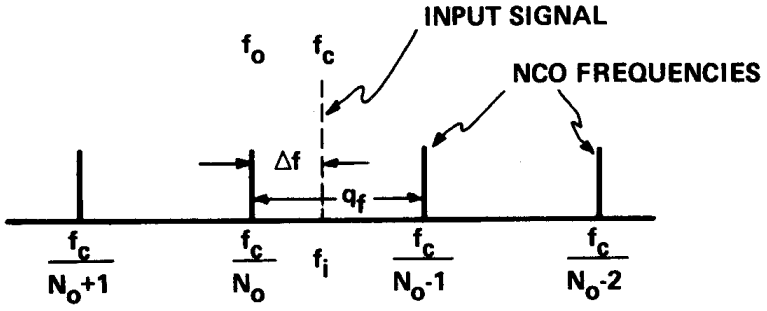


Figure 7 Linearized PLL Baseband Model in the S-Plane



$$q_f \approx \frac{f_o T_c}{T_s}$$

$$\Delta\phi = 2\pi f_o T_c$$

Figure 8 Discrete Frequency operation of the NCO

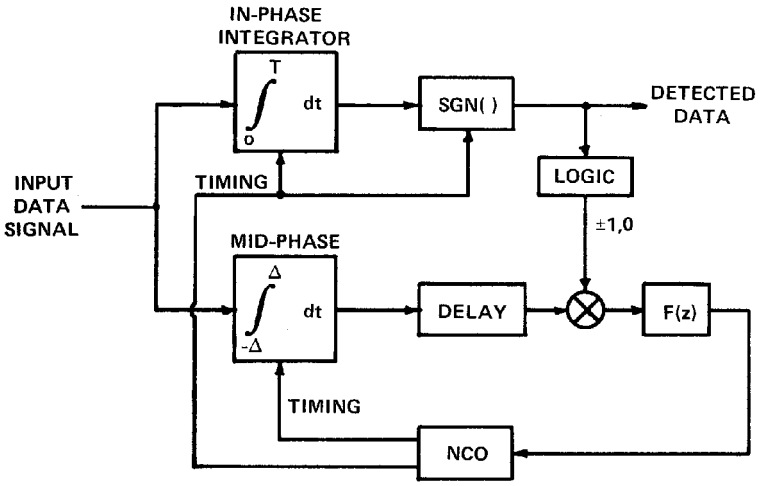
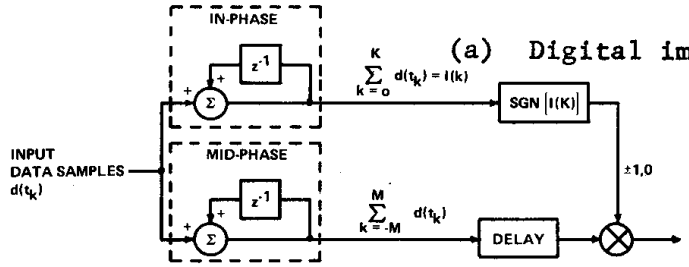
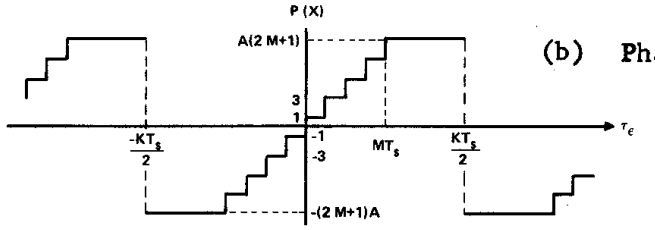


Figure 9 Functional Block Diagram of the Bit Synchronizer



(a) Digital implementation of the phase detector

Figure 10 Bit Synchronizer Phase Detector



(b) Phase detector characteristics

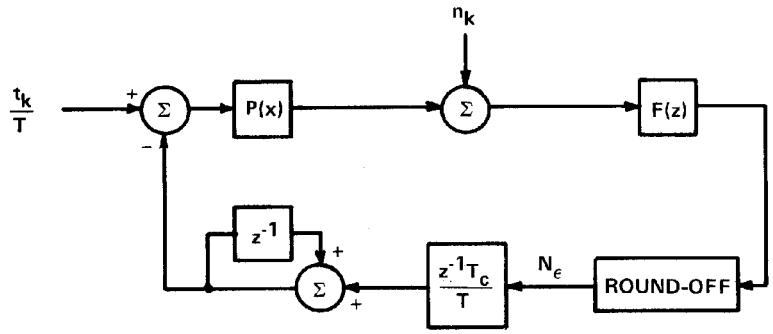


Figure 11 Baseband Model of the Digital Bit Synchronizer

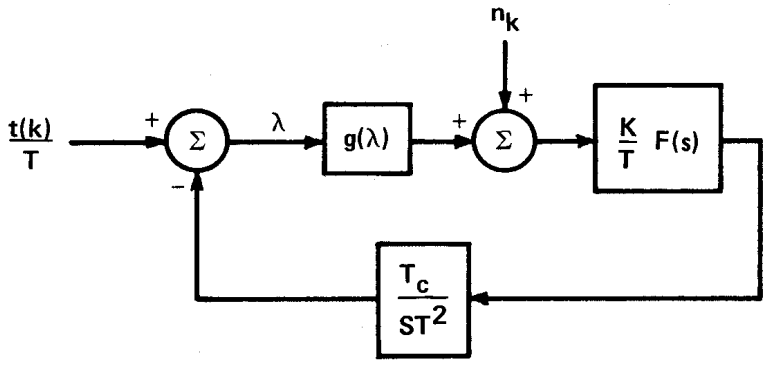


Figure 12 Synchronizer Baseband Model in the "S-Plane"

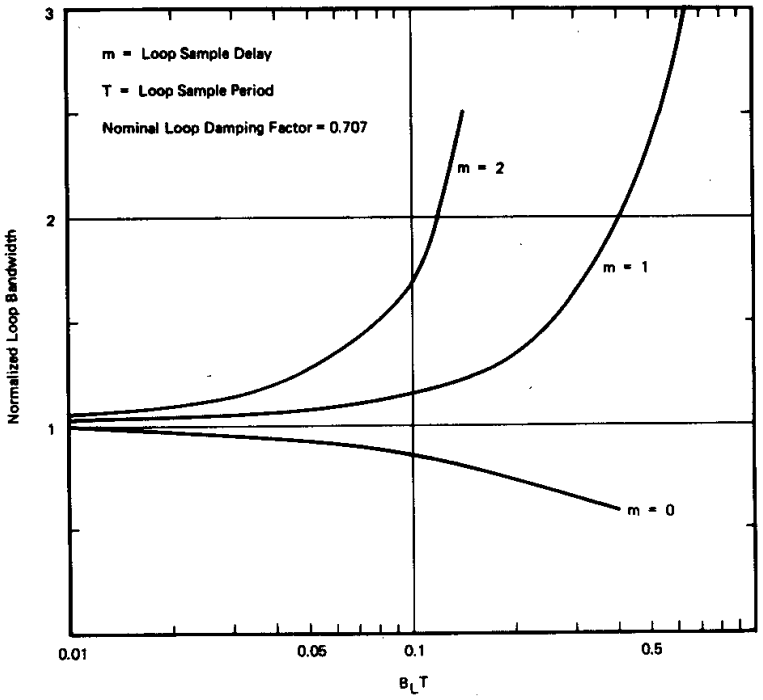


Figure 13 Increase in Digital Phase-Locked Loop Bandwidth over Design Bandwidth as $B_L T$ is Increased

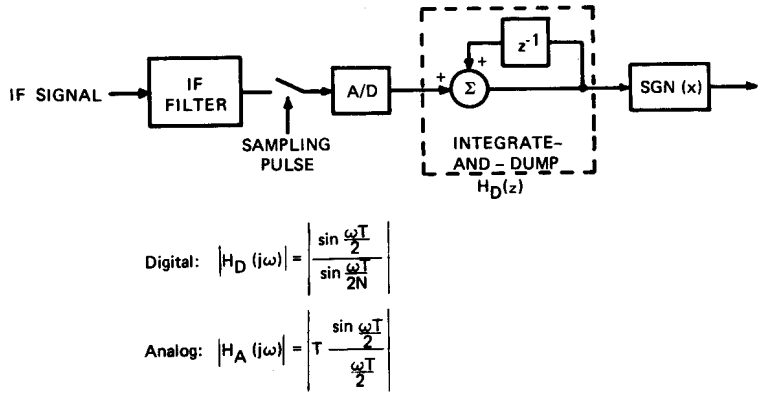


Figure 14 Data Detection Path

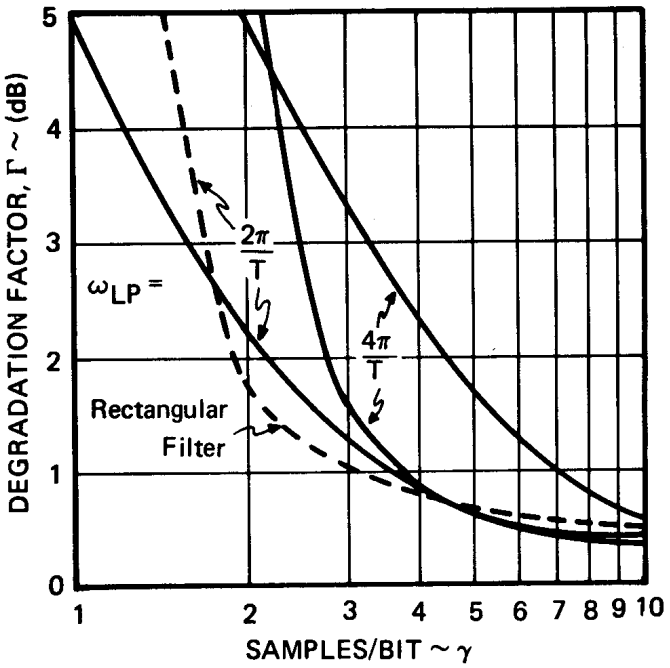


Figure 15 System Degradation Due to Sampling

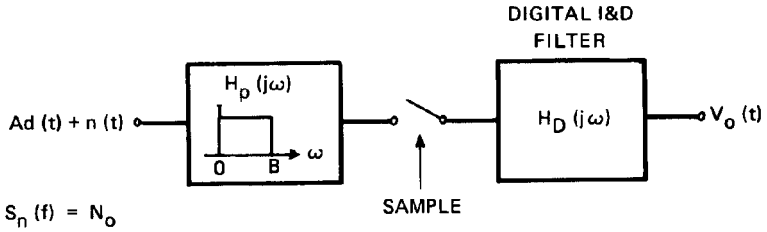


Figure 16 Model of Prefilter and Digital I&D Filter

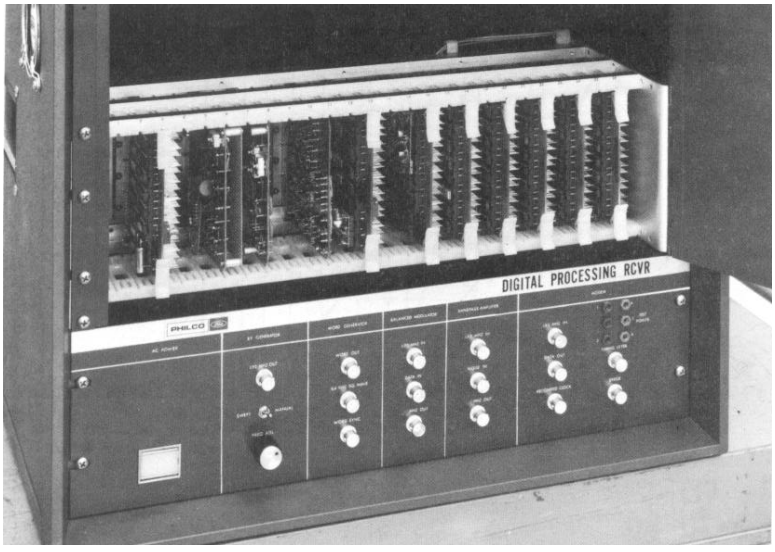


Figure 17 Experimental All-Digital PSK Receiver

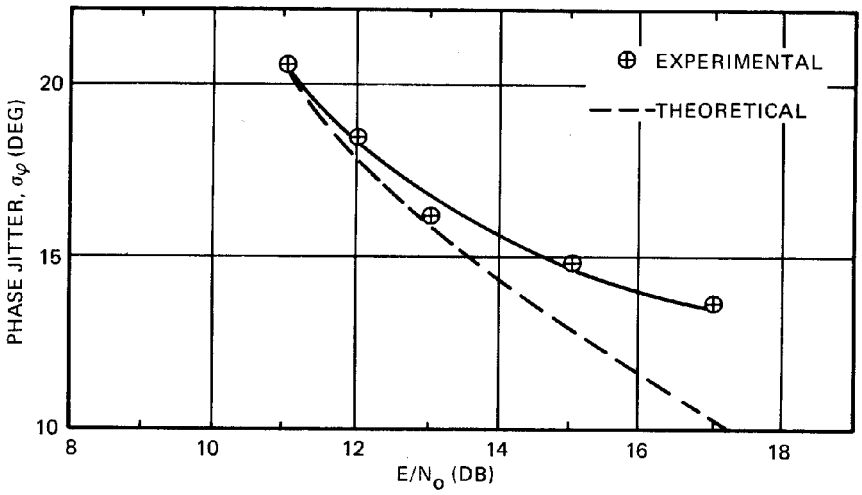


Figure 18 Carrier Tracking Loop Phase Jitter

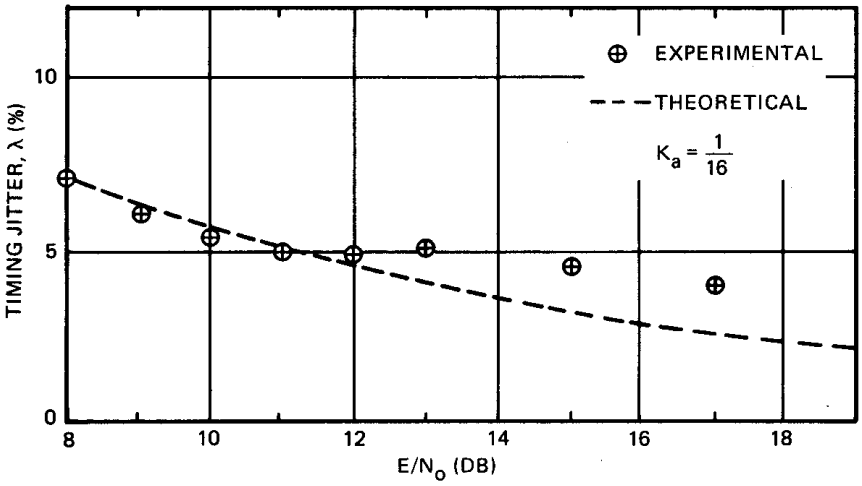


Figure 19 Bit Sync Timing Jitter

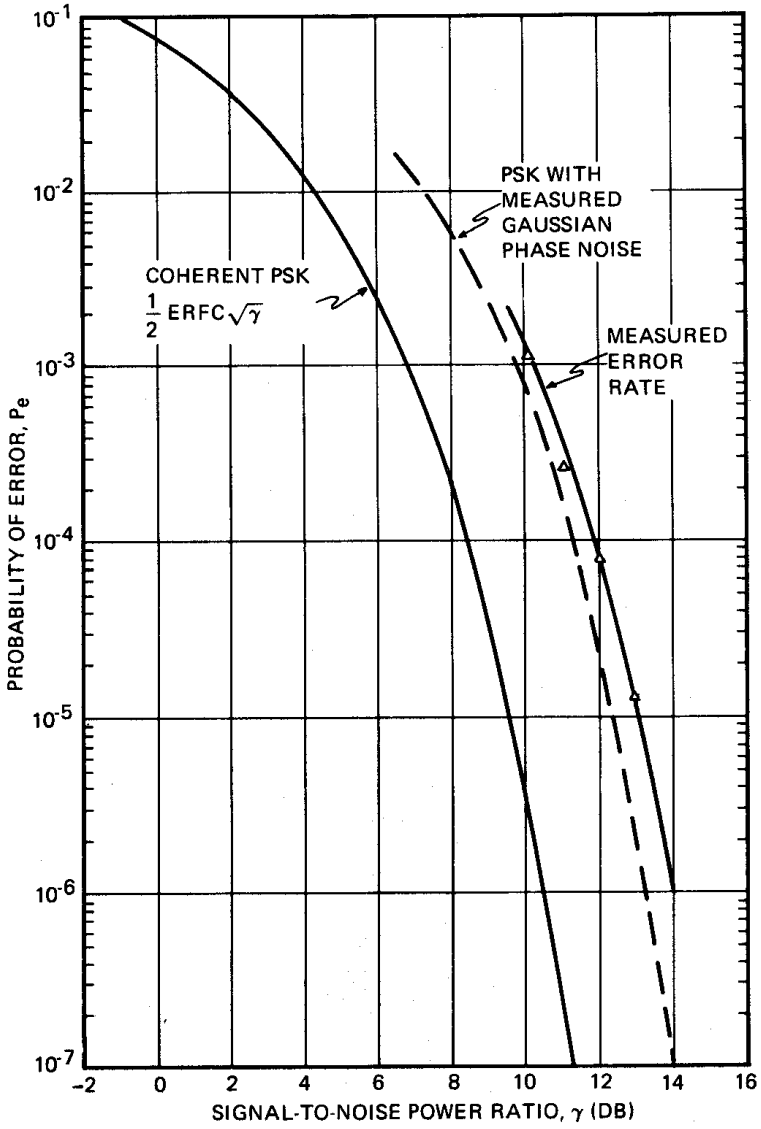


Figure 20 Bit Error Probability Measurement