ON SYNCHRONIZATION TECHNIQUES FOR DIGITAL COMMUNICATIONS SYSTEMS

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Summary This talk considers the transient response and the steady-state behavior of some digital phase-locked loops. When these loops are used to synchronize the transmission rate of digital communication stations, the system is capable of operating in two modes: (1) In master-to-slave mode when the communication stations are connected by digital transmission facilities, and (2) In slave-to-slave mode when these stations are connected by analog transmission facilities.

Introduction When digital communication stations are connected by wholly digital transmission facilities, it is most efficient to slave the clocks at the stations to a master clock in the system. To perform this operation, hereafter referred to as master-to-slave operation,[1] an interface unit at the station extracts timing pulses from the incoming digital data stream. These timing pulses are passed through a phase-locked loop to eliminate noise and jitter. The output of the phase-locked loop controls the signaling rate of the station.

Unfortunately a technical problem arises when data stations are synchronized in the above manner. Before digital systems evolve into a well-connected network, data stations are also often connected by wholly analog transmission facilities. When two data stations equipped to operate in the master-to-slave mode are connected by analog facilities, each station will regard the clock at the other station as the master clock and the two stations will attempt to mutually synchronize each other. This mode of synchronization can be called “slave-to-slave”.[2-8] Conventional phase-locked loops, which perform well in the master-to-slave mode, may not perform well in the slave-to-slave mode, being unusually sensitive to path length delays and other system parameters. Consequently, there is a need for a synchronization scheme capable of operating in both the master-to-slave and the slave-to-slave modes.

We analyze a synchronization system which employs digital rate-locked loops to determine if it can operate successfully in both modes. The phase detector in the rate-locked loop is a multistage counter that counts the difference between the number of zero crossings of the input signals. Because of this nonlinear counting process, the operation of the synchronization system is determined by nonlinear differential-integral equations.

These equations are difficult to analyze. For example, it is difficult to prove rigorously that in the master-to-slave mode the data stations will not add or delete bits from the customer's data stream.

We have examined the transient and steady-state behavior of the digital rate-locked loop to demonstrate that it can operate successfully in both modes. The analyses are too lengthy to be included here, so we shall only describe the mathematical model and present the analytical results. For clarity, master-to-slave mode is considered in Sections II and III, while slave-to-slave mode is considered in Sections IV and V.

Master-to-slave Operation Consider two communication stations as depicted in Fig. 1. Station 1 (with slave clock) represents a data station. Station 2 (with master clock) represents a station in the digital transmission facility. The master clock at station 2 emits a timing signal $\sin \omega_2 t = \sin 2\pi f_2 t$ which controls the transmission of data from station 2 to station 1 (for example station 2 may transmit a digit to station 1 at every 2nd zero crossing of this timing signal).

Station 1 receives data from station 2 and derives from the received data a timing signal $s_2(t) = \sin \omega_2(t - \tau_{12})$, where τ_{12} represents time delay in the transmission path. The signal $s_2(t)$ and the output $s_1(t)$ of a local oscillator are compared in a digital phase detector (Figure 2). The digital phase detector is a counter which counts the zero crossings of $s_2(t)$ and $s_1(t)$ and produces an output proportional to the difference between these two counts. Mathematically, this operation can be specified as follows. Let it be assumed that the digital phase detector is activated at $t = 0$. Let $N_1(t)$ and $N_2(t)$ be, respectively, the number of zero crossings (both upward and downward zero crossings) of $s_1(t)$ and $s_2(t)$ in the time interval 0 to t, then the output of the digital phase detector is

$$u_1(t) = e_1[N_2(t) - N_1(t)]$$

where e_1 is a positive constant $\left[\frac{\text{volts}}{\text{count}}\right]$ and may be called the gain of the counter. As depicted in Figure 2, $u_1(t)$ is passed through a filter and the filter output $v_1(t)$ controls the frequency of a voltage controlled oscillator (VCO_1). Let $\omega_1 = 2\pi f_1$ be the free running radian frequency of VC01, then the output of VCO_1 is

$$s_1(t) = \sin\left[\omega_1 t + a_1 \int_0^t v_1(\tau)d\tau + \theta_1\right]$$

where a_1 is the gain of VCO_1 $\left[\frac{\text{radians}}{\text{voltxsecond}}\right]$. The signal $s_1(t)$ is used to control the transmission of data from station 1 to station 2 (for example station 1 may transmit a digit to station 2 at every 2nd zero crossing of $s_1(t)$).

The zero crossing counting process introduces phase quantization errors. To illustrate this, let us derive an analytical expression for the number of zero crossings of $s_2(t)$ from t = 0 to a particular time instant τ. As illustrated in Figure 3, t' is the time instant at which the last zero crossing prior to t = 0 takes place, and t'' is the time instant at which the last zero crossing prior to $t = \tau$ takes place. It is obvious from Figure 3 that the number of zero crossings in the time interval 0 to τ is

$$N_2(\tau) = \frac{\omega_2 t'' + \theta_2}{\pi}$$

Note that the phase cumulated from t'' to τ does not contribute to the value of $N_2(\tau)$. This residual phase (or phase quantization error) will be designated $\psi_2(\tau)$, that is

$$\psi_2(\tau) = \omega_2 \tau - \omega_2 t''$$

The above two equations hold for all $\tau > 0$; therefore, we can replace their τ by the time variable t and write

$$N_2(t) = \frac{\omega_2 t'' + \theta_2}{\pi}$$

$$\psi_2(t) = \omega_2 t - \omega_2 t''$$

The variation of $\psi_2(t)$ with t is illustrated in Figure 3. Note that $\psi_2(t)$ increases from 0 to π. When $\psi_2(t)$ reaches π radians, a zero crossing takes place, and $\psi_2(t)$ drops to zero and increases from zero again. Clearly

$$0 \leq \psi_2(t) \leq \pi$$

Since $s_2(t)$ is a pure sine wave, $\psi_2(t)$ is a sawtooth wave.

From the above, we have

$$N_2(t) = \frac{\omega_2 t + \theta_2 - \psi_2(t)}{\pi}$$

Similarly, one can write the number of zero crossings of $s_1(t)$ as

$$N_1(t) = \frac{\omega_1 t + a_1 \int_0^t v_1(\tau) d\tau + \theta_1 - \psi_1(t)}{\pi}$$

where $\psi_1(t)$ is the phase quantization error as illustrated in Figure 4. As can be seen

$$0 \leq \psi_1(t) \leq \pi$$

Note that $\psi_1(t)$ is not shown as a sawtooth wave in Figure 4 because $s_1(t)$ is not a pure sine wave in the transient stage after t = 0. The presence of these phase quantization errors greatly complicates the analysis.

Steady-state and Transient Analyses for Master-to-Slave Mode This section summarizes analytical results for the master-to-slave mode. The first problem considered is whether the signaling rate of station 1 can lock to that of station 2 in the presence of phase quantization errors. To attack this problem, we first introduced the concept of equilibrium. The system is said to be in equilibrium if, corresponding to every digit received from station 2, station 1 also transmits a digit back to station 2. We proved the following theorem.

Theorem The system will reach equilibrium if

$$-\pi < L^{-1}\left[\frac{s}{s+F(s)}\,\psi_1(s)\right] < \pi$$

Based on this theorem, we proved that the system will reach equilibrium when the usual RC filter is used in the rate-locked loop. We then demonstrate that when RC filter is used the signaling interval of station 1 will lock to that of station 2 exactly.

Secondly, it is shown that the slave oscillator in the rate-locked loop locks to neither the instantaneous frequency nor the phase of the master oscillator. For this reason, we refer to this control loop as a rate-locked loop, instead of a frequency-locked loop or a phase-locked loop. This difference, while immaterial in synchronization application, should be carefully noted in other applications.

Thirdly, we have determined the transient response of the system, including the effects of the phase quantization errors. It is shown that the signaling rate of station 1 approaches that of station 2 in a monotone fashion. From the transient response, settling time of the slave oscillator can be easily estimated. This settling time can be rather long when the RC filter has a long time constant. For fast start-up purposes, it may be desirable for station 1 to transmit data before the slave oscillator is completely settled. Thus, during the start-up period, data can be transmitted from station 1 to station 2 faster than it can be transmitted out of station 2. Consequently, a buffer storage is required at station 2. We have determined the minimum buffer size requirement (see Table 1). For typical applications, the buffer size is small.

Fourthly, we considered the pull-in range of the digital rate-locked loop. As described in Section II, the digital phase detector is a counter which counts the difference in the number of zero crossings. In order to avoid counter overflow (that is, to ensure pulling in), the

counter must have a certain minimum size. We have determined this minimum size (see Table 1). For typical applications, the counter size is also small.

Finally, we considered alternate ways of implementing the rate-locked loop. Instead of counting both the upward and downward zero crossings of the input signals, the counter may count only one type of zero crossings. Instead of counting the zero crossings of the fundamental frequency, the counter may count the zero crossings of the harmonics. We have determined the minimum buffer and counter size requirements for each of these different implementations. To conserve space, we shall not elaborate on such results here.

Slave-to-slave Operation A mathematical model of slave-to-slave synchronization is depicted in Figure 5. The local oscillator at station 1 (VCO_1 in Figure 5) emits a timing signal $S_{11}(t)$ which controls the transmission of data from station 1 to station 2. (For example, station 1 may transmit a digit to station 2 at every second zero crossing of $S_{11}(t)$.)

Station 2 derives from the received data a timing signal $S_{12}(t)$ and compare $S_{12}(t)$ with its local oscillator output $S_{22}(t)$ at the digital phase detector. The digital phase detector is a counter which counts the zero crossings of $S_{12}(t)$ and $S_{22}(t)$ and produces an error signal $u_2(t)$ proportional to the difference between these two counts. The error signal $u_2(t)$ is passed through an RC filter $F_2(s)$ to control the frequency of VCO_2. Thus, in this fashion station 2 adjusts its clock rate toward that of station 1. Similarly, as depicted in Figure 5, station 1 regards the clock as the master clock and adjusts its clock rate toward that of station 2.

Practically, it is impossible to activate the two counters at the two different stations at the same time instant. Therefore, in this study, we consider an arbitrary starting sequence as follows: 1) At an arbitrary time instant t_1, either the counter at station 1 or the counter at station 2 is activated; 2) The other counter is activated at an arbitrary later time instant $t_2 (t_2 > t_1)$

Let ω_1 be the free running radian frequency of VCO_1, then we can write

$$s_{11}(t) = \sin \rho_{11}(t)$$

$$= \sin \left[\omega_1 t + a_1 \int_0^t v_1(\tau) d\tau + \theta_{11} \right]$$

and

$$s_{12}(t) = \sin\left[\rho_{11}(t-\tau_{12})\right]$$

where τ_{12} is the time delay introduced by the channel. Similarly, the free running frequency of VCO_2 is denoted ω_2 and

$$s_{22}(t) = \sin \rho_{22}(t)$$

$$= \sin\left[\omega_2 t + a_2\int_0^t v_2(\tau)d\tau + \theta_{22}\right]$$

and

$$s_{21}(t) = \sin\left[\rho_{22}(t-\tau_{21})\right]$$

The transmission medium from station 1 to station 2 is not identical with the transmission medium from station 2 to station 1; therefore, τ_{12} differs from τ_{21}.

Behavior of the System in the Slave-to-slave Mode This section summarizes some analytical results for the slave-to-slave mode of operation.

Before the two stations are mutually synchronized, $s_{11}(t)$ is sin $\omega_1 t$ and the signaling rate of station 1 is $h\omega_1$ digits/second. (h is a proportionality constant. For example, $h = \frac{1}{2\pi}$ when station 1 transmits a digit at every second zero crossings of $s_{11}(t)$.) Similarly, before the two stations are synchronized, $s_{22}(t)$ is sin $\omega_2 t$ and the signaling rate of station 2 is $h\omega_2$ digits/second. We have shown that whe n the two stations are mutually synchronized, $s_{11}(t)$ and $s_{22}(t)$ have the same zero crossing distribution as $s_0(t) = \sin \omega_0 t$ and the signaling rates of the two stations are $h\omega_0$ digits/second, where

$$\omega_0 = \frac{1}{k_1 a_1 + k_2 a_2 + k_1 a_1 k_2 a_2 (\tau_{12}+\tau_{21})}\left[\omega_1 k_2 a_2 + \omega_2 k_1 a_1\right.$$

$$+ \omega_1 k_1 a_1 k_2 a_2 \tau_{12} + \omega_2 k_1 a_1 k_2 a_2 \tau_{21}$$

$$+ [u_1(0) + k_1\theta_1 + k_1 a_2 R_{21}(0)]k_2 a_1 a_2$$

$$\left. + [u_2(0) + k_2\theta_2 + k_2 a_1 R_{12}(0)]k_1 a_1 a_2\right]$$

As can be seen from the above equation, ω_0 depends on ω_1, ω_2, and the following parameters: gains e_1 and e_2 of the two counters, gains a_1 and a_2 of the two oscillators, initial counter outputs $u_1(0)$ and $u_2(0)$, initial phases θ_1 and θ_2 initial filter outputs $v_1(t)$ and $v_2(t)$, and the time delays τ_{12} and τ_{21} in the communication channels.

The synchronization is satisfactory if $h\omega_0$ is sufficiently close to $h\omega_1$ or $h\omega_2$. More specifically, the steady-state signaling rate is satisfactory if

$$h\omega_1 - \epsilon < h\omega_0 < h\omega_2 + \epsilon$$

when $\omega_1 < \omega_2$, and if

$$h\omega_2 - \epsilon < h\omega_0 < h\omega_1 + \epsilon$$

when $\omega_2 < \omega_1$. The number ϵ is a prescribed small number.

Since ω_0 depends on so many parameters, it is not immediately clear whether ω_0 satisfies the above specifications. After some derivations, we have shown that ω_0 will satisfy the above specifications if the gains of the two stations are designed to satisfy the following two simple constraints

$$e_1 a_1 < \frac{\epsilon}{6h}$$

$$e_2 a_2 < \frac{\epsilon}{6h}$$

Since these two constraints can be easily satisfied and are independent of all the other parameters in the system, we conclude that the steady-state signaling rate can be easily made satisfactory regardless of the starting sequence, the initial system conditions, and the time delays in the communication channels.

REFERENCES

1. Gardner, F. M., Phaselock Techniques, John Wiley and Sons, Inc., New York, 1966, page 65.

2. Gersho, A., and Karafin, B. J., Mutual Synchronization of Geographically Separated Oscillators, B. S. T. J., Vol. XLV, No. 10, December, 1966, pp. 1689-1704.

3. Karnaugh, M., A Model for the Organic Synchronization of Communication Systems, B. S. T. J., Vol. XLV, No. 10, December, 1966, pp. 1705-1736.

4. Brilliant, M. B. , The Determination of Frequency in Systems of Mutually Synchronized Oscillators, B. S. T. J., Vol. XLV, No. 10, December, 1966, pp. 1737-1748.

5. Williard, M. W., Analysis of a System of Mutually Synchronized Oscillators, IEEE Trans. on Communication Technology, Vol. COM-18, No. 5, October, 1970, pp. 467-483.

6. Williard, M. W., and Dean, H. R., Dynamic Behavior of a System of Mutually Synchronized Oscillators, IEEE Trans. on Communication Technology, Vol. COM-19, No. 4, August, 1971, pp. 373-395.

7. Saito, T. , Dynamic Characteristics of Mutually Synchronized Systems, Electronics and Communications in Japan, Vol. 51-A, No. 4, 1968, pp. 19-27.

8. West, N. , Synchronous Digital Switching in Highly Interconnected Communication Networks, Proc. Inst. Elec. Eng., Vol. 114, No. 10, October, 1967, pp. 1378-1384.

Table 1. Buffer and counter size requirements. Note that the system parameters should be selected such that $0 < \beta_1 < 1$.

Definition For any positive number a, <a> denotes the integer immediately less than a when a is not an integer. <a> = a when a is an integer.

$$\text{Buffer size} = \left\langle \frac{2CR\omega'}{\beta_1 \pi} + 2 \right\rangle \quad \text{digits}$$

$$\text{Counter size} = \pm \left\langle \frac{4CR\omega'}{\beta_1 \pi} + 3 \right\rangle \quad \text{counts}$$

$$\omega' = \text{maximum value of } |\omega_1 - \omega_2|$$

$$\beta_1 = \frac{4 e_1 a_1 CR}{\pi}$$

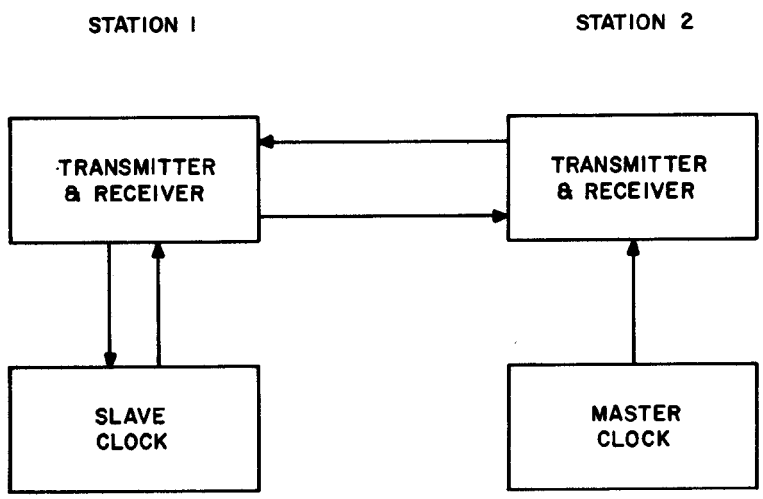

FIG. 1- MASTER-TO-SLAVE OPERATION, BLOCK DIAGRAM.

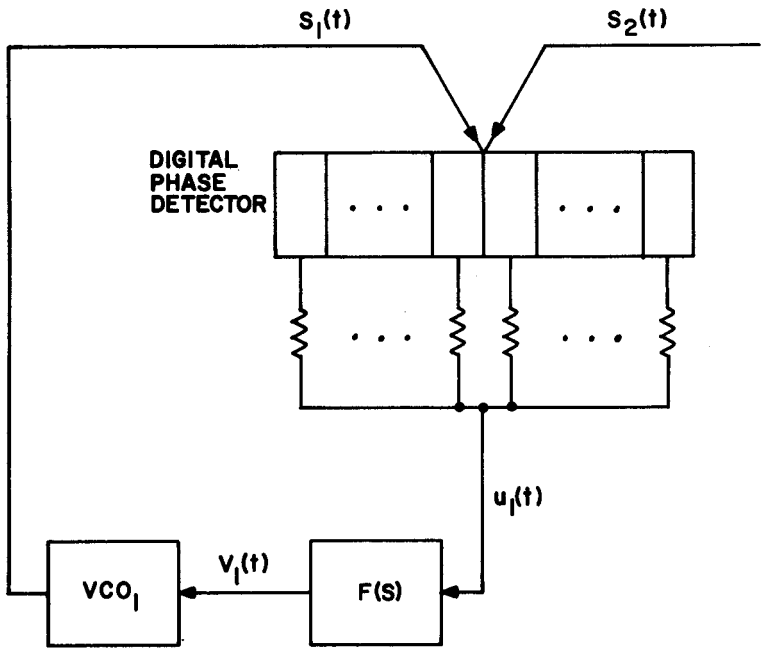

FIG. 2- DIGITAL PHASE DETECTOR AND THE RATE-LOCKED LOOP AT STATION 1.

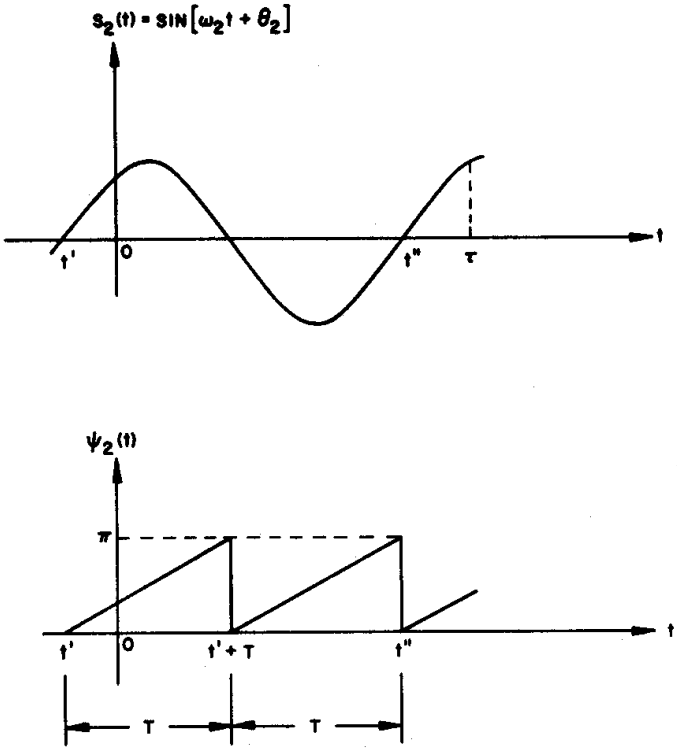

FIG. 3- ILLUSTRATION OF $S_2(t)$, $N_2(t)$, AND $\omega_2(t)$

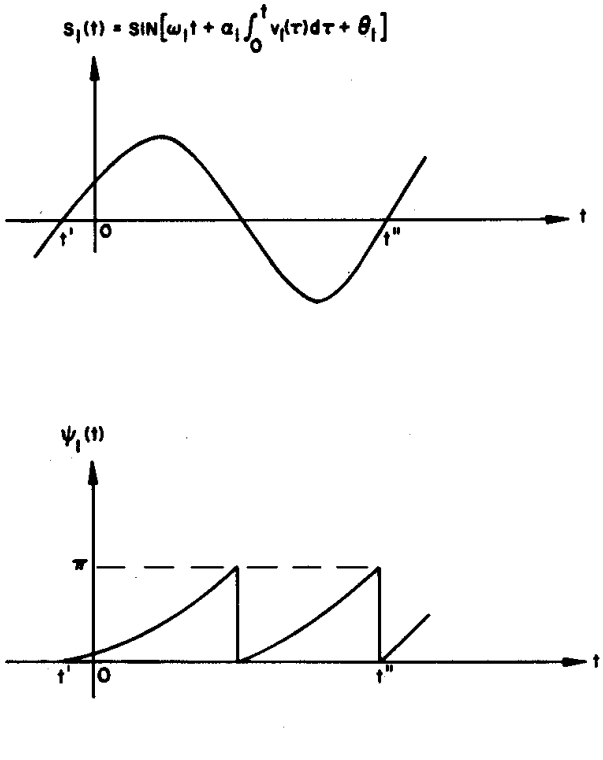

FIG. 4 - ILLUSTRATION OF $S_1(t)$, $N_1(t)$, AND $\psi_1(t)$

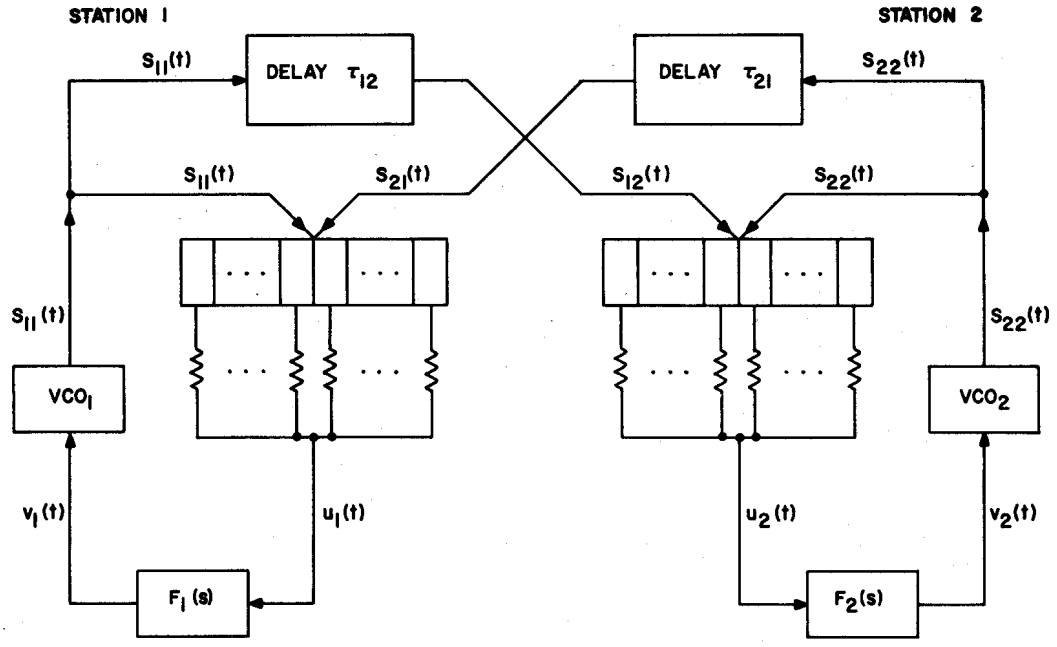

FIG. 5 - SLAVE-TO-SLAVE SYNCHRONIZATION WITH DIGITAL RATE-LOCKED LOOPS AT BOTH STATIONS.