RECENT DEVELOPMENT RESULTS ON THE HELIOS S-BAND COMMAND RECEIVER

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This Work was sponsored by the GfW - Gesellschaft fuer Weltraumforschung.

Summary By joint effort of the US and West Germany a Sunprobe will be launched by 1974 named HELIOS. In the Telecommunications Subsystem the Telecommand Receiver has a keyrole as Experiments have to be switched up to 2 AU distance from earth. The input power at the Receiver Equipment input terminal is -147 dbm with SNR of 6 db in 2 BL_o = 32,5 Hz Loop Bandwidth.

To achieve this sensitivity a Receiver in Phaselocked loop techniques with a low noise Preamplifier had to be developed. In cooperation and with consultance of well known US-Scientists it was possible to design and develope the S-Band Receiver up to the Qualifikation Model in less than two years. This report shall give a survey over concept and design of the receiver and some speceial experiences during development and integration tests.

Introduction With project HELIOS it was the first time that in Germany the necessity for development of a S-Band Transponder with high sensitivity arose. This Transponder had to be compatible with the already existing Deep Space Network of NASA and had to fulfill requirements which were comparable with the technical performance of the Mariner Missions. The frequency ratio had to be f_R/f_T = 221/240. The sensitivity had to enable the Spacecraft to receive commands at 2 AU with only 10 kw Transmitter power into a 26 m Dish. No work was done up to 1969 in the field of S-Band transponder, so the preparatory time of two years and the active development time of two years up to the Qualification Model was considerably short for this advanced programme.

AEG-TELEFUNKEN as subcontractor of MBB has respnsibility of the whole transponder. The work was devided into three parts. System Engineering, development of the Receiver Equipment and development of the Transmitter Equipment. The latter was given as Subcontract to the French Company Thomson-CSF.

Objective of this paper is to describe the design concept of the Receiver and to publish the technical Data achieved up to now. Existing problems and experiences will be mentioned .

For this reasons the organization of the paper will start with a survey over the functional blocks of the HELIOS telecommunications Subsystem going on to the particular description of the S-Band Receiver block diagram. Details of the mechanical and electrical design will be shown to enable comparison with already existing equipment of similar nature. At the end of the referate different solutions of parametric amplifier and Transistor amplifier for provision of the low noise figure will be discussed.

Short survey over the Transponder Subsystem The HELIOS Transponder is a combination of a Transmitter with 20 watt TWT Amplifiers and a Receiver System which is devided into three main units.

- the Preamplifier
- the Receiver
- the Command Detector

The first two items of the Receiver Equipment will be objective of our description the command Detector will be covered by another paper (Lit. 1).

Due to the Mission requirements the Transponder has to fulfill several tasks:

Reception of Command Symbol stream and carrier demodulation.

- Subcarrier demodulation and one channel Bit regeneration for the command symbol stream.
- Coherent operation i.e. supply of 38 MHz to the transmitter as a coherent base frequency for the transmitter
- Ranging operation i.e. receiving and first demodulation of a 1 Mbit ranging signal which is modulated on the Transmitter coherent carrier to make a loop for range measurements.
- Transmission of telemetry data + Ranging signals in several operational power levels HP (High Power), MP (Medium Power), LP (Low Power) with several phase deviations (HCS - High Carrier Suppression-, LCS - Low Carrier Suppression -) over three different Spacecraft Antennas H. G. A. (High Gain Antenna), M. G. A. (Medium Gain Antenna).

Because of Reliability requirements the Receiver as well as the transmitter are redundant in all essential Parts (Fig. 1).

Switching of the individual operational modes of RIP power to the three antennas is done in the RF-DU (Radio Frequency Distribution Unit) which containes also two Diplexers for separation of the Receiver and Transmitter Frequencies.

The Receiver Block Diagram The receiver itself consists essentially of the three main units Preamplifier, S-Band receiver and command Detector. See upper part of Fig. I. Since the receiver is made of two parallel chains we will explain one half of the units. One exception: the unit for amplification and first demodulation of the ranging Signal is only one time necessary therefore only one chain has the “Range Unit” incorporated. The second chain contains instead of the Range unit a Channel Selection Unit to select between the two VCXOs of the two chains. One of them is connected to the transmitter Modulator input as coherent frequency Source. Because of the symmetry of the two chains the basic idea for the Design of the three redundant boxes was to split each box into two identical halves, which are interchangeable in their individual parts in order to raise the possibility to exchange modules of chain I against chain II if in any model of the later manufacturing procedure replacement of modules might be necessary. So for instance a Model which was assigned for a chain I function with ranging could easily taken and retrofitted for chain II function with a CSU unit.

Fig. 2 shows all essential Blocks of a (half) Receiver unit. Actually the Receiver is a double superheterodyne Receiver with a second order phase locked loop demodulator. The major subassemblies after the Preamplifier - which will be explained later - are an Image Rejection Filter 2,116 Mc followed by a low noise mixer with Schottky Barrier Diodes and a low noise 47,5 Mc IF-preamplifier preceding the Ist and IInd IF stages (9,5 Mc). After a limiter stage with Xtal Filter a phase detector demodulates the PSK modulated squarewave Subcarrier of 512 Hz from the Carrier. Coherent AGC is generated in a second phase Detector which is in quadratur6 to the first one and which enables the IF-amplifiers to work in a dynamic range of 100 db with 1 db output signal change. The VCXO is as well the reference for the 2 phase detectors as for the drive to the transmitter after multiplication by 4, as for the injection frequencies in the Ist and IInd Mixer. In Fig. 2 the essential multiplication factors of the frequencies in the blocks are shown as a multiple of the VCXO-Frequency FQ.

A Ranging signal path is derived from the IInd IF before entering the Xtal Filter. Extreme care had to be taken to prevent a leakage from the VCXO over the Ranging phase detector back into the Xtal Filter and main phase detector. Therefore the ranging phase detector is driven in small signal ranges of 20 mv and the IF isolation amplifier has an isolation of more than 50 db.

The Channel Selection Unit is provided to enable both of the two VCXOs in the Receiver Subsystem to serve as a coherent drive to the transmitter. This unit is a relay operated switch selects 4x the VCXO Frequency of VCXO I or VCXO II of either

receiver chain. The unit also containes the command logic to operate the receiver chains either with VCXO I or VCXO II as a coherent Frequency source. Of course the receiver with the chosen VCXO must be in lock. Lock indication therefore is provided and telemetered down to the ground station for both receivers.

Static phase error, AGC-level, Temperature and presence of RF- power in the multiplier chains is telemetered also. Mechanical Design. The mechanical Design to a great extend depends upon questions of accessability, shielding, easy testing of subassemblies, small weight, orientation in the integrated spacecraft, EMC engineering, possibility of later changes. All this had to be accounted for before the circuits themselves were readily developed. RF connections should be as short as possible, functional blocks should be close together to prevent scattered ground loops with the possibility of leakage and coupling into other RF circuits causing DC offset of the phase detector thereby. Contrary to the technique of functional building blockes staked together and connected over shielded RF-cables which may stray and couple between each other we tried to combine good shielding and short RF connections by packaging the circuits into a double T frame which has good accessability from both sides and which has milled compartments for the subassemblies. Each Subassembly is a PC-Baord. The electrical circuitry uses ICs to a great extent.

The housing of the receiver is designed so that the very sensitive loop detector part is thoroughly shielded from IF and multiplier sections by a milled wall. On the other side of this wall milled cavities for Ist + Iind IF and for the multiplier chain are provided. Ranging assembly or Channel selection unit are mounted on top of the IF and multiplier sections, separated and shielded by a very tight metal cover (Fig. 3) (Fig. 4).

The housing is closed on both sides by blades of metal which slide in narrow slots. Good RF contact of the sliding cover is provided by spring action of the edges of the cover.

Technical Data and experince with the S-Band receiver Technical Data obtained during development refer to Table 1. During late 1971 the first Labmodels and EM-Models were completed and tested. A design verification test was conducted at the JPL-Pasadena. Later in April 72 compatibility with the DSN Station DSS 71 was tested. These tests, showed considerabel performance problems which had to be corrected very fast in 5 Month in parallel to the first integration tests which had to prove the ability of operating together with the transmitter without selflock or degradation Problems. In this respect one of the gratest concerns regarding the transponder development was that the design and development of Transmitter and Receiver had been devided between two design locations 500 miles apart in Europe and that by-this distance development problems regarding selflock could be detected too late for effective changes in the equipments. But just this point turned out to be not troublesome to the whole equipment. The points of trouble detected during Laboratory and integration tests of the EM-Models

were problems concerning the receiver itself. Compatibility with respect to operational requirements was met.

Experience with the first Labmodels showed that the following points had to be corrected:

- Phaselock circuits with respect to Loop gain and DC-offset of phase Detectors
- Noise Limiting in the IF, level plan
- AGC-dynamic range of receiver
- Noise figure of the receiver

With respect to these design parameters we can report the following:

1) Phase lock circuits
   - In our design the CA 3028 A is used. This integrated circuit comprises a differential amplifier with a third transistor acting as a current source for the emitters of the differential amplifier. Now you can use this circuit in that way that the signal is applied to the differential input, and the reference, which will be the larger voltage, to the input of the series transistor. The effect of this circuit is to have some sensitivity together with a good limiting effect. But, since DC offset of the differential parts is very sensitive to levels and waveshapes of the input signal and since the IF signal output was variing in our basic design by 10 db, the phase detector suffered high DC offset depending upon the signal voltage in turn was a function of input power to the receiver. After changing to the other possibility of applying the fixed level of the VCXO signal to the differential input and the variable level to the linear inputDC-offset decreased considerabely. At the same time provisions had to be made to prevent different wave shapes to enter the linear input and to prevent conducted EMC, esspecially the beat frequency, from entering and disturbing the PD-Function through the power lines. By this pushing effects were eliminated (Fig. 6, Fig. 7).
   - Loop gain should be considerably high to decrease Loopstress during frequency offset (Fig, 5).

2) Noiselimiting, IF Level plan
   Extensive discussions had been done in which the problem of limiting by excessive noise was stated very early. But figures found by experience with older concepts and transistorized IF amplifier were not applicable to our IF design using the IC MC 1550 G. Our first philosophy was: In order to get a small SPE-offset have high IF-signal levels, get inputs at the phase Detectors that are high in comparision to those coherent levels which could be present at the same terminals by Leakage or stray. - This policy is dangerous. - The noise accompanying the signal particularly at threshold levels is much larger than the linear operating range of the last IF stages.

There is no way around: in order to have the correct Limiter alpha-Factor and to prevent limiting of the IF by noise the level plan of the receiver has to work with linear behaviour for noise and signal levels which are in the range of some millivolts in the last IF stages. At the same time the gain of the IF has to be as high as possible in order to shift the knee of the Limiter curve to smaller input powers (Fig. 8).

3) AGC dynamic range of the receiver
The measure of extending gain in the IF in turn makes an extended AGC-control necessary to absorb the excessive gain. For HELIOS the dynamic IF-signal range of 85 db is brought under control by an AGC-range in excess of 100 ... 110 db.

4) Noise figure of the receiver
Carrier threshold of course is a direct function of Noise temperature of the receiver. Therefore during the time of development several approaches were undertaken, which tended to lower the overall Noise temperature of the receiver and to use a preamplifier to reduce the noise figure to the specified value of 2,9 db or 280°K. The schematics in Fig. 9 show several configurations investigated during development. For the S-Band receiver part variations of Noise Temperature in the order of 5000°K (N F = 12,6 db) to 1100°K (N F 6,8 db) are possible depending upon the configuration. Since a good compromise between available gain, lowest available Noise Figure, moderate technical complexity and availability of qualified and space proved electrical components had to be made, the configuration B. IRF-Filter-Low Noise Mixer-IF Preamplifter-IF, Amplifier was chosen resulting in 1850°K or 8,7 db NF. For reducing the overall Noise Figure to the specified value a parametric preamplifier is under development which has typical Noise Temperatures from 150°K to 200°K and 14 db of gain. With these figures the whole Receiver Equipment gets a typical Noise temperature of 224 to 274°K of 2,5 - 2,9 db NF.

The parametric preamplifier is non reciprocal and does not use circulators. The amplifier is a chain of an up-and down converter with a pump generator pumping currents into the two varactor diodes with $\varphi = \pm 90^\circ$ phase difference. The mixer chain comprises in that way a phasenonreciprocal network at the signal frequency if a reactive admittance y_n is placed between output and input terminals. The available gain depends upon the ratio between pump- and signalfrequency. With 7 Gc pumpfrequency the available gain is 14 to 18 db, the bandwidth at 14 db gain is adjustable to 10 to -20 Mc.

The functional schematic of the Amplifier is shown in Fig. 10 to realise these conditions considerable Know How had to be gained to learn the tuning and rather tricky alignment of the 6 circuits interacting each other. Fig. 11 shows the block diagram with the parametric amplifier and all auxiliary electronic blocks for stabilizing the pumppower,

pump frequency and temp. compensating of amplifier and pump oscillator at 1,4 GHz before multiplying x 5. Technical Data of the device are to be seen in Table 2.

To-day after 2 years of development the Noise figures of transistors in the 2 GHz frequency band caught up very close to those achieved by this parametric amplifier. Furthermore a transistorized amplifier does not need as many auxiliary electronic circuits, is simple with respect to manufacturing processes of the transforming input and output networks and has a lower current consumption of about 1/10 of that of the pump generation for the parametric type.

For these reasons a parallel development of a transistorized preamplifier was begun in late 71 (MT 4000 Fairchild). Data gained with first Labmodels were very enconraging 14 db gain and 3,0 db NF of the amplifier made an overall Receiver Noise Figure of 3, 7 db possible. Of course specimens must be selected and considerable effort for proper matching of optimum parameters has to be done.

The tradeoff between choice of parametric amplifier and transistorized amplifier is now in progress. It tends toward the transistorized version in spite of having 1 db less Noise performance. The benefit of higher reliability, few parts, less weight and less power consumption will overrule the sole demand for maximum margin in Link design.

Conclusion and acknowledgement The Command Receiver of Project HELIOS is a redundant S-Band double conversion receiver with second order phase locked loop, coherent AGC and ranging facility. The operational range is 2 AU by having a Noise temperature of 300°K. After a first model for design verification tests some changes in level plan and circuit design led to a model with excellent performance and full compatibility with the DSN Network.

Since a mixed technique of printed circuits with Integrated circuits is applied the equipment has small weight, small current consumption, has an extremly low magnetic content and has a low absolute threshold in the order of -161 dbm. Two types of preamplifiers are available, a transistorized version with 290°K Noise temperature and 14 db Gain or a parametric amplifier which is more complex but has low Noise temperatures as low as 150°K which are not reached with transisters up to now.

At this point our thank and acknowledgement is given to Dr. FM Gardner and specialists of the JPL, whose consultance and advices in many questions of the phase lock techniques were of considerable importance to our work.

References

Lit. 1	S. Knapp	A Single Channel Command Detector for Deep Space Mission
Lit. 2	R. Maurer	Nichtreziproker parametrischer Verstärker für das Mikrowellengebiet.

Table I Technical Data of the HELIOS Command Receiver (* = with preamplifier)

Nominal Frequency	2115 . 699 846	Mc
Absolute Carrier Threshold*	- 159	dbm
Command Threshold*	- 144	dbm
Command + Ranging Threshold*	- 126	dbm
Dynamic Range*	to - 70	dbm
Noise Temperature*	300^{o}	K
VCXO Frequency	9,57	Mc
Lon term stability	2×10^{-5}	
Subcarrier for Command modulation	512 / 448	Hz squarewave
Symbolrate	8	sps
Modulation		PSK / PCM
S/N in 8 Hz	13	db at Command Threshold
RF aquisition -144 dbm - 70 dbm	80 Hz/sec $\pm$ 10,5 kc 500 Hz/sec $\pm$ 21 kc	
Phase detector gain factor	30	mv/deg
VCXO gain constant	150	Hz/volt
Nominal loop noise Bandwidth 2 BL_o	20	Hz
Power consumption	2,7	watt
Reliability (3400^{h})	0,9656	
Weight (w.o. Preamplifier)	1,8	kg
Dimensions	26 x 14 x 5,5	cm^3
Volume	2000	cm^3

Table II Technical Data of Parametric preamplifier (non redundant)

Nominal frequency	2115.7	Mc
Bandwidth	10 ... 20	Mc
Gain	13 ... 15	db
Noise Temperature	150 ...200°	K
Noise Figure	1,7.. 2,3	db
Power consumption (non redundant)	3,5	w
Passbandshift/pump frequency shift	1	Mc/Mc
Gainshift/Pumppower	2	db/db
Gainshift/Pumpfrequency	0,6	db/Mc
Paramp oscillator Frequency	1,400	Mc
Pump Frequency	7,000	Mc
Multiplier Passband(Filter Bandwidth)	334	Mc
Pin diode attenuation range	6	db
Pin Diode attenuator	4,5	db/mA
Level Detector characteristic	12,5	mv/mw
Reliability (3.400^{h})	0,9927	
Weight	1,1	kg
Dimensions	20 x 12 x 5	cm^3
Volume	1 200	cm^3

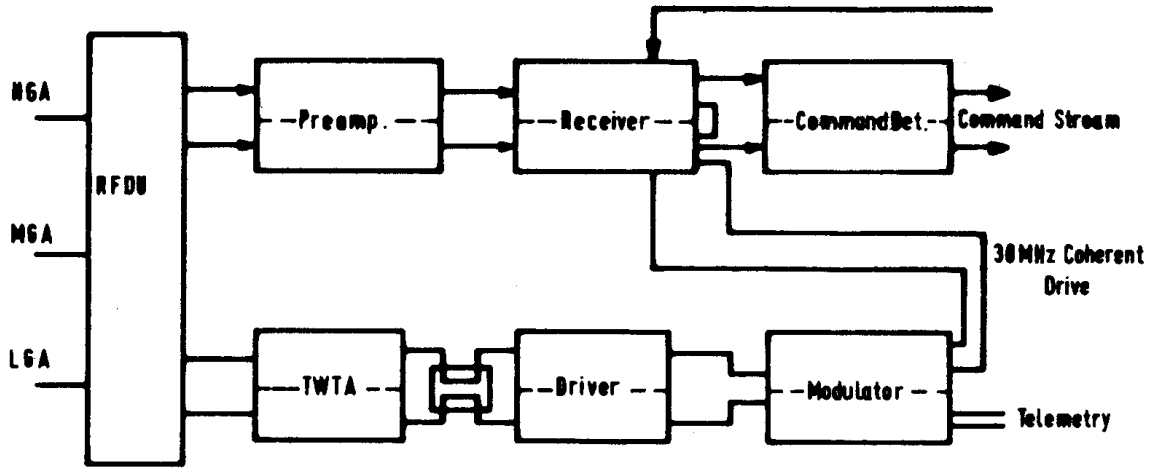


Fig. 1 Block Diagram of Helios Transponder

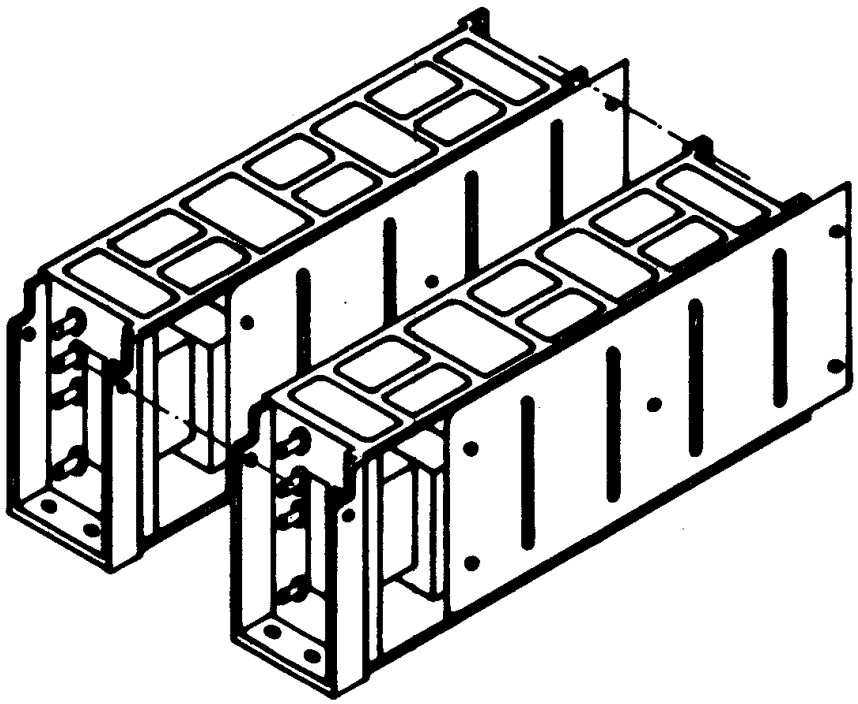


Fig. 3 Principle Housing Design of Helios Receiver Components

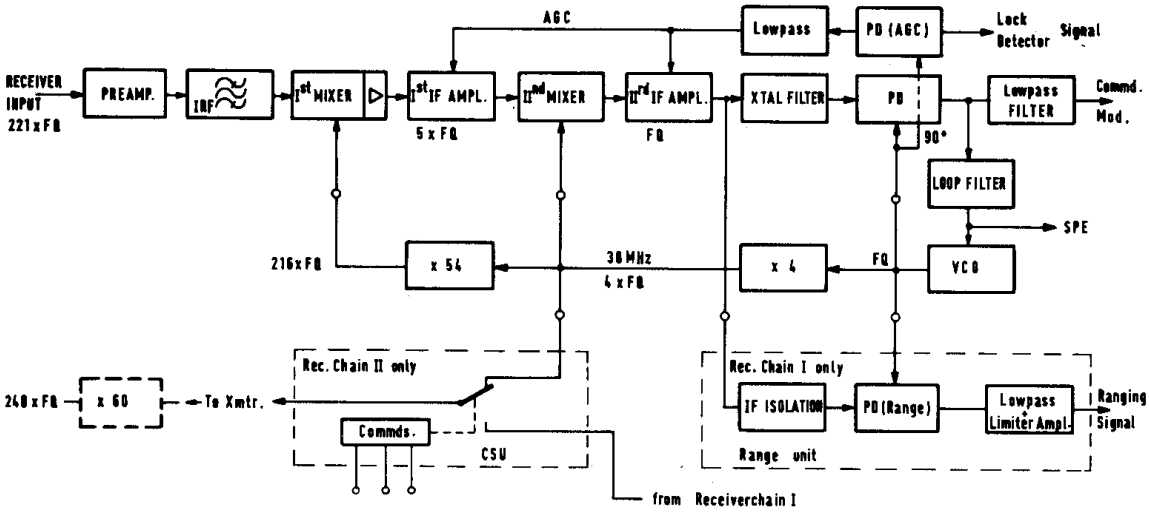


Fig. 2 HELIOS RECEIVER BLOCK DIAGRAM

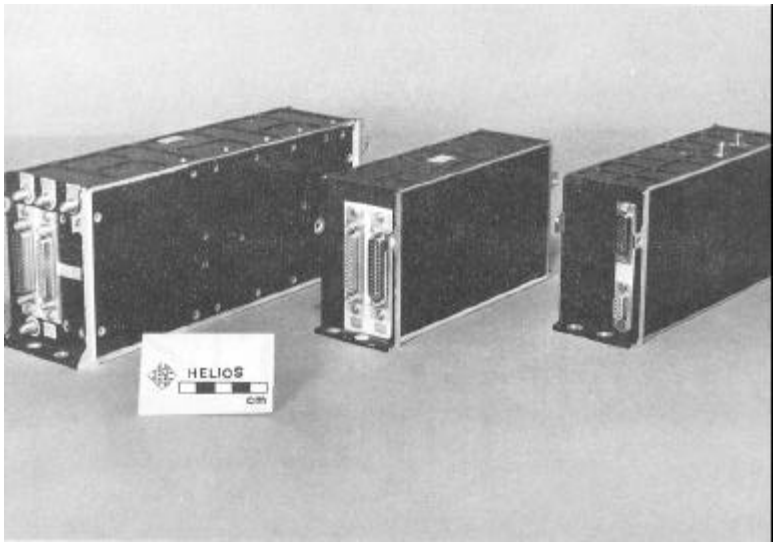
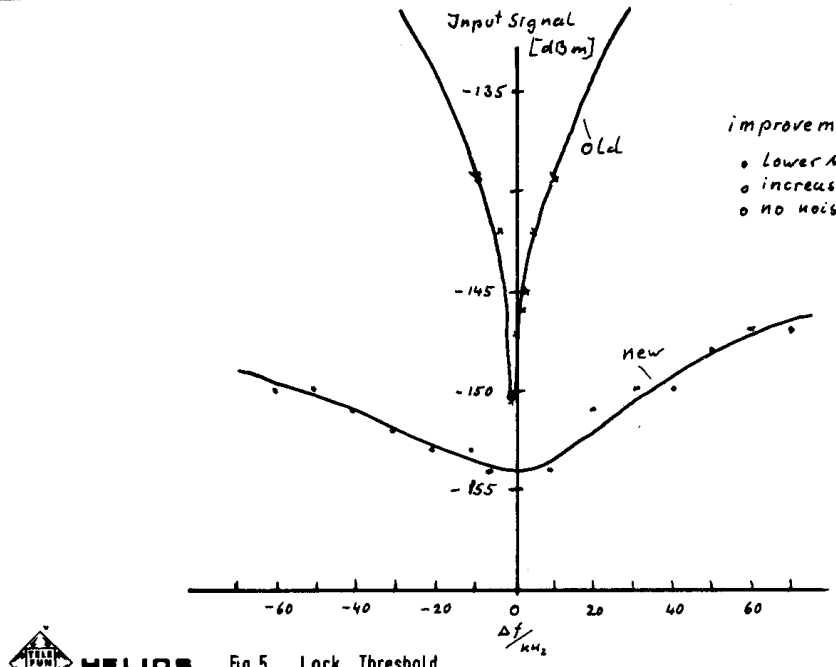


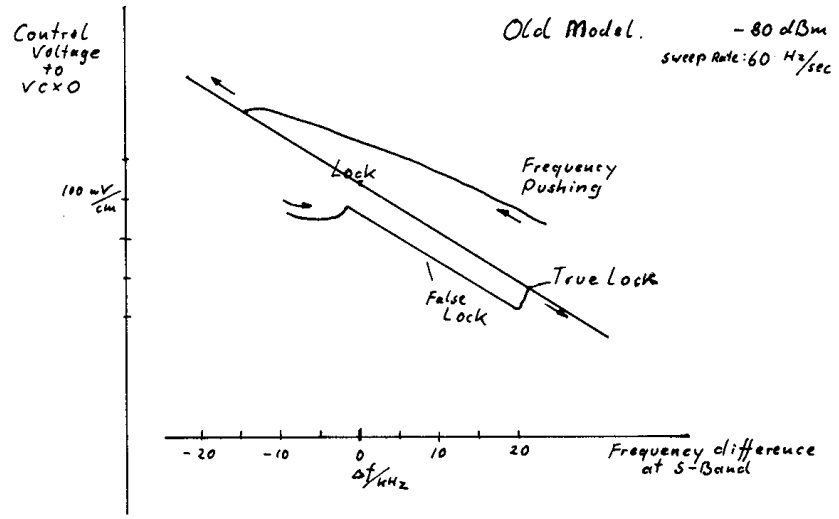
Fig. 4 Helios Command Receiver half non -redundant Unit

Middle: Command Detector

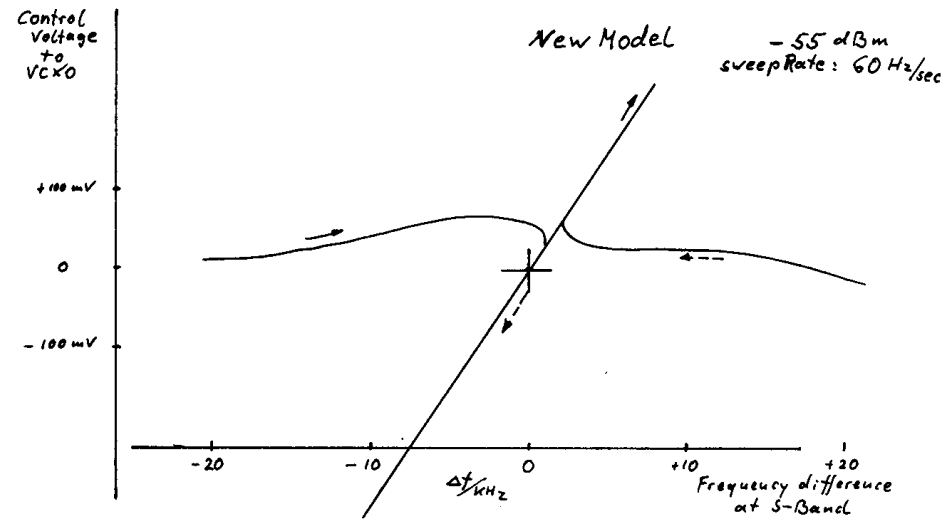
Left: Receiver **Right: Preamplifier**



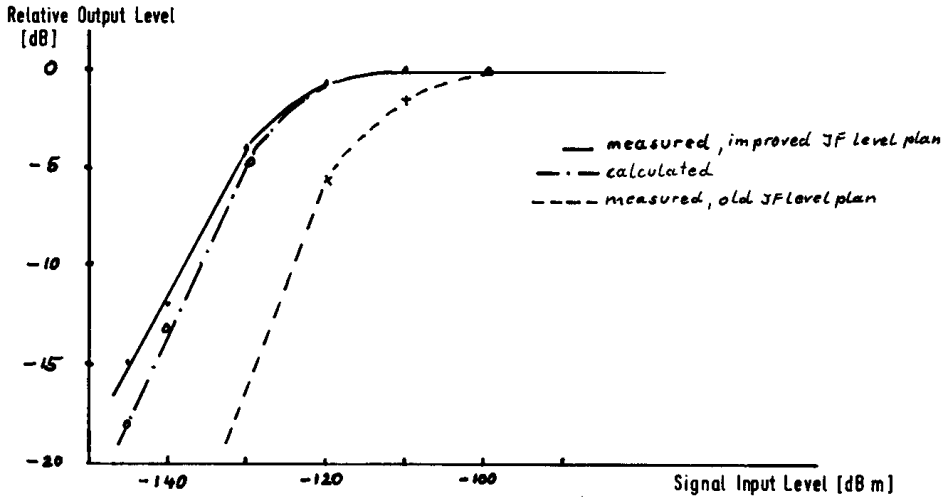
HELIOS Fig. 5 Lock Threshold



HELIOS Fig. 6 Aquisition Behavior Strong Signal



HELIOS Fig.7 Aquisition Behavior Strong Signal



HELIOS Fig. 8 Limiter Suppression Factor

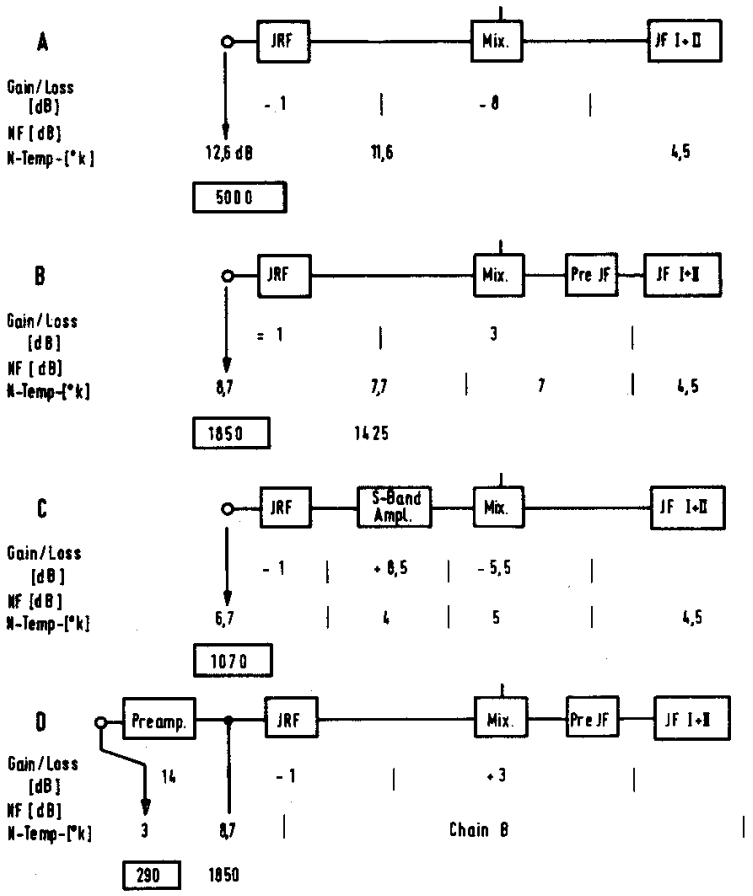


Fig. 9 Receiver Configurations and Noise Figures

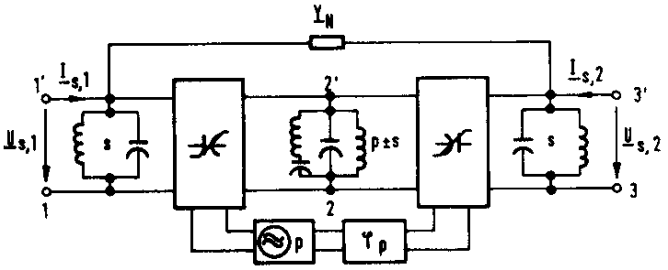


Fig. 10 Principal Schematic of Nonreciprocal Parametric Amplifier

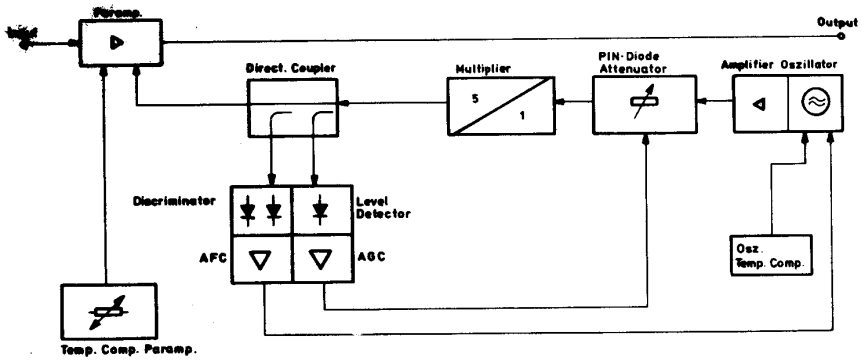


Fig. 11 Preamplifier