A DIGITAL INTEGRATOR FOR AN S-BAND HIGH-SPEED FREQUENCY-HOPPING PHASE-LOCKED LOOP

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ABSTRACT

Phase-locked loop (PLL) frequency synthesizers used for high-speed data transmission must rapidly hop and lock to new frequencies. The fundamental problem is that the settling time depends inversely on the loop bandwidth, and increasing the bandwidth causes unwanted noise interference and stability problems for the circuit. We demonstrate the feasibility of replacing the analog integrator in the PLL with a digital integrator. This circuit has advantages of increased hopping speed, ability to compensate for temperature drift and system stability. PLL lock-in was demonstrated in a prototype circuit designed and built with both discrete components and with a programmable logic device.

KEY WORDS

Phase-locked loops, frequency synthesizers, fast frequency hopping

INTRODUCTION

PLL frequency synthesizers are a basic building block of communication systems. When used for high-speed data transmission, the PLL must be able to rapidly hop and lock to a new frequency. The fundamental problem is that the settling time is inversely proportional to the loop bandwidth. Increasing the bandwidth in order to decrease the settling time allows unwanted sidebands from the phase detector to pass through. The noise interference from these sidebands causes stability problems for the circuit. The loop bandwidth depends on the loop gain, the filter cutoff frequency and the frequency divide ratio. In practice, the filter cutoff is often the limiting factor [1].

To solve this problem, a PLL using a digital summer to replace the analog integrator is proposed. In this approach, three advances are achieved simultaneously: (1) the hopping speed is greatly increased by the replacement of the analog integrator with digital; (2) the system is adaptive and can compensate for temperature drift in its components; and (3) the digital circuitry provides lead compensation to assure system stability.

BACKGROUND

The idea of replacing analog PLL circuitry with digital to reduce size and cost and improve performance and versatility has been around since the late 1960's [2]. (It should be clarified here that the Emhiser PLL discussed in this paper is not really a digital PLL at all, but is a hybrid circuit using an analog VCO and other analog components.) One early approach for designing fast frequency-hopping PLL synthesizers was to use non-integer ratio dividers [3,4]. In a traditional PLL, the frequency step size is an integer multiple of the reference frequency (f_{ref}). The bandwidth also depends on f_{ref} for system stability. The bandwidth needs to be much less than f_{ref}, typically 1/10 or less, to avoid unwanted sidebands [5]. Since the settling time depends inversely on the bandwidth, there is a trade-off between step size and hopping time. In these "fractional-N" or "cycle-swallower" PLLs, however, the step size can be a fraction of f_{ref}. Therefore, f_{ref} and the bandwidth can be increased and the hopping time correspondingly decreased. However, these PLLs suffer from serious noise problems, including sideband spurs at fractional multiples of the reference frequency.

Another early approach was to preset the VCO target frequency [6]. This method as conceived did not find wide use as the pre-programming was not simple and it did not easily allow for compensation of temperature drift. However, the Emhiser approach of holding voltage information in RAM is based on the same concept. More recently, a popular approach is to combine a direct digital synthesizer (DDS) and a PLL [7,8,9]. Like the fractional-N PLL, the main advantage of this approach is to improve resolution. By making the frequency step size, here controlled by the DDS, independent of f_{ref}, the circuit can operate with higher f_{ref} and faster hopping time. Including the PLL with the DDS allows a higher output frequency than with a DDS alone. The disadvantages are that some of these designs are quite complex, and the speed is still limited by the loop filter.

Another approach is based on temporarily increasing the loop bandwidth to speed up the loop during hopping. This is most often done by switching between multiple loops [10,11,12,13]. Typically, there will be one narrow bandwidth, slow, low noise loop for in-lock operation, and a higher bandwidth, faster loop for jumping to a new frequency. While the switching in these cases can be very rapid, there are issues of glitches during switching, dead zones and synchronization, and additional circuitry and power are required. Finally, several recent approaches use a digital calculation of phase error to speed up the locking process [14,15,16]. These are in some ways similar to our approach. However, none of these references demonstrate closed-loop response in a comparable frequency range (2.4 GHz).

A FAST FREQUENCY-HOPPING PLL

For reference, a block diagram of a traditional PLL frequency synthesizer is shown in Figure 1. The high frequency output signal is generated by a voltage-controlled oscillator (VCO), a tunable oscillator whose output frequency can be adjusted by an input voltage. The output of the VCO is integrated to give an output phase θ_o and is then stepped down by a factor N by the frequency divider. The phase detector compares the divided VCO phase signal θ_o/N to a reference phase θ_i, where θ_i represents the phase of the crystal oscillator input signal. The phase detector output is a voltage proportional to the difference between the divided VCO output phase and the reference phase. The phase detector output signal is amplified, filtered to remove noise and high-frequency components, and fed to the VCO input. If non-zero, this provides a correction to the VCO to keep it locked to the desired frequency.

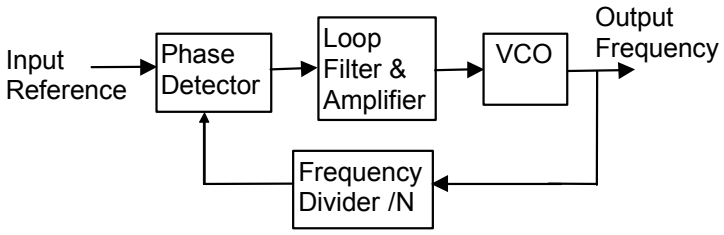

Figure 1. Block diagram of a PLL frequency synthesizer.

The concept for a fast frequency-hopping PLL-based transmitter was proposed by Emhiser Research, Inc. [17]. A block diagram of the transmitter is shown in Figure 2. The information that sets the different frequencies is stored in the RAM. When the command to switch frequencies comes in, the RAM location with that frequency information is immediately accessed. Until the output stabilizes at the new frequency, the digital adder will increment the signal up or down as needed based on the error signal from the phase detector. It is expected that the hopping time is less than 1 microsecond. If operating conditions such as temperature have shifted the voltage required to establish a certain frequency, the new information will be stored in the RAM for the next time. Therefore, this transmitter can learn and adapt to changing environments.

In a traditional PLL, the error signal from the phase detector goes through an analog integrator. In this PLL, the digital circuitry consisting of the adder and RAM replaces the analog integrator. As well as replacing the time-integration function with a clocked adding function, the digital circuitry must supply the lead compensation provided by the integrator to assure stability of the digital circuit. In general, stability is a more difficult issue in digital systems as compared to analog systems. This is primarily because the requirement for stability in the z-domain (all poles within the unit circle) is more restrictive than that in the s-domain (all poles in the left-hand plane). In addition, the clock rate adds an additional variable to the stability analysis. A stability analysis of this circuit is submitted for publication elsewhere [18].

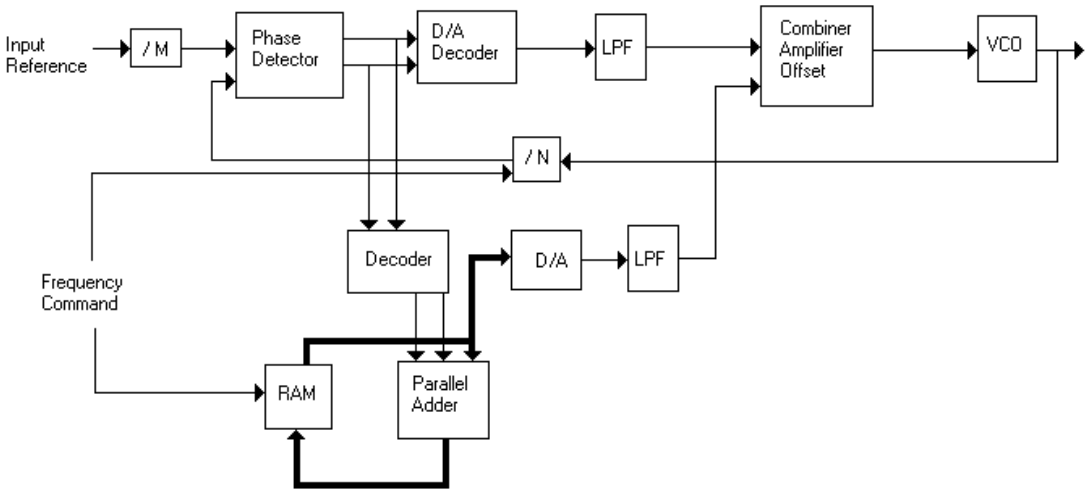

Figure 2. Block diagram of the fast frequency-hopping PLL.

EXPERIMENTAL RESULTS

The PLL with digital integrator was implemented using an existing 2.2525 GHz transmitter provided by Emhiser for the VCO, phase detector and frequency divider circuitry. The usual integrating amplifier and low-pass filter are disconnected so that the digital integrator and combiner/amplifier/offset blocks can be inserted. The digital integrator portion (decoder-adder-RAM loop) was fabricated in both discrete chips and in a programmable logic device (PLD).

The digital integrator circuit consists of a 16-bit adder, RAM and sixteen D-type flip-flops. The RAM was not included in the discrete chip board for initial testing, but is included in the PLD. The inputs are the decoded up and down commands, as shown in Table 1. The signal ZU is applied to the first adder input and ZD is applied to the remaining 15 inputs. The output is applied to a 16-bit digital-to-analog converter (DAC). This DAC is a critical component, and needs to be chosen for high linearity, monotonicity and speed. The DAC used was the Burr-Brown DAC701. Additional circuitry contains the combiner/amplifier/offset block, decoders and low-pass filters. The design is shown in Figure 3. The phase detector outputs are first held in a pair of flip-flops for synchronization with the adder (or RAM) output. The phase detector decoder is simply a resistor bridge. The phase detector outputs are logic active low, and, as seen in Table 1, the voltage at the center of the bridge is approximately 5, 2.5 or 0 V for the “up”, “no change” and “down” commands, respectively. The simple RC low-pass filters were designed to filter out higher frequency signals from the phase detector. The filtered signals from the DAC and the phase detector decoder are summed at the input to the op amp. The offset is controlled by a potentiometer that can be adjusted to give an output in the desired range for the VCO.

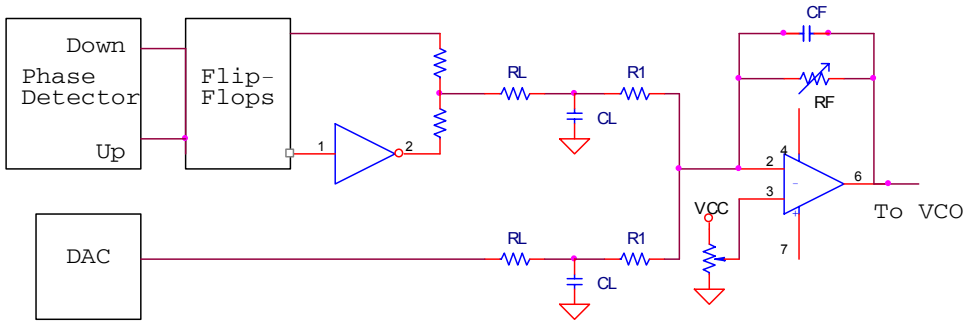

Figure 3. Design of combiner/amplifier/offset block.

Table 1. Decoded UP and DOWN commands.

Phase Detector Outputs		Adder Inputs		Amplifier Inputs	Meaning
UP	DOWN	ZU = $\overline{UD}$	ZD = $\overline{D}$		
1	1	0	0	2.5 V	no change
0	1	1	0	5 V	increase
1	0	1	1	0 V	decrease

The PLD used was the EPF10K20 provided by Altera Corporation. The PLD was programmed in AHDL (Altera Hardware Description Language), which is very similar to the industry standard VHDL. The program was simulated before it was used to program the PLD, and typical results are shown in Figure 4. The decoded up and down commands, ZU and ZD, are cycled through the combinations of 01 (add one), 11 (subtract 1) and 00 (stay the same). It can be seen that the 16-bit output will count up, count down or stay constant as appropriate.

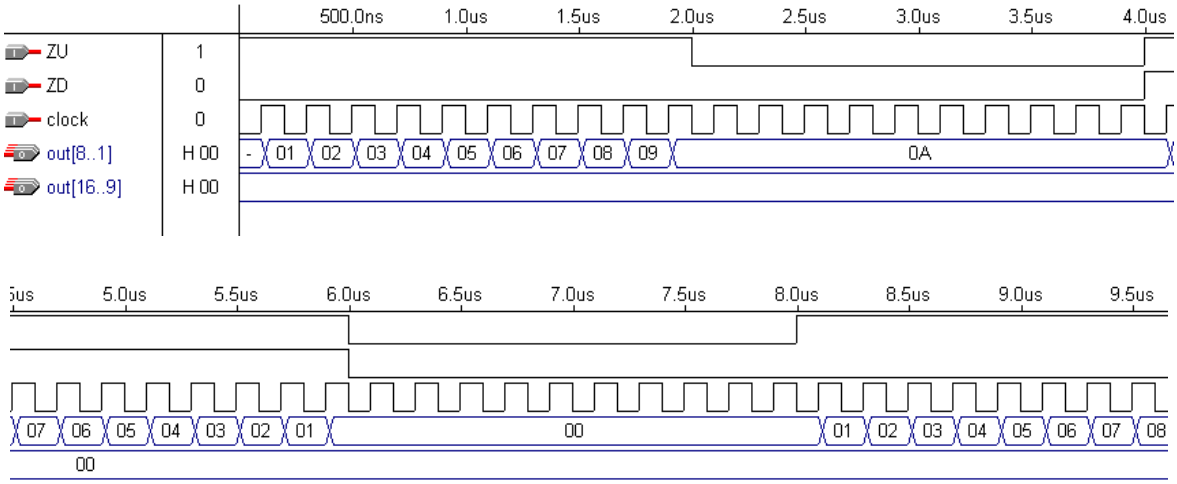

Figure 4. Simulation of PLD program.

The circuit was tested in closed-loop with the transmitter. A typical output spectrum is shown in Figure 5. The circuits with discrete chips and with the PLD had nearly identical results. It can be seen that the output does peak at the correct frequency, but has more noise than is desirable. This is not surprising since the test configuration was not optimal. The discrete chip circuits were implemented on separate test boards with numerous leads and additional connections, and the PLD was on a test board designed for a laboratory package with many long traces and unused connectors.

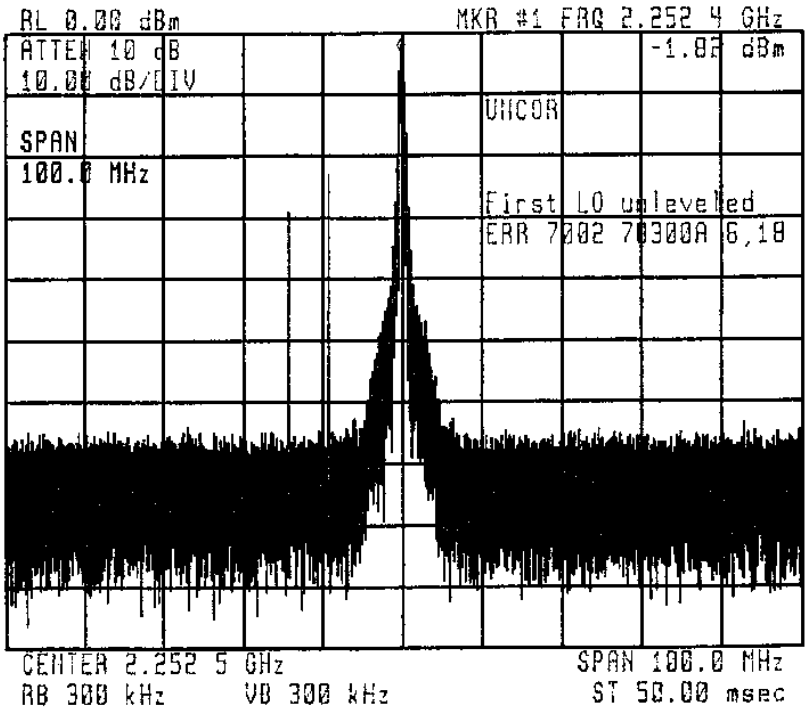

Figure 5. Transmitter output spectrum with digital integrator.

CONCLUSIONS

The objective of this research was to test the feasibility of replacing the standard PLL analog integrator with a digital adder circuit. The purpose of this is to speed up the loop response for fast frequency hopping. In this work, we have shown that the loop will lock with the digital integrator circuit. However, the circuit performance was not ideal, with higher noise and slower settling time than desired. While we have tested the operation and stability of the digital integrator circuitry, we have not yet attempted frequency hopping. Therefore, future work remains to be done in two areas: improving the circuit performance through integration and optimization, and testing its frequency-hopping capabilities.

ACKNOWLEDGMENTS

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