HARDWARE DESIGN AND IMPLEMENTATION OF A MULTI-CHANNEL GPS SIMULATOR

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ABSTRACT

Hardware architecture and design details of a multi-channel GPS signal simulator with highly flexibility is presented, while the dynamic performance objectives and the requirements on the hardware architecture are discussed. The IF part of the simulator is implemented almost entirely in the digital domain by use of a field programmable gate array (FPGA), which mainly include C/A code generators, carrier generators, spreaders, and BPSK modulators. The results of testing the proposed simulator hardware architecture at IF with the help of a GPS receiver are presented.

KEY WORDS

Simulator, Global Positioning System(GPS) , Direct Digital Synthesis, Doppler frequency

INTRODUCTION

Global Positioning System (GPS) signal simulator is expected to generate in real time, the composite GPS signal that would be coincident with the signal at a GPS receiver antenna. When GPS systems are used in critical applications like avionic systems, it becomes essential and often mandatory to exhaustively characterize the performance of such receivers under all anticipated worst-case scenarios including varying platform dynamics and signal impairment (multipath, jamming, etc.). Other than carrying out actual detailed field trials which would be prohibitive from a cost and time standpoint, such a detailed characterization of the receivers would only be possible with help of suitably designed real time GPS signal simulators.

The details of GPS signal structure are provided in reference [1]. The satellite orbital configuration provided a minimum of six satellites in view at any time, with a maximum of 11. Because different satellites have different distance and relative velocity reference to the same

GPS receiver, so when GPS satellites' signals come to the front-end of one receiver, they are different at amplitude, phase and the Doppler shift frequency. Give the receiver platform's coordinates, dynamics and local times, at L1 frequency, the composite signal seen by a civil GPS receiver at its antenna terminals can be presented by[2]

$$r(t) = \sum_{i=1}^{M} A_i(t) C_i(t - \tau_i(t)) D_i(t - \tau_i(t)) \sin[2\pi(f_0 + f_{id})(t - \tau_i(t)) + \phi_i(t)] \qquad (1)$$

where $A_i(t)$ represents the amplitude of the signal received from the ith satellite. $D_i(t)$ represent the data bit transmitted from the ith satellite at the nominal rate of 50bit/s. $C_i(t)$ represents the particular Gold code of length 1023 chips used by the ith satellite at the nominal code rate of 1.023Mcps. $\tau_i(t)$ represents the propagation delay of the ith satellite. f_0=1575.42MHz, f_{id} represents the Doppler shift frequency of the ith satellite. Φ_i represents the initial phase of the carrier of the ith satellite. M represents the number of satellites visible to the receiver at the same time.

Equation (1) shows that the simulator are required not only to produce the GPS signal from different satellite, but also to precisely present the relative phase and different amplitude between them. Development on the techniques of digital signal processing provides more flexible method for the simulator designing. It is possible to incorporate all dynamic signal characteristics into a baseband or IF signal, then up-convert to a radio frequency (RF).

HARDWARE ARCHITECTURE

An overall hardware architecture block diagram of the proposed system is shown in Fig.1. The simulator is composed of three major parts: a powerful computer, a PCI card, and a RF box. GPS navigation data and all the time varying signal parameters are calculated in a powerful computer depend on the receiver's operating environment. Then all information is provided to a digital Intermediate Frequency (IF) transmitter in real time for signal generating through PCI bus. After a D/A converter and a band-pass filter, the desired analog IF signal is obtained, then it is up-converted to the final L1 frequency.

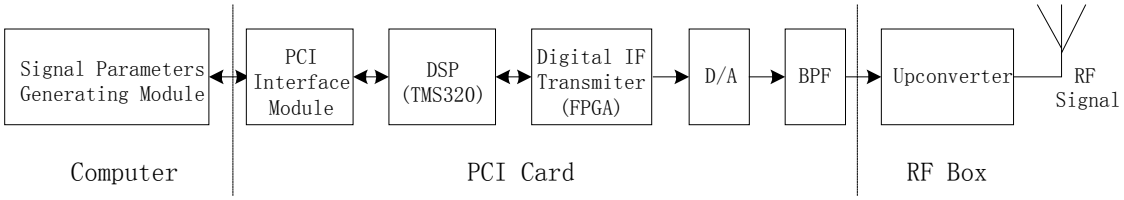

Fig.1 Overall Hardware Architecture Block Diagram of the Simulator

Block diagram of the proposed IF transmitter is shown in Fig.2. Clock Manager block provide a time base signal which trigger an interrupt for DSP at regular intervals, so navigation data and all the controlling parameters are updated periodically by writing and reading the corresponding register fill. C/A Code Generator generate the Gold sequence according the number of the selected GPS satellite, it is required that initial code phase can be set and the number of the

selected satellite can be changed. Code NCO synthesizes the oscillator required to drive the code generator. Epoch Counter keep track of the number of C/A code periods over a 1 second interval, and it also provides clock information to update the navigation data. The navigation data is spread with the C/A code and then passed through a low-pass filter to limiter the bandwidth, later modulated with a digital carrier by a BPSK modulator. Most function parts are implemented in a FPGA, and this allows for rapid reconfiguration.

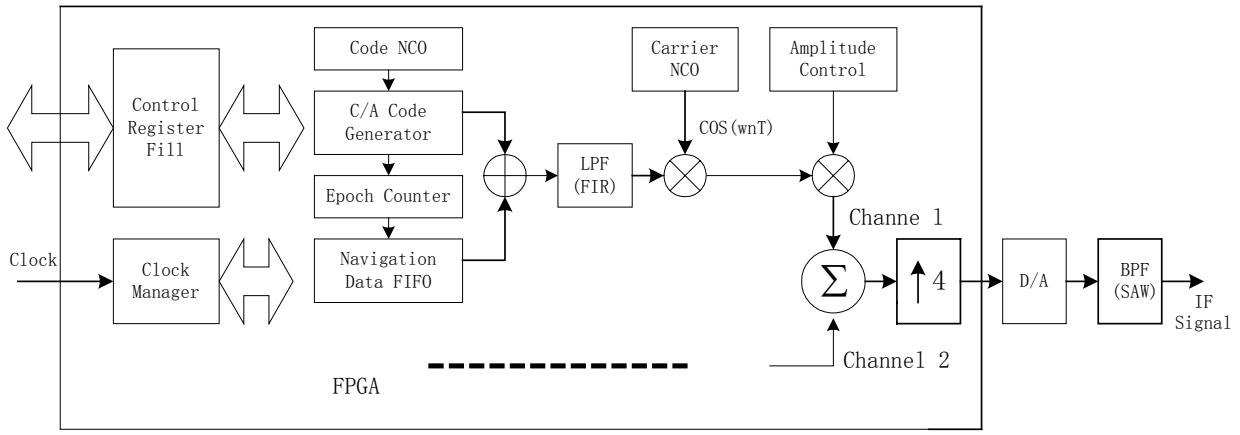

Fig.2 Block diagram of the proposed IF transmitter

Any timing delay error of one microsecond could lead to errors of hundreds of meters in the position process, so the reference clock should be highly precision and stabilized. In the present design a precision rubidium oscillator is adopted, the master clock of FPGA is obtained by using a PLL synthesizer. The nominal carrier frequency is f_1 = 4.58MHz, sampling frequency f_s = 20MHz, and the nominal code rate is 1.023Mcps. For a stationary observers, the maximum Doppler frequency shift caused by the movement of the GPS satellite is around ±5kHz. Suppose the maximum platform velocity is 10km/s (corresponding Doppler frequency shift of ±52.52kHz), then the totally Doppler frequency shift is about ±57.52kHz. The frequency scope of the baseband signal is about 4.58±(1.023+0.0576)MHz.

The D/A converting speed is upgraded to $4f_s$ = 80MHz, after upsampling and interpolation by a factor of 4. D/A converters introduce an inherent sin(x)/x amplitude distortion into the spectrum of signals being converted , this results from the sample-and-hold nature of it. The signal spectrum structure after D/A converter was showed in Fig.3.

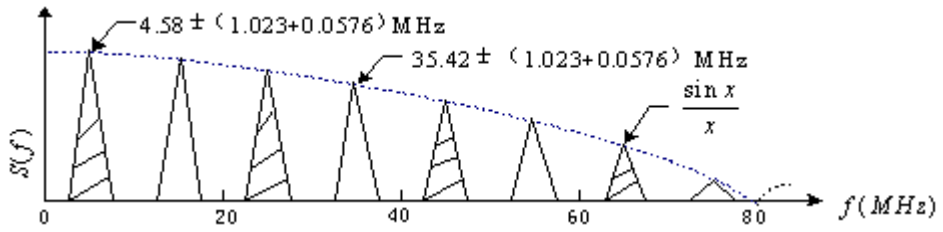

Fig.3 Signal spectrum structure after interpolation

As shown in Fig.3, the spectrum of the signal after interpolation includes not only the spectrum

of the original baseband signal but also some equally-spaced image spectra of the same form. So if the filter's center frequency is selected as (40 － 4.58)MHz=35.42MHz , and its pass-band-width [2×(1.023+0.0576)]MHz, then get the IF signal at the frequency range 35.42±(1.023+0.0576)MHz. Interpolation lower the operating speed of the digital circuits, less the roll-off effect on the band-fixed signal caused by the inherent sin(x)/x amplitude distortion of D/A converters. The frequency magnitude response for zero-order holds is given by

$$H(f) = \frac{\sin(\frac{\pi f}{f_s'})}{\frac{\pi f}{f_s'}} \qquad (2)$$

As a consequence, a continuous spectrum roll-off occurs at the IF bandwidth about 0.4dB.

The heart of the hardware design of a GPS signal simulator is the code generator, the ability to control the relative phase of them, and Doppler effects on the code and carrier. The phase and frequency controlling are realized by using numerically controlled oscillator (NCO) [3][4]. Both code NCO and Carrier NCO are working on the principle of direct digital frequency synthesizers. The difference is that the output of Carrier NCO is digital sine wave samples, where the output of code NCO is a square waveform.

Block diagram of Carrier NCO with FM chirp function was presented in Fig.4. Supposing the required extreme platform acceleration is 10g, the corresponding Doppler shift rate was 514.5Hz/s. If one were not to exceed a maximum pseudo range rate error of 0.005m/s (corresponding to a frequency error of 0.026Hz/s), then the required update rate for frequency controlling parameters should no less then 10μs according to the sampling theorem. Considering the computation ability and speed of the computer, the data exchange intervals between the computer and PCI card could not be too high, which is usually about 100ms. The more fast update rate of controlling parameters in the PCI card could obtain by using interpolation or FIFO (first-in-first-out). So the FM chirp function is very important for the dynamic performance of the simulator.

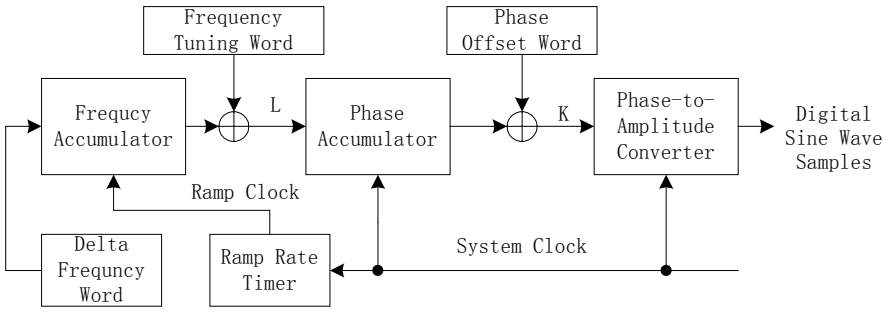

Fig4 Block Diagram of Carrier NCO with FM Chirp Function

Phase accumulator truncation is the most important source of distortion affecting the spurs performance in DDS. And the magnitude of the worst-case spurious response introduced by phase accumulator truncation, which was determined to be [5]

$$\zeta_{\max} = 2^{-K} \frac{\pi \frac{GCD(Fr, 2^{L-K})}{2^{L-K}}}{\sin[\pi \frac{GCD(Fr, 2^{L-K})}{2^{L-K}}]} \qquad (3)$$

where Fr is frequency tuning word, L is bit number of phase accumulator, K is the phase resolution of the sine function. GCD(F_r,2^{L-K}) denotes the greatest common divisor of F_r and 2^{L-K}. As the rule of thumb, the worst spurious signal introduced by phase truncation is approximately 6K[dB] below the desired output signal. In the digital carrier design, the frequency control word length is 32 bits, the phase resolution of the sine function is 15-bit, so the worst spurious signal introduced by phase truncation is approximately －90dB.

To achieve a positioning accuracy requirement of 10 m, the required ranging accuracy should be at 10/3 m rough order for a PDOP≈3, approximates to σ_r < 10 ns (σ_r denotes the root mean square error of the line-in-sight ranging), corresponding to 1% of one C/A code chip[6]. As a source signal, the performance requirement should be stricter. In the design, the code NCO has a 32bit frequency tuning word, a 16bit phase offset word, and the phase resolution is about $1/2^{16}$ of a C/A code chip.

TEST RESULTS

Using the Xilinx's FPGA (XC2V250), Analog Devices' 14bit D/A converters (AD9764), and a 35.42MHz surface acoustic wave (SAW) band pass filter (DW9255), a prototype was built, and 2 channel GPS signal was generated at IF for the first proof-of-concept testing. The generated signal was fed to a spectrum analyzer and the resulting spectrum is depicted in Fig.5, Fig.6, which were redrawing of the data recorded by AV4021 spectrum analyzer (made in China) in matlab. The same result was observed with a HP8591E spectrum analyzer. Fig.5 is a plot of the power spectrum of baseband signal after D/A converter, it has the nominal $(\sin x/x)^2$ envelope, the central frequency of the mainlobe is about 4.58MHz. Fig.6 is a plot of power spectrum of IF signal after band pass filter, now the central frequency of the mainlobe is about 35.42MHz, and the sidelobe is suppressed. Since the SAW DW9255 has an insertion loss about 17dB, the signal power become much less after the band pass filter.

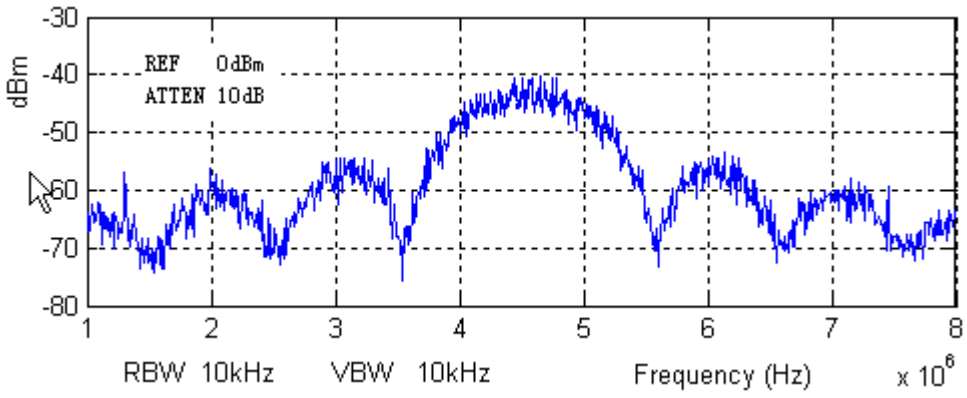

Fig.5 Power spectrum of baseband signal after D/A converter

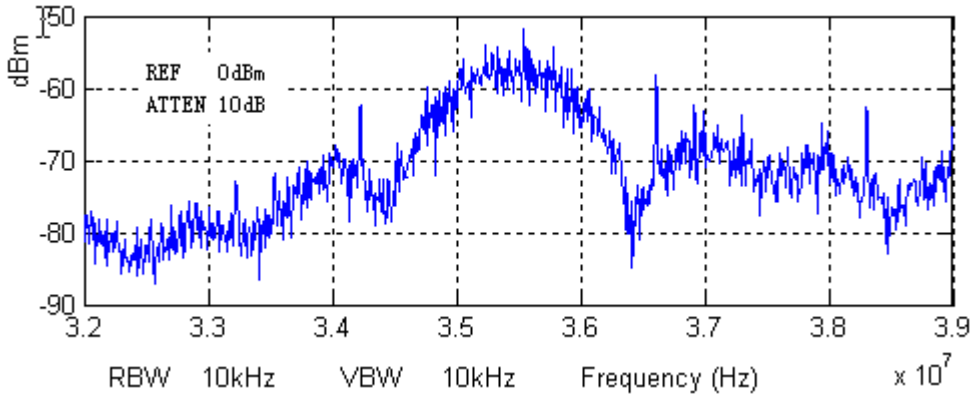

Fig.6 Power spectrum of IF signal after band pass filter

Next, a noise generator was used to reduce the signal-to-noise ration to simulate propagation loss, the IF signal was first combined with noise signal through a combiner, then the signal was attenuated by an adjustable attenuators, and fed to IF stage of a GPS receiver developed by ourselves (based on Zarlink's GP2000 chipset, center frequency of IF is 35.42MHz), the result showed that the receiver software could successfully acquire, track, and demodulated the navigation data simultaneously.

CONCLUSION

Using the techniques of digital signal processing such as direct digital synthesis and interpolation, the hardware architecture and design of the digital IF part of a multi-channel GPS simulator with highly agility is described in detail. Both the spreader and the BPSK modulator were implemented in digital method. To meet the dynamic performance requirement, NCO with FM chirp function and FIFO were extensively used in the design. The results of testing the proposed simulator hardware architecture at IF with the help of a GPS receiver developed by us are presented. With the help of the advanced EDA tool, the development period was greatly reduced.

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