SELECTABLE PERMUTATION ENCODER/DECODER FOR A QPSK MODEM

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ABSTRACT

An artifact of QPSK modems is ambiguity of the recovered data. There are four variations of the output data for a given input data stream. All are equally probable. To resolve this ambiguity, the QPSK data streams can be differentially encoded before modulation and differentially decoded after demodulation. The encoder maps each input data pair to a phase angle change of the QPSK carrier. In the demodulator, the inverse is performed – each phase change of the input QPSK carrier is mapped to an output data pair.

This paper discusses a very simple and unique differential encoder/decoder that handles all possible data pair/phase change permutations.

KEY WORDS

QPSK, Differential Encoding / Decoding, Data Ambiguity, Permutation .

INTRODUCTION

All coherent QPSK demodulators recover a local version (F'c) of the modulator's pre-modulation carrier (Fc). "A stable lock state can be achieved at any of four different phases [*phase angles between the two carriers*]: 0, $\pm$90 and 180." [1] The four lock states are equally likely to occur. In each of the lock states, the data output by the demodulator is a different function of the original modulation data.

A QPSK signal can be represented as two data streams (I and Q) modulating a carrier of frequency Fc Hz.. The I data modulates sin Fc, while Q data modulates cos Fc. The normalized output of the modulator is:

$$I \sin(Fc) + Q \cos(Fc).$$

I and Q have values of $\pm$ 1 volt depending on the logic state (0,1) of the input I and Q data. See Figure 1.

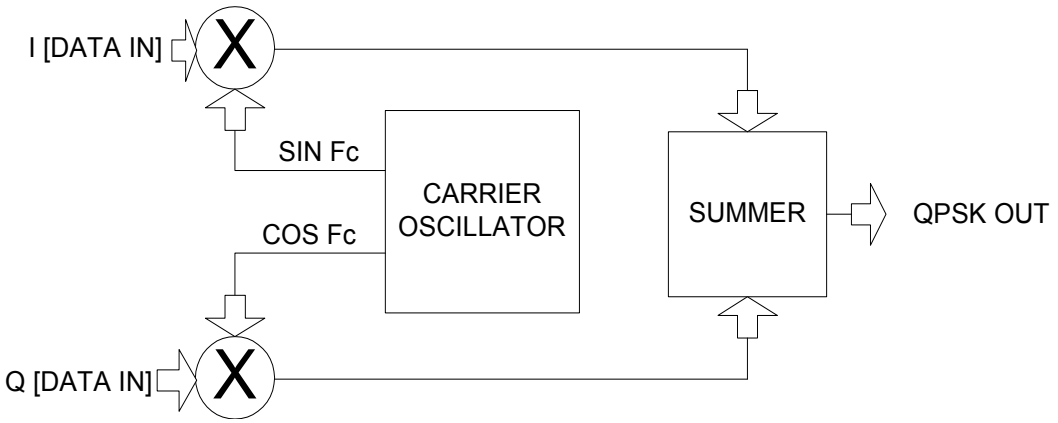

Figure 1. QPSK Modulator

QPSK demodulators have two outputs:

1. The input QPSK signal down converted by the recovered sin F'c.
2. The input QPSK signal down converted by the recovered cos F'c.

These outputs are called A and B, respectively. See Figure 2.

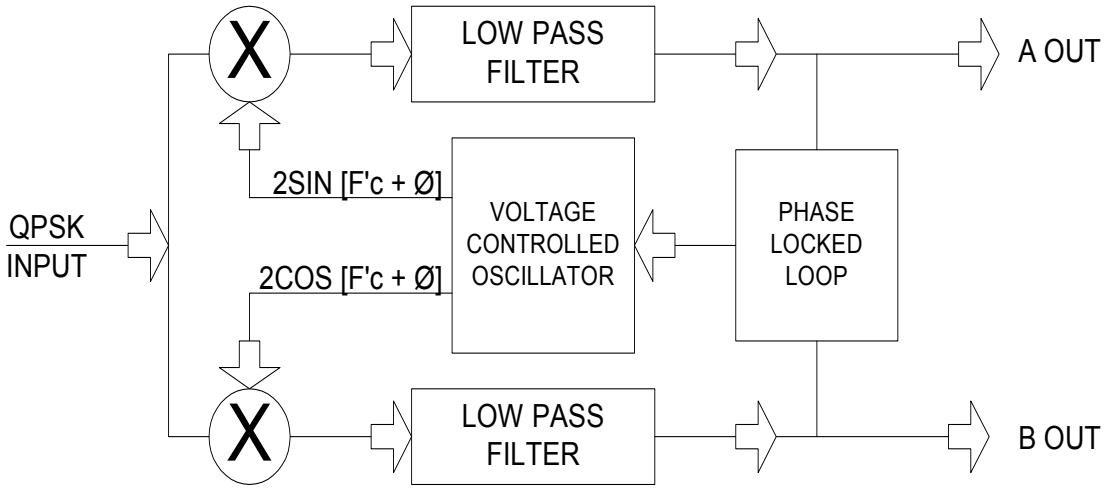

Figure 2. QPSK Demodulator

Because of the four lock states, either A or B can have a value of I, Q, -I or –Q. In all four lock states, some version of I and some version of Q will simultaneously be available at A and B. The data ambiguity of demodulator A,B vs modulator I,Q caused by the four lock states is shown in Table 1.

Table 1. Lock State Ambiguity

Lock State	A, B Output
0°	I, Q
90°	Q, -I
180°	-I, -Q
270°	-Q, I

See Appendix for proof.

" The ambiguity is not a defect of the squaring loop—or other carrier synchronizers—but is inherent to suppressed-carrier, phase-shift keying." [1].

THEORY OF OPERATION

As shown above, data ambiguity is an inherent, though undesirable, characteristic of QPSK demodulation. A differential encoder/decoder approach can be used to resolve this ambiguity. We may not know the absolute phase of the input QPSK signal, but we do know how many degrees it has moved since the last I/Q pair of data bits was transmitted. In differentially encoded QPSK, the transmitted signal phase changes a predetermined amount as a function of the input data pair. At the demodulator, the output data is a function of how much the input carrier phase has changed from one data pair to the next. A new data bit pair is output as a function of the amount of this phase change.

Differential encoding/decoding does have a drawback. The differentially encoded output data error rate is nominally twice the error rate in the channel. One error in the channel turns into two errors in the output data stream. This is because the amount of phase shift *to* the error phase state is the wrong value and the amount of phase shift *from* the error phase state is also the wrong value.

Refer to Figure 4 which illustrates a QPSK Constellation. This unit circle phasor diagram shows the four possible phases that the QPSK modulator can transmit. The phase states change as a function of input data (I,Q) bit-pairs.

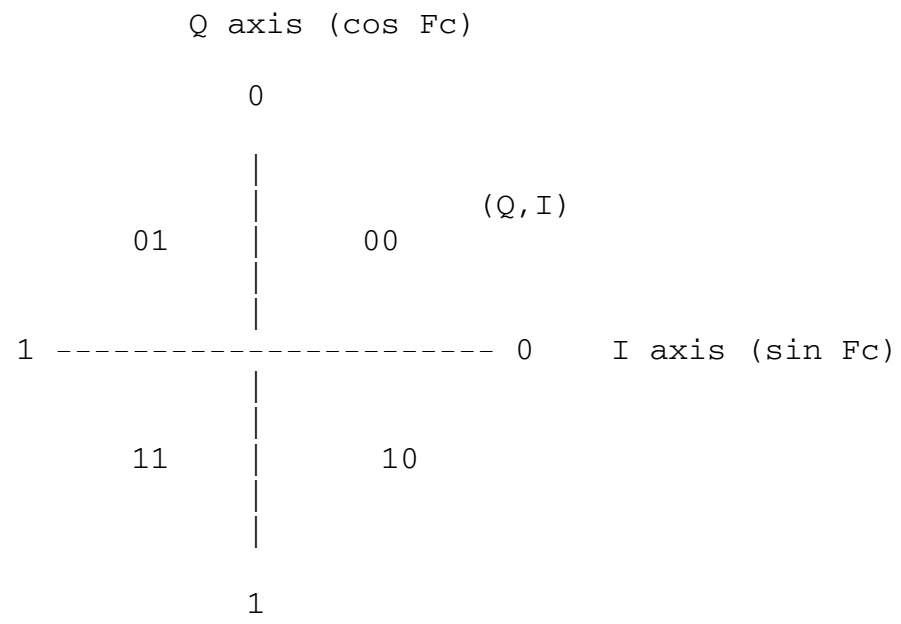

FIGURE 3 QPSK Constellation

Assigning the values of Q and I as shown above, the values of the four quadrants starting from upper right and going counter clockwise are 0,1,3,2. Table 2 shows how the four possible transmitted data combinations are output for each of the four lock states.

Table 2

----------B, A Output @ Demodulator For Each Lock State----------

Q,I Transmitted	0°	90°	180°	270°
00(0)	00(0)	10(2)	11(3)	01(1)
01(1)	01(1)	00(0)	10(2)	11(3)
11(3)	11(3)	01(1)	00(0)	10(2)
10(2)	10(2)	11(3)	01(1)	00(0)

Remember that when moving in a CCW direction, the quadrants of the unit circle phasor diagram are numbered 0, 1, 3 and 2. Notice that moving the transmitted phasor a given number of quadrants also moves the output phasor of any of the four lock state an equivalent amount. If the value of quadrants 2 and 3 were switched, we could use a standard adder for phase incrementing. The logic shown below in Figure 4, 3-to-2/2-to-3 Mapper, performs that function. Input values of 2 and 3 are output as 3 and 2 respectively. This logic block leads to the following (en/de)coder for a QPSK modem.

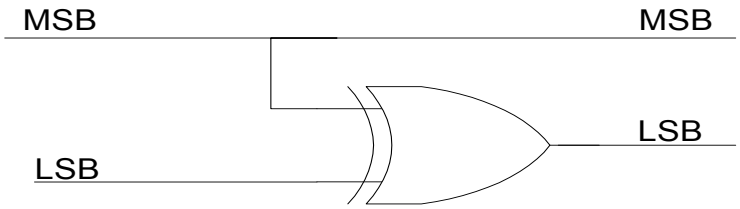

Figure 4 3-to-2/2-to-3 Mapper

Refer to Figure 5 illustrating a Permutation Encoder for a QPSK Transmitter. The left-most block, Map Input Data Bits to Phase Change, is a look-up table that maps the four possible QI data pairs to a unique phase change. An output value of 0 causes a 0° phase change, 1 causes a 90°change, 2 cause a 180° change and 3 causes a 270°change. In our application, the mapping is not fixed and can be set to any of the 24 possible input-data-to-phase-change permutations. Twenty four mappings/permutations occur because there are four possible data bit-pairs [00,01,10,11] and each of them can correspond to one of the four possible phase change values [0, 90, 180, 270]. There are 24 permutations when four items are taken four at a time. The mapping block is a combination of an eight bit register and a two-bit wide, one-of-four mux. The host computer writes an eight bit word to the register. Bits 1,0 set the phase change for when the QI data bits are equal to 00. Bits 3,2 set the phase change for when the QI data bits are equal 01. Bits 5,4 set the phase change for when the QI data bits are equal to 10 and Bits 7,6 set the phase change for when QI data bits are equal to 11. Register bits 1,0 are present at mux input #0. Bits 3,2 are present at mux input #1. Bits 5,4 are present at mux input #2. Bits 7,6 are present at mux input #3. The QI data bits are used to select the mux input. Depending on the values of the QI data bits, a desired phase change value is input to the 2 bit adder at the A input. It can be seen that this phase change value is added to the present phase (B input). The value of the current phase state is increased by an amount that is a function of the QI data input. The output of the Adder is the new current phase state. The fact that the phase values count in a 0, 1, 3, 2 sequence is handled by the 3-to-2 / 2-to-3 mapping block. The mapper outputs are level shifted to be bipolar and then input to the sin Fc and cos Fc multipliers.

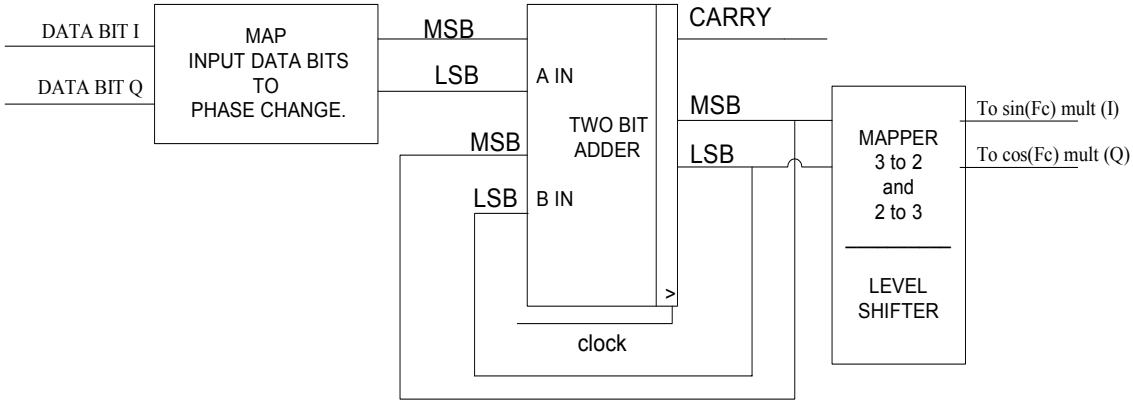

Figure 5 Permutation Encoder for a QPSK Transmitter

The Permutation Decoder for a QPSK Demodulator is shown in Figure 6. The demodulator decoder is basically the reciprocal of the modulator encoder. The bipolar multiplier outputs are level shifted to TTL and then mapped 3-to-2/2-to-3. The four phases are now represented by values of 0, 1, 2 and 3 corresponding to phases of 0, 90, 180 and 270, respectively. These binary versions of the phase are clocked through a two-bit wide flip-flop so that both the current and previous phase are simultaneously available. The modulator's adder is replaced by a subtractor (A-B) which is the next step in the decoding. The previous phase is subtracted from the current phase and the phase difference is output from the subtractor. It is a three bit subtractor with fixed MSBs to account for wrap around. On a bit-pair by bit-pair basis, the output of the subtractor is the change in carrier phase. This phase change value goes to a mapper that converts phase change to output bit-pair. While the mapper can be a fixed look-up table , this approach is more flexible. Like the modulator encoder, an 8 bit word from the host computer is input to the mapper. This allows one to make the output bit-pairs correspond to any one of the 24 possible permutations.

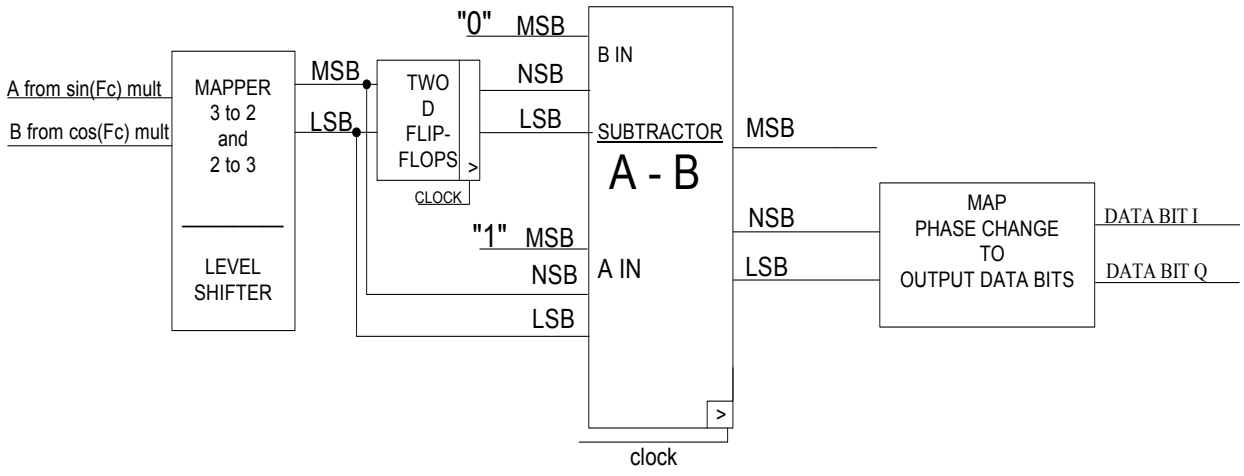

Figure 6 Permutation Decoder for a QPSK Demodulator

CONCLUSION

Differential Encoding in QPSK has been utilized for many years. Originally, a QPSK modem would have a fixed mapping of "data bits in to phase change out" at the modulator and "phase change in to data bits out" at the demodulator. Later QPSK modems would have a permutation selector (with choices 00 to 24) at both ends. These selectors used cumbersome logic or look-up tables for the mapping.

The approach in this paper simplifies the design. The novelty of this design is the renumbering of the phasor diagram quadrants which allows adders and subtractors to be used for the mappings.

REFERENCE

[1] Gardner, F. M., Phaselock Techniques, 2nd Edition, John Wiley & Sons, Inc., 1979.

APPENDIX

DATA AMBIGUITY IN A QPSK DEMODULATOR

The following is a proof of how the four lock states of the QPSK Costas demodulator affects the demodulator A and B data outputs.

The original signal from the modulator is:

$$I\sin(Fc) + Q\cos(Fc).$$

I and Q have values of +- 1v depending on the logic state (1,0) of data inputs.

In Figure 2, the recovered carrier has a frequency of F'c. The modulator frequency is Fc. When in lock, , F'c and Fc are equal. F'c is only used in the first equation to illustrate where a specific signal was developed. After that, Fc is used for F'c.

1. Setting the Demodulator LO Phase = 0°

The A signal output of the demodulator in Fig. 2 is:

$$2\sin[F'c + 0°] \times [I\sin(Fc) + Q\cos(Fc)]$$
$$= I\cos[Fc-Fc] - I\cos[2Fc] + Q\sin[2Fc] + Q\sin[Fc-Fc]$$
$$= I.$$

In the last step, the 2Fc terms were eliminated by the low pass filter. Cos0 °= 1 and sin0° = 0, so those terms were set accordingly.

The B signal output of the demodulator in Fig. 2 is:

$$2\cos[F'c + 0°] \times [I\sin(Fc) + Q\cos(Fc)]$$
$$= I\sin[2Fc] - I\sin[Fc-Fc] + Q\cos[2Fc] + Q\cos[Fc-Fc]$$
$$= Q.$$

For Costas demodulator locked in the 0° state, the A output is the I signal from the modulator and the B output is the Q signal from the modulator.

2. Setting the Demodulator LO Phase = 90°

The A signal output of the demodulator is:

$$2\sin[F'c + 90°] \times [I\sin(Fc) + Q\cos(Fc)]$$
$$= 2\cos[Fc] \times [I\sin(Fc) + Q\cos(Fc)] \quad (1)$$
$$= I\sin[2Fc] - I\sin[Fc-Fc] + Q\cos[2Fc] + Q\cos([Fc-Fc]$$
$$= Q \quad (2)$$

In step (1), trig identity sin[x +90°] = cos x was used.

In step (2), the 2Fc terms were eliminated by the low pass filter also, cos0° = 1 and sin0°= 0, so those terms were set accordingly.

The B signal output of the demodulator is:

$$2\cos[F'c + 90°] \times [I\sin(Fc) + Q\cos(Fc)]$$
$$= 2 \times -\sin[Fc] \times [I\sin(Fc) + Q\cos(Fc)] \quad (1)$$
$$= -I\cos[Fc-Fc] + I\cos[2Fc] - Q\sin[2Fc] - Q\sin[Fc-Fc]$$
$$= -I \quad (2)$$

In step (1), $\cos[x + 90°] = -\sin x$ was used.

For Costas demodulator locked in the 90° state, the A output is the Q signal from the modulator and the B output is the -I signal from the modulator.

3. Setting the Demodulator LO Phase = 180°

The A signal output of the demodulator is:

$$2\sin[F'c + 180°] \times [I\sin(Fc) + Q\cos(Fc)]$$
$$= 2 \times -\sin[Fc] \times [I\sin(Fc) + Q\cos(Fc)] \quad (1)$$
$$= I\cos[2Fc] - I\cos[Fc-Fc] - Q\sin[2Fc] - Q\sin[Fc-Fc]$$
$$= -I$$

In step (1), $\sin[x + 180°] = -\sin x$ was used.

The B signal output of the demodulator is:

$$2\cos[F'c + 180°] \times [I\sin(Fc) + Q\cos(Fc)]$$
$$= 2 \times -\cos[Fc] \times [I\sin(Fc) + Q\cos(Fc)] \quad (1)$$
$$= -I\sin[2Fc] + I\sin[Fc-Fc] - Q\cos[2Fc] - Q\cos[Fc-Fc]$$
$$= -Q$$

In step (1), $\cos[x +180°] = -\sin x$ was used.

For Costas demodulator locked in the 180° state, the A output is the -I signal from the modulator and the B output is the -Q signal from the modulator.

4. Setting the Demodulator LO Phase = 270°

The A signal output of the demodulator is:

$$2\sin[F'c + 270°] \times [I\sin(Fc) + Q\cos(Fc)]$$
$$= 2 \times -\cos[Fc] \times [I\sin(Fc) + Q\cos(Fc)] \quad (1)$$
$$= -I\sin[2Fc] + I\sin[Fc-Fc] - Q\cos[2Fc] - Q\cos[Fc-Fc]$$
$$= -Q$$

In step (1), $\sin[x + 270°] = -\cos x$ was used.

The B signal output of the demodulator is:

$$\begin{aligned} & 2\cos[F'c + 270°] \times [I\sin(Fc) + Q\cos(Fc)] \\ = 2 \times \sin[Fc] & \times [I\sin(Fc) + Q\cos(Fc)] \qquad (1) \\ & = -I\cos[2Fc] + I\cos[Fc-Fc] + Q\sin[2Fc] + Q\sin[Fc-Fc] \\ & = I \end{aligned}$$

In step (1), $\cos[x + 270°] = \sin x$ was used.

For Costas demodulator locked in the 270° state, the A output is the -Q signal from the modulator and the B output is the I signal from the modulator.

The A,B outputs for all of the lock states were shown in Table 1, which is repeated below.

Table 1. Lock State Ambiguity

Lock State	A, B Output
0°	I, Q
90°	Q, -I
180°	-I, -Q
270°	-Q, I