A PROGRAMMABLE DUAL MODULATOR TESTBED FOR MIMO APPLICATIONS

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ABSTRACT

Multiple-input multiple-output (MIMO) systems use multiple transmitters and receivers to increase the capacity and reliability of radio frequency communication links used in multipath and disruptive environments. This paper describes a recently designed hardware testbed that can be used as a modulator and transmitter for MIMO systems which use two transmitters. The testbed consists of a field programmable gate array (FPGA) that generates the I/Q baseband signals for the two transmitters. A wide variety of modulation and coding formats, up to data rates of 10 Mbps, can be implemented by reprogramming the FPGA. The dual I/Q outputs from the FPGA are then fed to a pair of quadrature modulators, which have programmable carrier frequencies from 1,025 to 2,450 MHz. The system is implemented on a single printed circuit board, and has dual RF outputs with programmable power levels up to 0 dBm.

INTRODUCTION

There has been a substantial amount of research in the past few years on the use of MIMO systems [1-4]. By using multiple antennas at both the transmitter and receiver, these systems can either achieve higher throughput, or higher reliability, than traditional single-antenna systems or beamforming systems. However to see these gains, one must be able to carefully control and coordinate the signals generated by each transmitter. There are a variety of methods for performing MIMO modulation, and it is not always clear which technique will work best in any given situation. It would be convenient to have a test bed that would allow the user to quickly reprogram the transmitters. Ideally, such a test bed would be reasonably small, to allow it to be used in typical telemetry applications. This paper describes the development of such a test bed. Since it will accommodate two transmit antennas, it was given the name dual-antenna radio-transmitter (DART).

A high level block diagram of the DART board is shown in Fig. 1. The DART system will allow transmission of data up to 1 Mbit/sec. The data is read into an Altera® Cyclone II field programmable gate array (FPGA). The user can program, and then reprogram, the FPGA to

implement a variety of MIMO modulation formats. Provided there is sufficient space on the FPGA, it would also be possible to implement source compression, encryption and forward error correction algorithms.

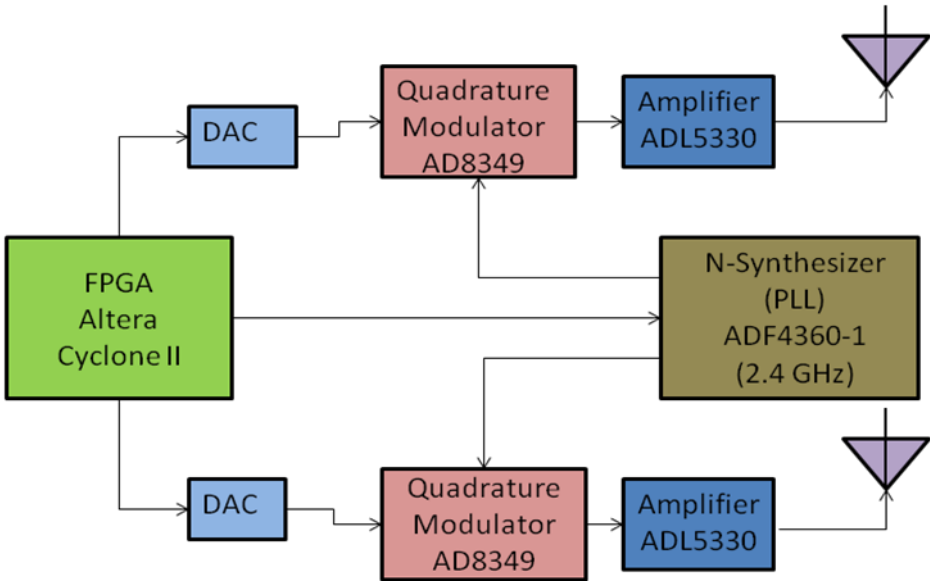

Figure 1. High Level Block Diagram of DART Board

The output of the FPGA consists of four digital data streams, each 14 bits wide. The output streams are fed to a pair of dual, 14-bit digital to analog converters (DAC) made by Texas Instruments® (DAC2904). These DAC each produce a pair of differential analog signals which are treated as in-phase and quadrature-phase (I/Q) signals. These signals are properly conditioned, and sent to an Analog Devices® AD8349 quadrature modulator. The output of each modulator is amplified by an ADL5330 RF amplifier, before final termination into a 50 Ω antenna. A detailed block diagram of the DART board is shown in Fig. 2.

Radio transmission capabilities are built upon a simple quadrature modulation scheme in which a pair of differential baseband I/Q signals, separated by a 90 degree phase shift, are multiplied by a carrier signal and are then combined to produce a resulting RF signal. The DART's quadrature modulators receive the carrier frequency from an Analog Devices® ADF4360-1 N-synthesizer, which serves as a programmable phase-locked-loop (PLL). A variety of carrier frequency ranges can be attained through utilization of pin-compatible ICs within the ADF4360 family.

CIRCUIT EXPLANATION

A set of schematics for the entire DART board is presented in Figures A1 - A6 in the appendix. The limited resolution of these figures may make it difficult to view some details. A high-resolution schematic can be obtained by contacting any of the authors. The remainder of this section discusses many of the design decisions made when laying out this circuit.

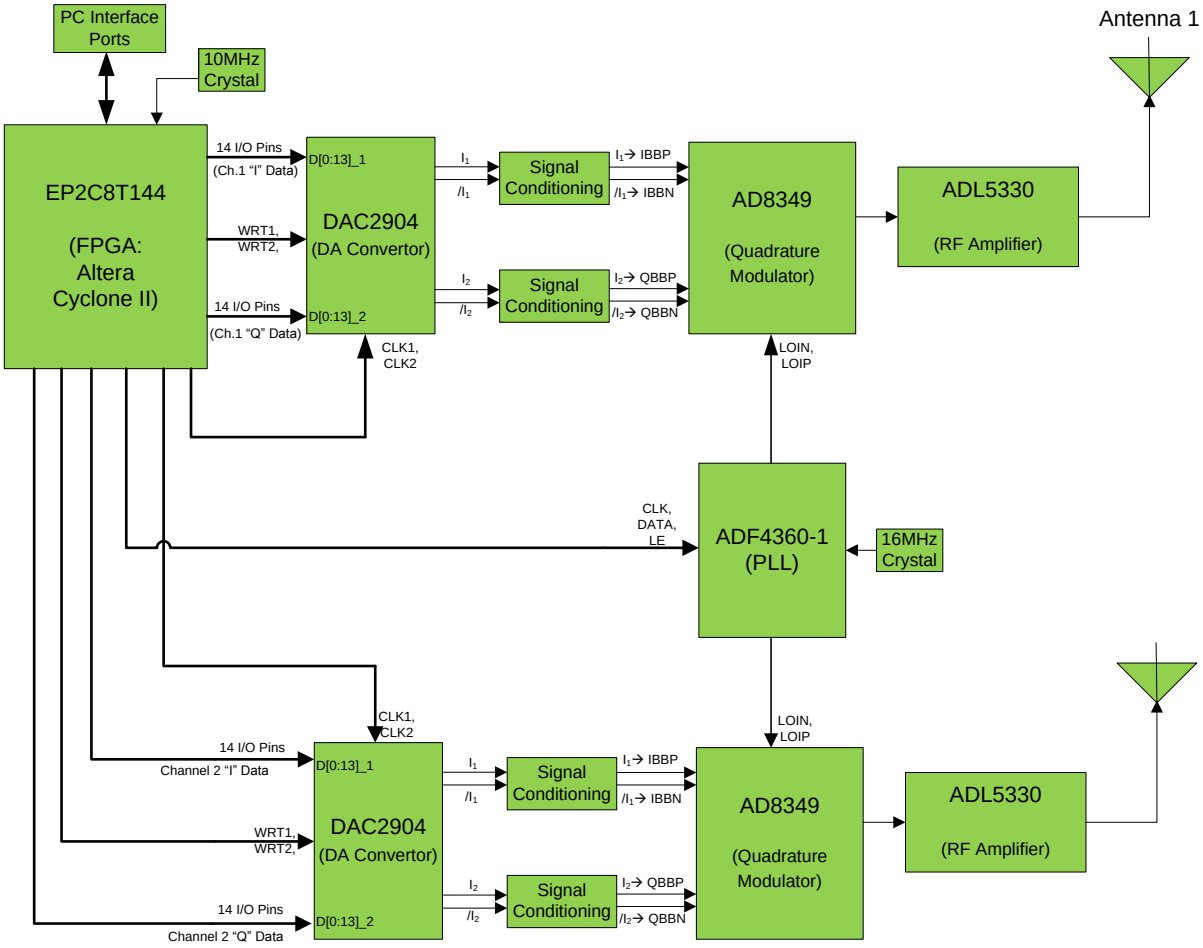

Figure 2. Detailed DART Block Diagram

Two 10-pin headers allow programming of the FPGA by either JTAG or AS serial interfaces, respectively. Either header can be used in conjunction with a standard Altera® USB-Blaster programming device. Programming of the Cyclone II via JTAG is volatile (i.e., the board must be re-programmed if powered off), whereas non-volatile AS programming stores program data in a 4MB flash chip. Jumpers are used to set the programming mode.

Three I/O pins connect the FPGA to the ADF4360-1's serial-peripheral interface (SPI) for PLL initialization. A 10MHz oscillator provides an external reference frequency to simplify programming. All remaining I/O pins are connected through 22Ω resistors to the DAC's digital input pins.

Each analog output of the DAC2904 requires a characteristic impedance of 50Ω. Therefore, 50Ω termination resistors are used to convert the DACs' differential current outputs to a usable form. The analog outputs are AC-coupled and DC biased to 400mV using a resistor divider network as required by the AD8349 modulator.

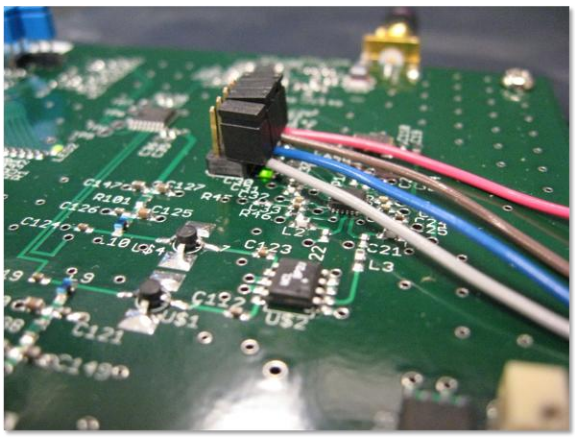

Figure 3. Programming Connection for FPGA

A jumper block allows for manual bypassing (see Fig. 3) of the FPGA's connection to the ADF4360-1. This enables the ADF4360-1's SPI interface to be externally interfaced. Some 100Ω resistors and 0.1µF capacitors provide buffering and input protection. The differential outputs of the PLL are AC-coupled as recommended in the ADF4360-1 datasheet. Because both AD8349 modulators require a differential oscillator input, each output of the PLL is connected to a 50Ω power splitter and RF amplifier before connecting to a modulator. An LED is connected to the ADF4360-1's "muxout" pin, which can be programmed to send a high signal when the PLL achieves a frequency lock.

The ADL5330 features differential RF inputs and outputs, while the AD8349 modulator outputs are single-ended. This interface issue was easily resolved by AC-coupling the negative differential input to ground. For the ADL5330's output, a 50Ω balun transformer resolves the same issue by converting the differential output into a single-ended form for connection to a 50Ω antenna. A trim-pot resistor and unity-gain operational amplifier configuration allow the voltage input to the ADL5330 "gain" pin to be controlled from 0-1.25V, thereby allowing for manual adjustment of the output power at each antenna.

Power is delivered to the DART using an external 5V, switching AC-to-DC power supply. Diode protection and linear regulators are used to step down the voltage to separate digital and analog +3.3V and +1.2V supplies. Bulk and surface mount decoupling capacitors are generously placed throughout the circuit.

PRINTED CIRCUIT BOARD LAYOUT

The DART was designed on a standard 62 mil, 4-layer PCB stackup with 1oz copper traces, as shown in Fig. 4. Because five DC voltage levels are used throughout the DART's circuit, power traces are routed in layer 4 and rely on well-placed decoupling capacitors instead of a power/ground plane pair. All analog signal trace widths are set to 16.299 mils to achieve the desired trace characteristic impedance, $Z_0 = 50\Omega$.

Layers 2 and 3 consist of solid ground planes, which avoids complex ground return paths caused by split plane techniques. Vias are placed at 5mm intervals throughout the board to minimize impedance between the separate ground planes. Vias connecting surface mount components to ground are placed as closely to the component pads as possible in order to reduce parasitic inductance. For the same reason, passive components connecting to RF signal traces were placed as closely as possible, or directly upon the signal trace.

The front and back of the assembled board is shown in Fig 5 and Fig 6 respectively.

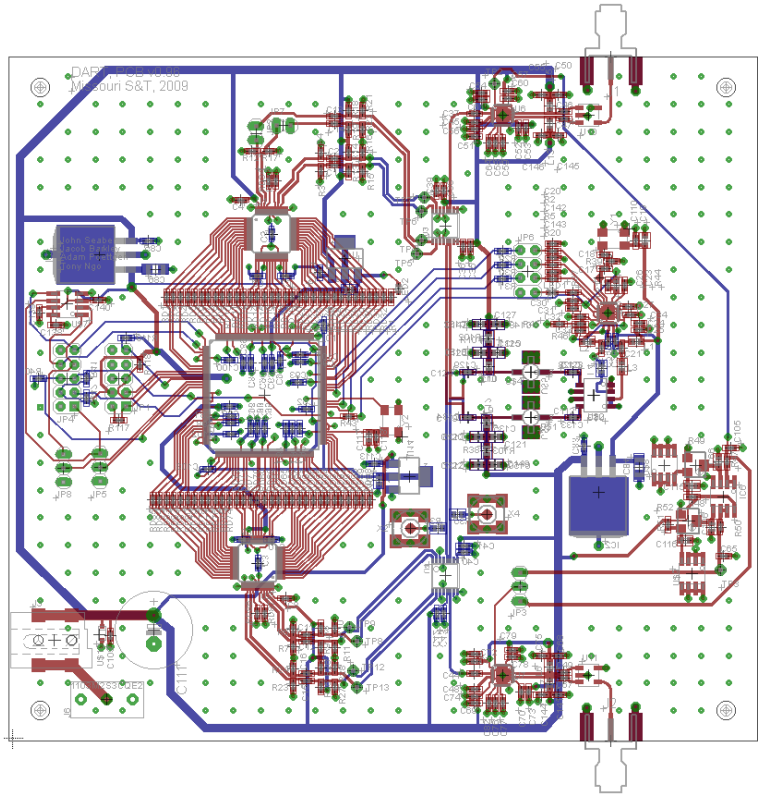

Figure 4. DART Printed Circuit Board Layout

PROGRAMMING

The Verilog hardware description language is used for all FPGA coding. To generate signals, the FPGA reads data points from a pre-made text file. One data point is read at each rising edge of an external 10MHz oscillator. Therefore, the number of data points in a list is directly proportional to the frequency of the output signal. Test signals can be created with Matlab® or equivalent tools, then quickly compiled and programmed to the FPGA via the Altera® Quartus II software.

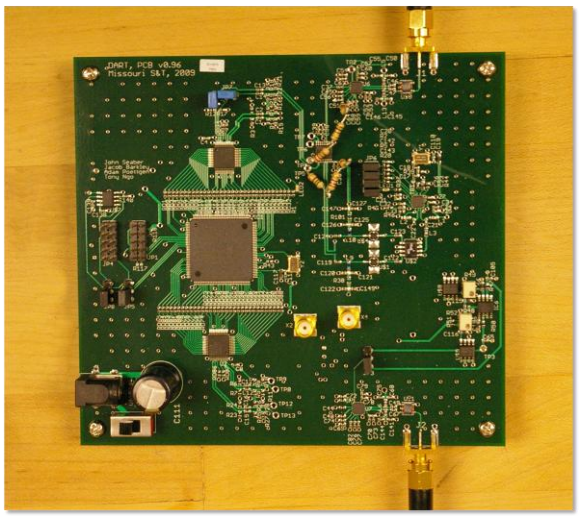

Figure 5. Front of Assembled PCB

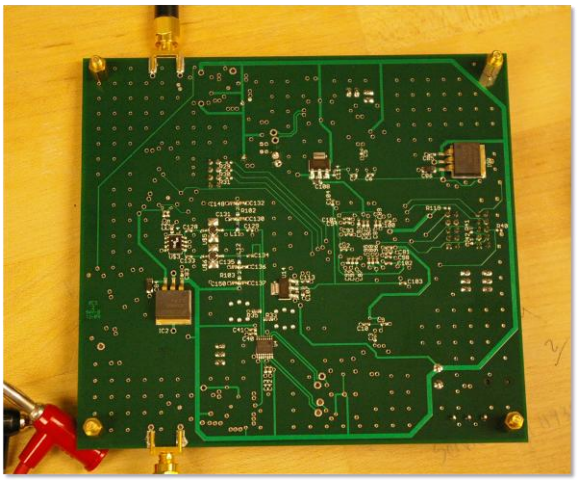

Figure 6. Rear of Assembled PCB

The DART PLL must be initialized through a 3-wire serial-peripheral interface (SPI) each time the board is powered on. The ADF4360-1 reads three sets of 24-bit data, each followed by a high pulse on the latch pin. These three latches (and preceding data) set chip operating parameters, such as frequency and output power. Without proper initialization, the PLL cannot achieve a frequency lock. Thus, the FPGA is programmed to produce the necessary SPI initialization routine prior to outputting the programmed periodic signals.

CHALLENGES

Two major difficulties were encountered during development and testing of the DART:

1. PLL Initialization: Initializing the PLL directly from the FPGA was unreliable, even though it appeared to be presented with the appropriate SPI waveform. Using manufacturer-provided evaluation software for the ADF4360-1 with the DART's external SPI bypass jumpers, the PLL achieved a frequency lock during several test sessions. Future experimentation is planned by cutting traces on the PCB and supplying an external, differential 2.4GHz signal into two SMA jacks.

2. Power Splitters: Each modulator requires a differential oscillator input, but a single ADF4360-1 chip can only provide one differential oscillator signal. Parallel signal connections are not practical at 2.4GHz, so 50Ω power splitters are used to split the PLL signal. Series +8.9dBm RF amplifiers are placed after each splitter output to make up for the 3-6dBm signal loss. Exact output can later be programmed through the ADF4360-1 to achieve the target oscillator input power of -6dBm into each AD8349.

CONCLUSIONS

The foundation of the DART has been successfully built. An FPGA/DAC hardware platform and software are fully operational for generation of dual I/Q baseband signals for transmission to dual quadrature modulators. Limited PLL chip functionality, however, deems modulated signal transmissions inoperable. As a result, the modulators and RF amplification stages of the device have not been tested. In the future, the DART's radio transmission capabilities can be tested by manual insertion of a 2.4GHz oscillator signal.

REFERENCES

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[3] D. Tse and P. Viswanath, *Fundamental of Wireless Communication*. New York, NY: Cambridge University Press, 2005.

[4] A. Goldsmith, *Wireless Communications*. New York: Cambridge University Press, 2005.

APPENDIX - SCHEMATICS

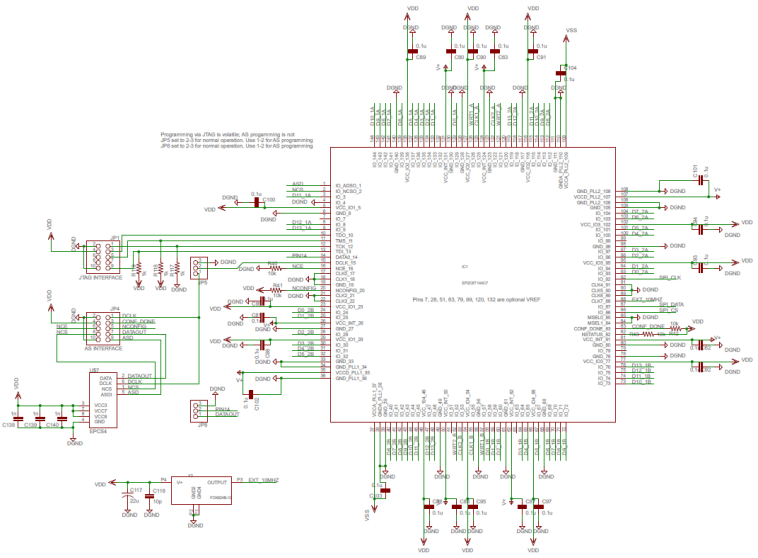

Figure A1. Power Supply and FPGA Schematic

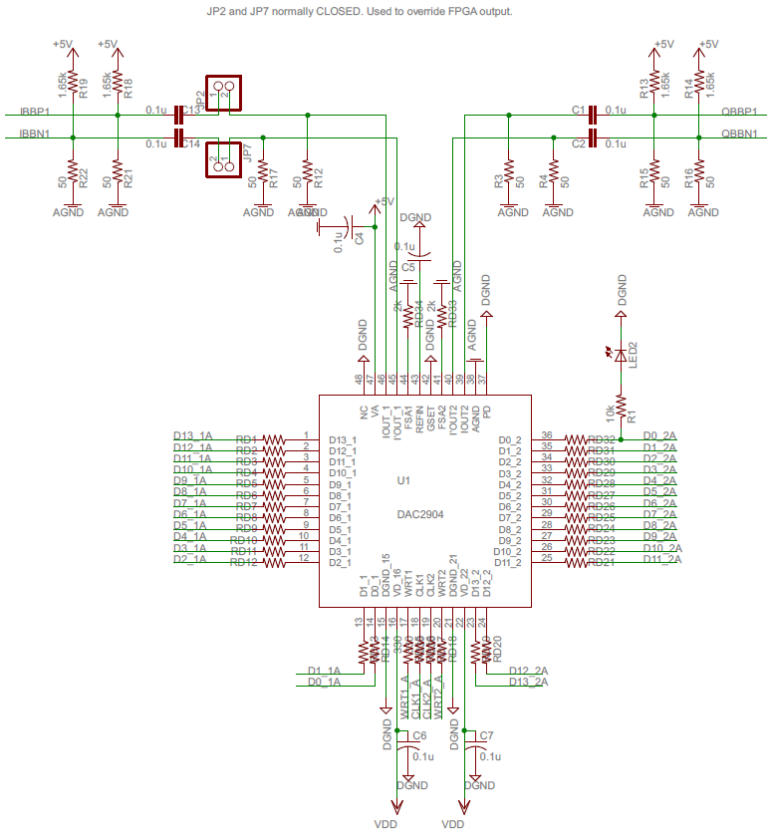

Figure A2. Digital to Analog Converter Schematic

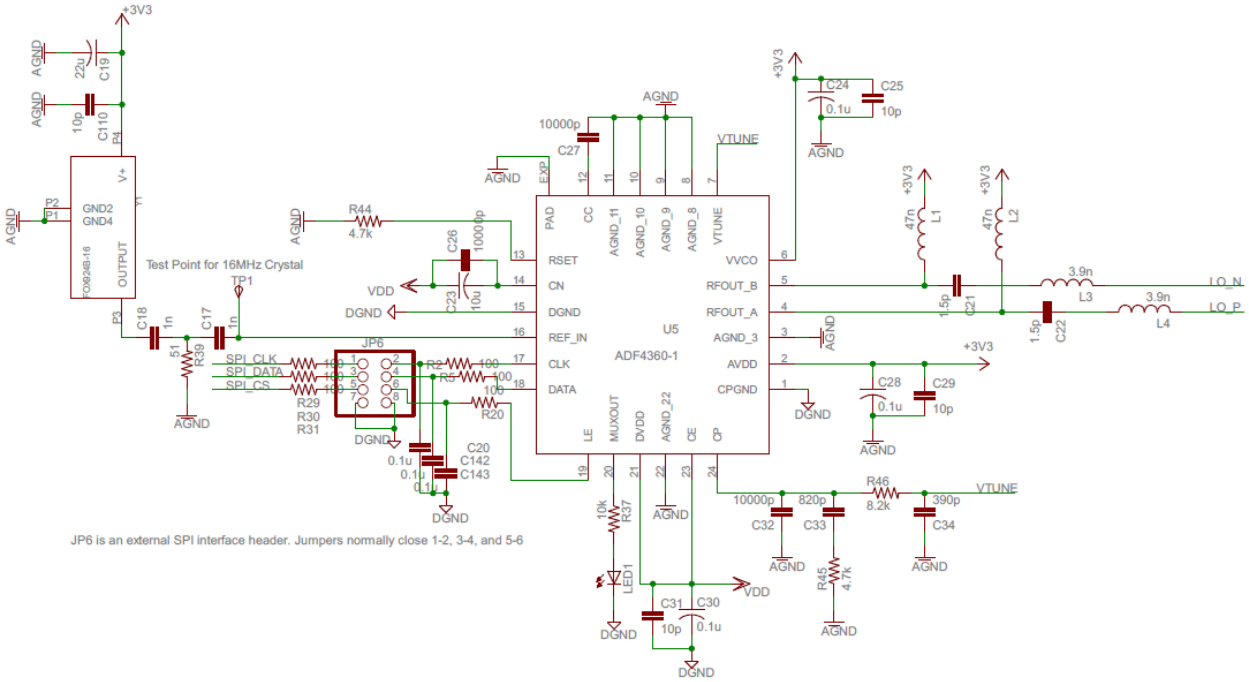

Figure A3. PLL Schematic

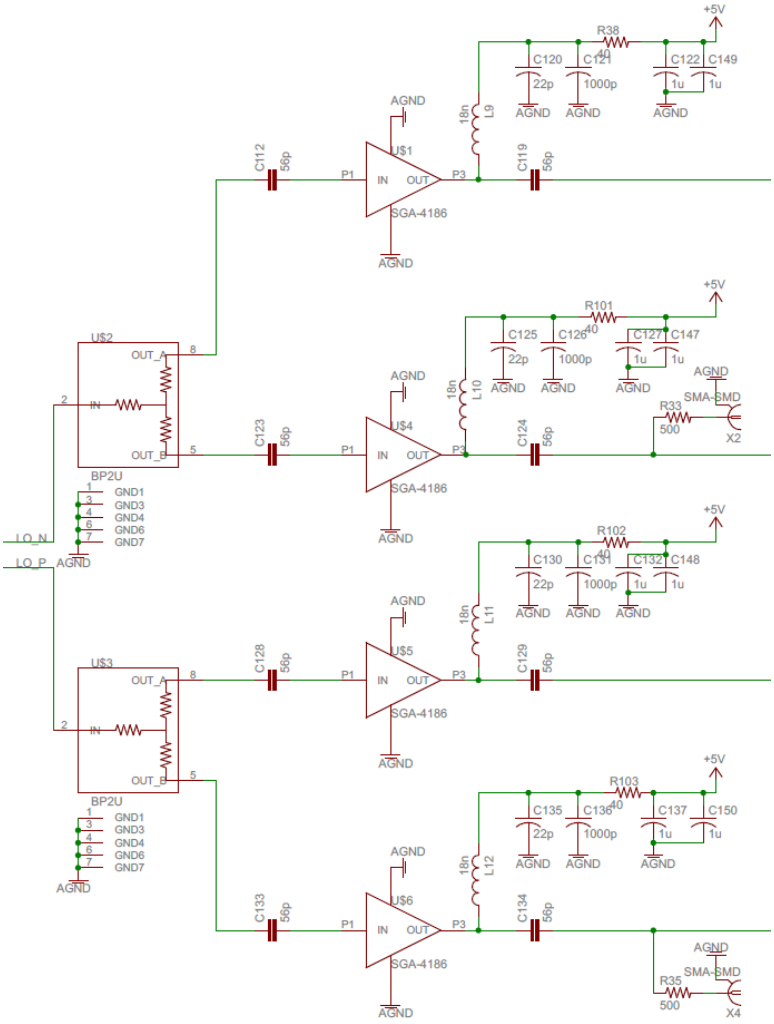

Figure A4. Power Splitter Schematic

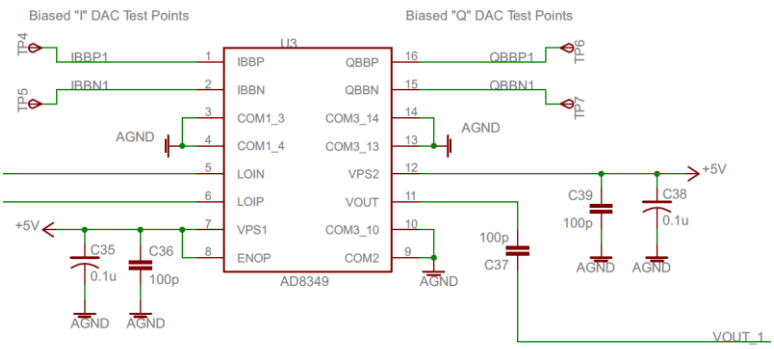

Figure A5. Modulator Schematic

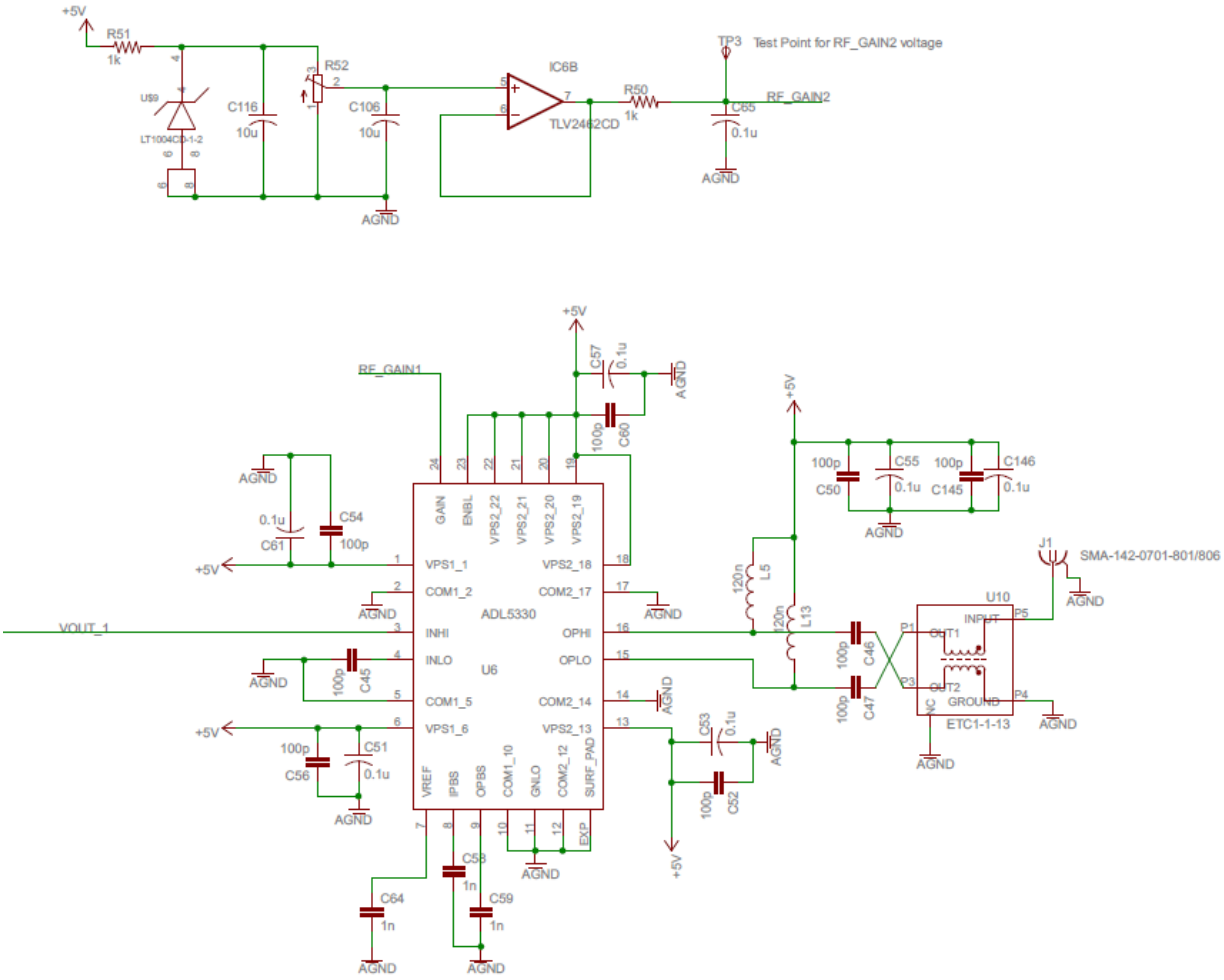

Figure A6. RF Amplifier Schematics