THE TECHNOLOGY OF DBPSK MODULATION-DEMODULATION FOR TELECOMMAND IN REMOTE CONTROL TEST SYSTEM

By

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Abstract

This design adopts the software radio and DBPSK（Differential Binary Phase Shift Keying）modulation-demodulation, which detects the telecommand receiving by the guided-missile system correctly. The DBPSK modulation module in Altera FPGA chip converts the binary telecommand into DBPSK signal, which will be frequency modulated after D/A conversion. In the receiver, the FM signal is demodulated and A/D converted before sending to the FPGA. The DBPSK demodulation module in FPGA finally gets the telecommand which will be tally with the telecommand from transmitter. At last, the whole DBPSK modulation-demodulation module is embedded into the remote control test system. The design is working properly and meeting the requirements of the test system.

Key Words: DBPSK modulation-demodulation, FPGA, Software Defined Radio

INTRODUCTION

The main the function of this design achieves the DBPSK Modulation-demodulation for Telecommand in Remote Control Test System.

Compared with the other binary digital modulation, PSK(Phase Shift Keying) be applied extensively in satellite communications、land mobile service、measurement

and control data link communications and so on because of its characteristic such as strong noise resistance、better data rate-to-bandwidth ratio、power-efficient and easy to hardware implementation.[1]

Binary digital phase modulation has two types of modulation：the CBPSK（Coherent Binary Phase Shift Keying）whose controlled carrier signal changes with the base-band changes and the DBPSK whose phase difference between the contiguous before and after carrier indicate the baseband signals (Differential Binary Phase Shift Keying). Compared with the CBPSK, DBPSK can avoid the phenomenon of Inverted Π and its hardware implementation is easy . Take into account the two points above, this design adopts the DBPSK Modulation-demodulation for Telecommand in Remote Control Test System.

The term "Software Defined Radio" was coined in 1991 by Joseph Mitola, who published the first paper on the topic in 1992.Its core idea is to structure a common hardware platform with open、standardized、modularized.There are three types of digital hardware to achieve: ASIC (Application Specific Integrated Circuit)、FPGA(Field Programmable Gate Array)、DSP(Digital Signal Processor).Compared with the other two types, the FPGA internal be rich in resources that can be configured kinds of circuit block and designed more parallel modules system ,and it has the characteristics of high speed computing power、high reusable and integrated IP(intellectual property) core. Take all factors into consideration, this design adopt a implementation scheme about digital signal processing ,which is based on the technologies of SOPC(system on a programmable chip)、EDA(electronic design automation) and FPGA. [2]

BODY

1.1 General descriptions of DBPSK modulation-demodulation structure

There is the software designing structure of the DBPSK modulation-demodulation as shown in figure 1.1.The whole system is driven by the 10MHz external crystal oscillator. The clocked signal generator module will convert the 10MHz clocked signal into square wave signal with frequency f1(307.2KHz) which will drive almost all the modules bellowed.

In the part of the DBSPK Modulation, the frequency f1 will be converted into frequency f2(2.4KHz) with which the difference code module will produce the difference code and the binary useful information(data_out1) that are all with the frequency f1(307.2KHz). And then, with the input of f3(12KHz) sine wave which is produced by the sine wave generator and the input of the binary useful information(data_out1), the decide A module will produce the DBPSK signal A with the frequency f3(12KHz).

In the part of the DBSPK Demodulation, the DBPSK signal B which is converted by the A/D converter, which will be multiplied by itself that has one code width latency time. Then the result output from the multiplier will be filtered by Low-pass filter which is adopted an FIR (Finite Impulse Response) IP core, the MSB(most

significant bit) of the filter's output will be processed by the DPLL(Digital Phase-Locked Loop) module and the Decide B module respectively. At the end, this part will get the bit synchronization and the binary useful information named data_out2.

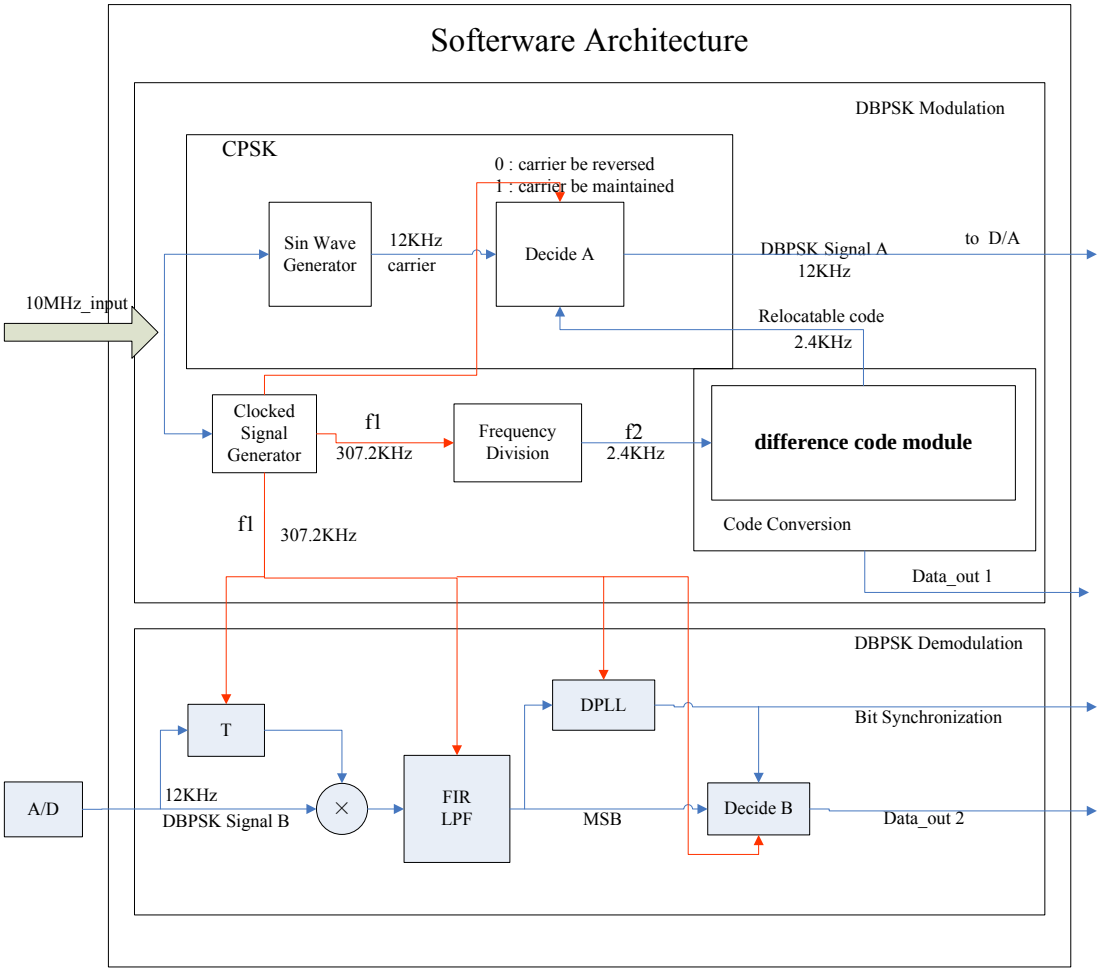


Figure1.1 DBSPK Modulation-Demodulation

The whole Remote Control Test System will make a comparison between data_out1and data_out2 and judge whether the Control is transmitted properly.

1.2 clocked signal generator module design

The clocked signal generator mainly provides all the other modules of the whole system with the frequency f1 square wave clock. Its design principle is similar to the DDS（direct digital frequency synthesis）whose structure diagram is shown in figure 2.1. The Phase Accumulator includes the N bits adder and the N bits accumulator register. The adder will add the frequency control word named K to the data that output from the accumulator register and then the result will be sent to the input of the accumulator register at every clock pulse named Fclk. And the new data of phase that produced by the accumulator register at last clock pulse will be sent to the adder, so the adder can keep on accumulate with the K at next clock pulse. On the whole, the Phase Accumulator accumulates the K a time while every clock pulse be input and the

data out of the Phase Accumulator be synthesized into the phase of the signal, so the frequency of the overflow signal is the frequency of the output signal.

Compare the DDS, the clocked signal generator needs a MSB judgment module instead of the wave memory to output a frequency f1 square wave clock judges by the plus-minus of the data's sign just see figure2.2.

Similarly，the output frequency Fout of the clocked signal generator module can be expressed by the frequency Fclk、N bits width of the phase accumulator and the frequency control word named K, the mathematical expression is shown in (2.1):

$$Fout = \frac{(Fclk \times K)}{2^N} \qquad (2.1)$$

And the frequency resolution is:

$$\Delta F = \frac{Fclk}{2^N} \qquad (2.2)$$

So, the Fout can be changed freely during allowed limits by the software to set up the Fclk、the N and the K according to the actual requirements.[3]

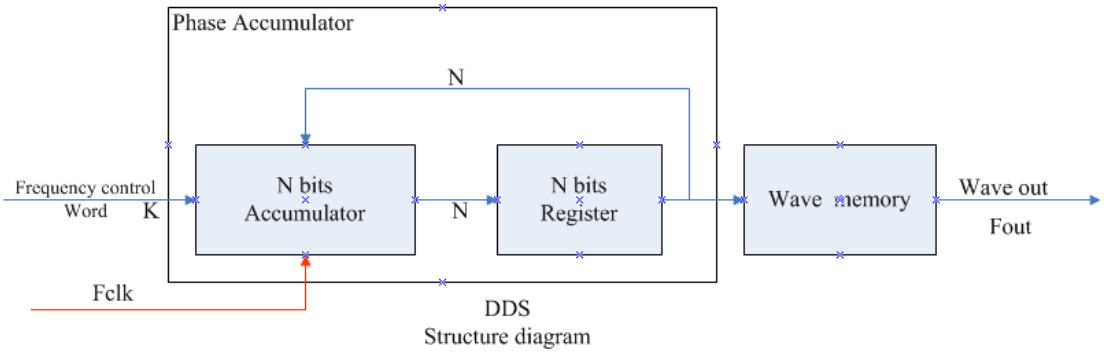


Figure 2.1 DDS Structure diagram

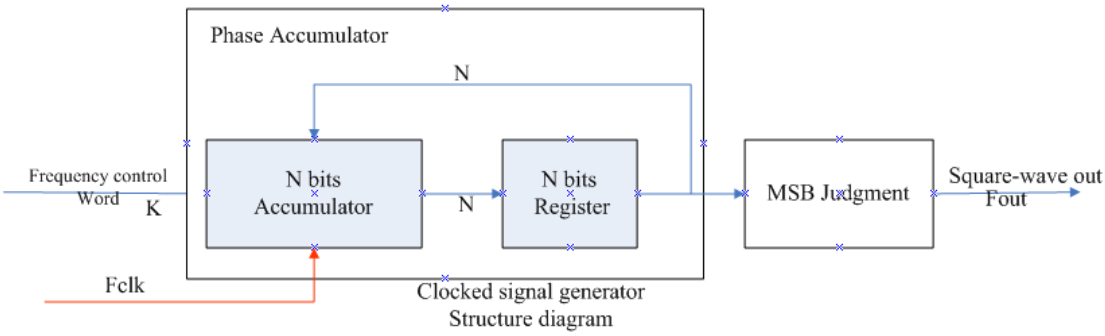


Figure 2.2 Clocked signal generator Structure diagram

1.3 difference code module design

During this design, the difference code module is the signal resource for the whole design. It can get differential code B by convert the absolute code A with the formula (3.1).

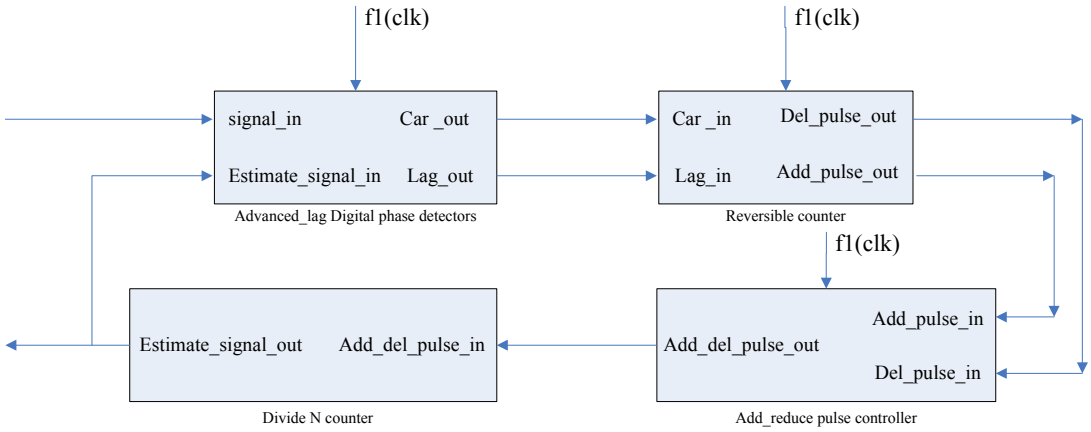
$$B_k = A_k \oplus B_{k-1} \qquad (3.1)$$

1.4 DPLL(Digital Phase Lock Loop) module design

DPLL includes lead-lag phase digital detector、K modular reversible counter and digital controlled oscillator(DCO) as shown in figure 1.1.

(1) The output of the lead-lag digital phase detector is a result that local estimated signal named signal_out subtracts or be subtracted the signal input named signal_in. If the signal_out ahead the signal_in, the detector will output a ahead pulse named car in order to control the phase of signal_out to move backward; or the detector output a lag pulse and the phase of signal_out to move forward.

(2) The K modular reversible counter will count the signal_out reversibly. When the result out of from the counter reaches a default value, it will output a add/discount pulse signal. So that the DCO can adjust the phase, and the counter be used as a loop filter on the whole. The initial value is set to N. If the ahead pulse arrive at and the counter adds 1, or the lag pulse arrive at and the counter minus 1. After a while, when the value if the counter is 2N that means local signal ahead the input signal and the counter will output a discount pulse signal, at the same time the counter will be reset to N. While the value of the counter is 0, that means local signal lag the input signal of the counter. So the counter will output a add pulse while it will be reset to N.



Advanced lag character synchronous
digital phase lock loop

Figure 4.1 ahead-lag character synchronous digital phase lock loop

(3) The DCO have another name called digital clock ,it includes pulse add-minus controller and N frequency divider .The DCO's output is a impulse sequence. The pulse add-minus controller will track and adjust its input signal's frequency and phase, then the output signal's frequency and phase will be locked the same as the input signal at last. The output signal of the pulse add-minus controller will be frequency divided with N by N frequency divider, in order to get the local estimated signal. While the local estimated signal ahead the input signal, the minus pulse will minus one pulse of the local high speed clock named Add_del_pulse_out, and then the Add_del_pulse_out will be frequency divided with N by N frequency divider to get the local estimated signal whose phase is moved backward , whereas Add_del_pulse_out will be insert one pulse and be frequency divided with N to get

the local estimated signal whose phase is moved forward. If there is neither minus pulse nor add pulse to control the output signal, the Add_del_pulse_out will can't be controlled but to be frequency divided with N and its phase is in synch state.

1.5 Other module design

In order to reduce product's cycle of development and improve the flexibility and stability of the product, this design takes full advantage of the IP core in the software Quartus II. The sine wave generator module adopts the NCO IP core to produce a sine wave. The LPF(Low pass filter) adopts a FIR(Finite Impulse Response) IP core whose type of window、sample rate and cut-off frequency all can be set to meet demand. So this design is adjustable because of using the IP core in some important parts of the whole design.

1.6 simulation and test result

(1) The input clock frequency of the DBPSK modulation is 10MHz. See the figure 6.1,this is the result of DBPSK modulation that be simulated with modelsim simulator. The cycle of the information code and the difference code named a_out labeled with blue frame, the frequency 's cycle of the carrier labeled with red frame.

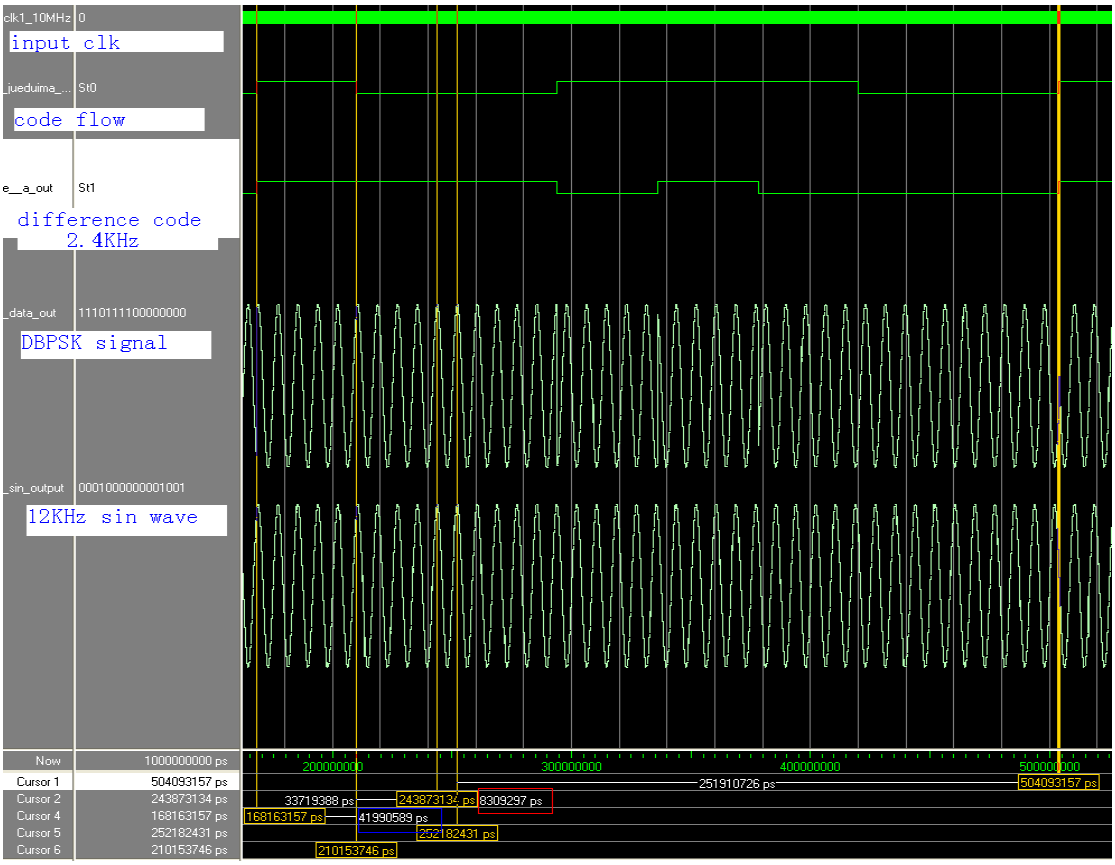


Figure 6.1 simulation result

(2)The whole design external connects a 10 MHz crystal oscillator and works under 3.3V voltage. Its important part is the FPGA chip EP1C20F324I7 produced by Altera company. The whole software loaded into the chip and then it will produce DBPSK

signal whose code frequency is 2.4 KHz and carrier frequency is 12 KHz.

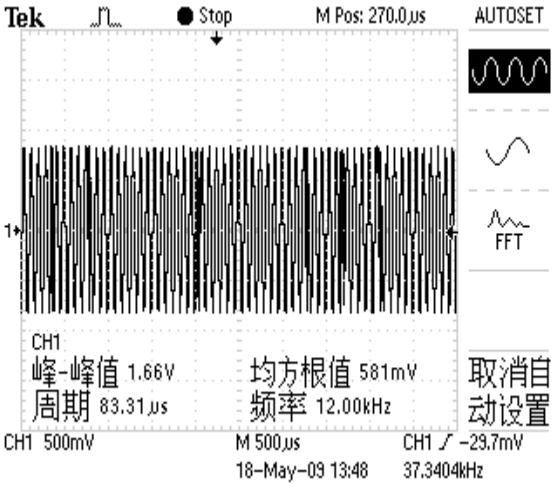


Figure 6.2 DBPSK modulation

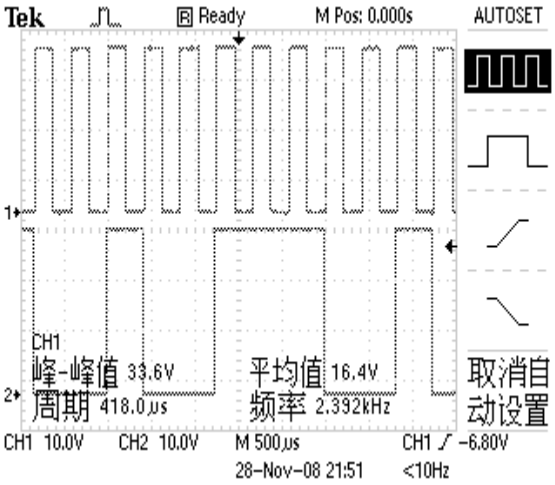


Figure 6.3 DBPSK demodulation

In addition, it will demodulate the DBPSK signal received from the receiver's front end to the information code and bit synchronization whose frequencies are 2.4 KHz. The test results are shown in figure 6.2 which is DBPSK modulation signal and figure 6.3 which are bit synchronization signal marked with one and information code marked with two that judged rising edge by the bit synchronization. And figure 6.4 is the test result of the DBPSK demodulation when this design is embedded in the whole Telecommand in Remote Control Test System whose information code is marked with yellow, the other is marked with green.

Figure 6.4 DBPSK demodulation

CONCLUSION

The paper introduces the software structure of the whole design at first, and then analyzes the important modules in detail. At last, the test results are all meet demand when the design is independent and embedded in the whole Telecommand in Remote Control Test System.

This design can achieve that the frequencies of the information code and the carrier are adjustable just change them in the software and then load into the chip, but inconvenient to adjust the parameters above mentioned by PC or land station directly. So it maybe comes true for the future.

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