TRANSISTOR -MAGNETIC LOGIC IN AEROSPACE TIMING

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INTRODUCTION

Over a period of years, a number of magnetic circuit programmers for control logic and timing systems have been developed for Aerospace use. These units all have in common the non-volatility of storage inherent in magnetic material and exhibit low power consumption in both standby and operating modes. Depending upon the parameters of the application, a number of various types of magnetic logic could apply and it is the purpose of this paper to present design balances, tradeoffs and approaches to system design. The core-memory programmer discussed here in some length, has been used in a number of spacecraft.

Basic Method

In the process of executing a program, magnetic logic performs two basic operations. (a) Count down from an oscillator time base to establish the execution time, and (b) Storage in memory of the time for execution of a given operation and of the operation itself. A general block diagram of a sequential programmer is shown in Figure 1.

The simplest magnetic counting circuit is the two phase core-diode circuit. This is shown in Figure 2. The circuit requires two shift currents labelled I_1 and I_2. The widths of these currents are not particularly important so long as sufficient volt seconds can be supplied to the core to switch it. The technique consists of starting a “ONE” at the core labelled 0_1 and allowing this “ONE” to propagate 1/2 stage for each shift drive. The system operates as a shift register which may be used for counting, shifting or storing processes. The diodes shown are to insure the propagation of information only in the left to right direction at the occurrence of a shift time and to re duce response to spurious noise and external sources of ionization.

Figure 3 shows another implementation of core-diode counting. The number of cores is reduced by a factor of 2. The penalty paid is the inclusion of a delay network of time delay longer than the width of the shift pulse. Figure 4 shows the sequence of operations. The shift pulse of width 1/2 microseconds pushes the core to the “ZERO” state. If the

core was in the “ONE” state, energy is transferred to the delay network. This shifting operation takes place in all cores simultaneously. Following the shift, the energy stored in the delay network arrives at core 2 and sets it to the “ONE” state. For given energy transfer and for a given rate of change of current, a particular voltage will develop across each shift winding, and the total voltage developed in the entire register will then be determined by the number of “ONE” present in the register. A core containing a “ZERO” will undergo a small flux change when shifted and will have a small back voltage.

The number of cores that can be shifted by a current driving network becomes quite small when high speed counting is desired. It is difficult to obtain reliable operation for less than about 0.5 volts for the few hundred milliamps usually available in aerospace equipments. The voltage output of each stage can be transferred to a shift register for cycling and comparison to the active wording memory.

Core-Transistor Methods

The inclusion of a transistor in place of the diode adds reliability and flexibility to the operation.

a. Regenerative operation. Figure 5 shows a transistor core and delay network wired in the regenerative mode. The shift pulse supplies energy to turn the transistor into the conducting state. The regenerative core winding in the collector of the transistor then continues the switching to the “ZERO” state. Thus, the energy is supplied to the core by the transistor and not by the shift. The shift back-voltage is reduced and the number of stages which can be driven from the current source in the shift line is increased.

b. Figure 6 shows the core, transistor and delay network connected without regenerative feedback. There is a somewhat higher back voltage and lower voltage margin with this circuit.

Counting techniques utilizing sequential methods are based upon the use of a shift register with feedback. Figure 7 shows an N-stage feedback shift register in which the first core is set to a “ONE” before shifting begins. The feedback is modulo 2 from the two adjacent final states. The coudter shown is no longer operable as a scaler or counter by itself, but requires auxiliary stages for the detection of a code state. This device can generate all possible states except the “ZERO” state and can give an output binary code. The detector can be as simple as one extra core. By presetting the proper codes, the count can be preset to any desired value. Figure 8 shows a dual register timer designed for a military missile.

The shift register shown in Figure 7 can now be coupled with the magnetic core memory and code coincidence detector to produce the basic reference timer. As shown in Figure 9, the outputs of the register and the memory are compared in a magnetic exclusive-or circuit. When the circuit determines a word equality situation, the program portion of the word stored in memory is sent to the system control logic for execution. The operation can be performed each time the register is indexed if the commands in memory have been previously stored in time sequence of operation. This is the preferred storage method since a non-organized storage will require complete scan of the memory at each count index.

Storage of Count

Since temporary power shutdown often occurs in an ordnance or aerospace vehicle, operation of the equipment during power outage must be considered. If a system uses only semi-conductor solid-state elements, power loss implies loss of information and time. A properly designed magnetic logic system will hold its state during outages and shutdown as well as through severe line transients.

The magnetic shift register can be used also for serial to parallel or parallel to serial conversion. Thus, the serial data word from memory can be easily converted to parallel for execution. The presetting method is shown in Figure 10 in the case of a shift register. Presetting can be accomplished by loading information at any stage in the system in sequence or in parallel as shown. A block diagram of a system of this type was shown in Figure 8 which had incorporated in it the first stage of counting.

Use of Core Memories

Figure 11 shows a memory sequence timer in which the storage of instruction and time is in a magnetic core memory. This sequential memory coupled with the use of core-transistor linear feedback register and one decoding stage offers the best possiblity for the execution of a very large number of programs. As each program is loaded, counted down and sequenced, the memory loads the next sequential number into the shift register. As an example of the saving involved, a typical programmer using field settable resistive plugs, the DI/AN Model 12-12/FP, weighs 5 pounds and occupies a total of 109 cu. in. A memory sequence timer of similar weight and volume could handle 75 sequences with independent outputs. Thus, the technique can be seen to be very powerful for control functions in which large numbers of circuit activations are required.

In addition, the memory sequence devices can be altered at any time via a telemetry link.

The programmer can be tied to the telemetry link to both send and receive instructions and time information. The program may be fixed via a pre-wired circuit or can be altered

before launch in a number of ways. In those cases, the times of discreets are not alterable by telemetry. In most applications, the occurance of a discreet is fed to the TM link for transmittal to the ground.

When a fixed program is used, a number of approaches can be taken.

When the number of stored times gets above 3 or 4, the number of permanent connections can yield a large, unwieldy connector for programming. Recourse is to a plugboard matrix setup. This approach is valid from 5 to about 20 intervals. The photograph in Figure 12 shows a programming plug matrix presently used on the Agena launch vehicle. Each plug constitutes the jumping of a resistance between two points in the matrix.

For more than 20 instructions, the combination of serial memory and linear feedback register becomes best. The estimated volume of a programmer is shown in the graph of Figure 13. The lower curve shows the optimum values which can be expected when volume and weight are of primary importance. As the number of instructions increases, less alternatives exist and the volume latitude narrows. The smallest single-event timers occupy about 3 cu. inches, but special ordnance use timers have been built with accuracy down to 2 cubic inches. The projection indicates that a carefully designed memory sequence timer of 100 instructions would occupy from 140 to 180 cu., inches. This would include the sequential memory of from 1000 to 2000 bits.

The weight of these units varies in proportion to the system volume. Modularized, encapsulated circuits mounted on printed circuit cards with ancillary circuitry and sufficient mechanical structural support weigh approximately I/ 2 ounce per cubic inch of volume. When one considers the density of epoxies, electrical components, and structural members, this number is not unreasonable. The dotted lines in the figure indicate the approximate weight boundries. A well-designed single-event timer for moderate accuracy could weigh as low as 1-1/2 ounces and the 100 interval memory sequence timer would weigh in the range of 6 -1/2 to 9 -1/2 lbs.

Reliability Considerations

With regards to relative reliability of the devices considered here, there is as always a wide discrepancy in interpretation of exixting data. In the case of the small programmer, the selection of a logic- approach may be heavily swayed by the component count or the types of failure modes. Regardless of the number of intervals, the time base and counting mechanisms generally do not change. However, the mechanism of storage and the method of achieving the outputs have a strong effect on the reliability of the overall system and these may be varied depending upon the system requirements.

If a consistent definition of reliability values for cores, windings diodes, etc., is taken, then a relative reliability of various systems can be calculated. This calculation is a relative statement of reliability since in ordnance applications, it is often not the random failure mode that effects a failure, but a special failure mode brought about by a unique environmental situation.

First, one must consider the mode in which the output signals will be utilized in setting up reliability criteria. Many steps, such as quad-redundant diode and capacitor groups or series connected relays can be instituted to insure failsafe operation with a moderate sacrifice in the reliability in the direction of failure resulting in no output, that is, no instruction given is better than the wrong instruction.

From a straightforward component count and failure rate calculation the system using (MAD Shift registers) appears optimum, since the number of active components is minimized. Following that technique, would come, from a hardware standpoint, the 2-phase core diode approach and the bucket and ladle technique, core diode circuitry with delya, core-transistor circuitry with delay and finally core transistor (regeneratively connected) circuitry with delay. Of course, one must take into account the logical design approach (linear feedback register, loop accumulator, scaler) and the length of the program since the hardware could increase linearly. For a large number of instructions, it is assumed that a core memory accompanies the counting hardware.

The technique using multi-aperature devices results in a design which is extremely sensitive to voltage variations and temperature margins and requires relatively high current shift pulses. The latter requirement reduces the reliability by increasing the complexity and the stress levels of the associated shifting circuitry. This also applies to these devices when used in the memory portion of the programmer.

The two-phase core-diode circuit is desirable even though the number of actual stages is doubled by the need for odd and even shifts. only a single diode need be placed between stages to obtain reasonable range of operation. The second diode performs as a failure reduction circuit in radiation environment. The requirements on the associated drive circuitry are more critical in the two phase core-diode register than any system except MAD circuits.

In the core-diode circuit with passive delay network, a significant increase in margins can be obtained at a sacrifice in parts count reliability. A further increase in operating margins can be obtained with the core transistor circuit with delay network technique. Here again, the failure rate of the overall system would appear to increase, but a trade-off begins to appear obvious since extremely long divider chains can be implemented.

A reliability balance sheet shown in Figure 14 has been prepared with the approaches rated with regard to the relative reliability of each technique. Three categories have been provided: (a) parts count, (b) design margins, (c) accuracy and long term stability. The specific weighing that one would place on each category in an actual sub-system design would depend somewhat upon the criteria delineated when other aspects, such as the environment and operational modes, are considered. Thus, the high-rel requirement of a satellite programmer and the absolute fail-safe requirements for accuracy a nuclear device would obviously require different weighing factors since the relative reliability factors are different.

CONCLUSION

Magnetic logic is inherently suited for serial data handling and therefore is easily used with telemetry systems. The wide margins of the core-transistor circuit, plus its ability to store its state during power shutdowns makes the technique highly valuable for spacecraft control systems.

Core-logic is compatible with magnetic core memories used for storing program information by time coincidence measurements. Intervalometers and programmers of a desired size and accuracy can be built with a minimum number of semi-conductors. The resulting core logic system is highly reliable and relatively impervious to temperature, shook and radiation.

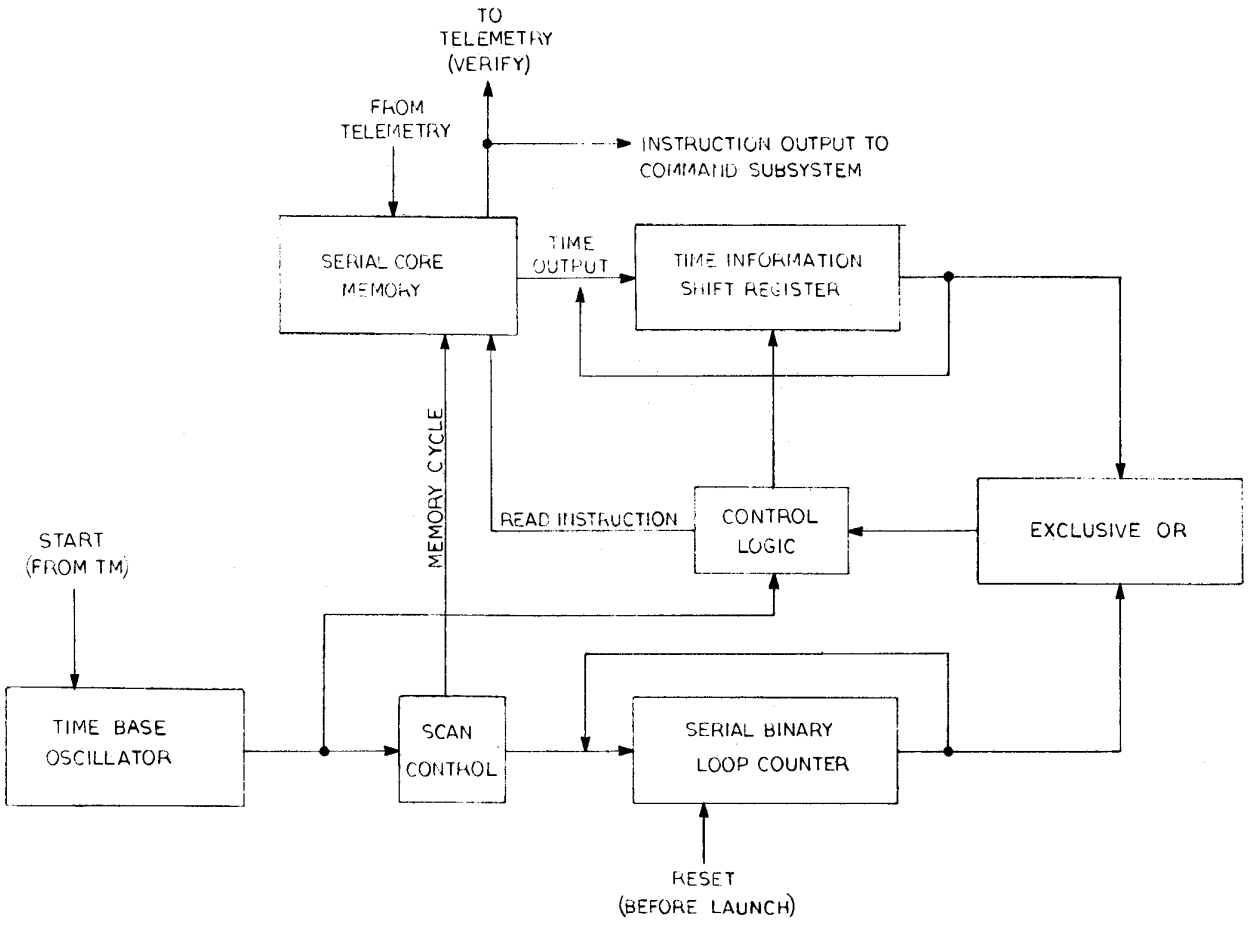

Fig. 1 - Magnetic Sequential Programmer Block Diagram

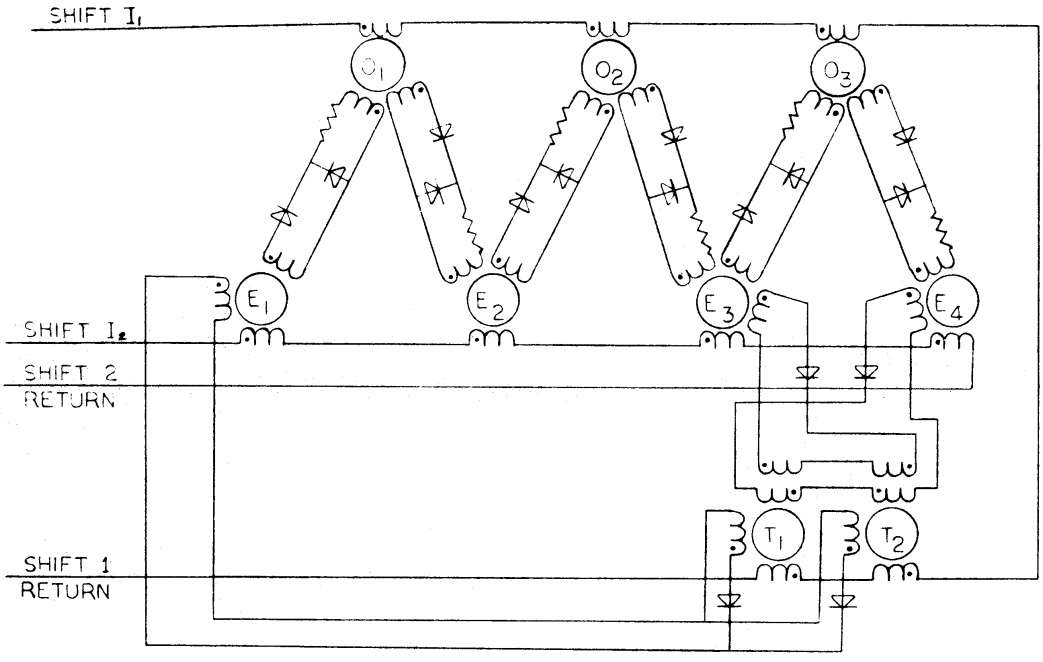

Fig. 2 - Two Phase Core Diode Register

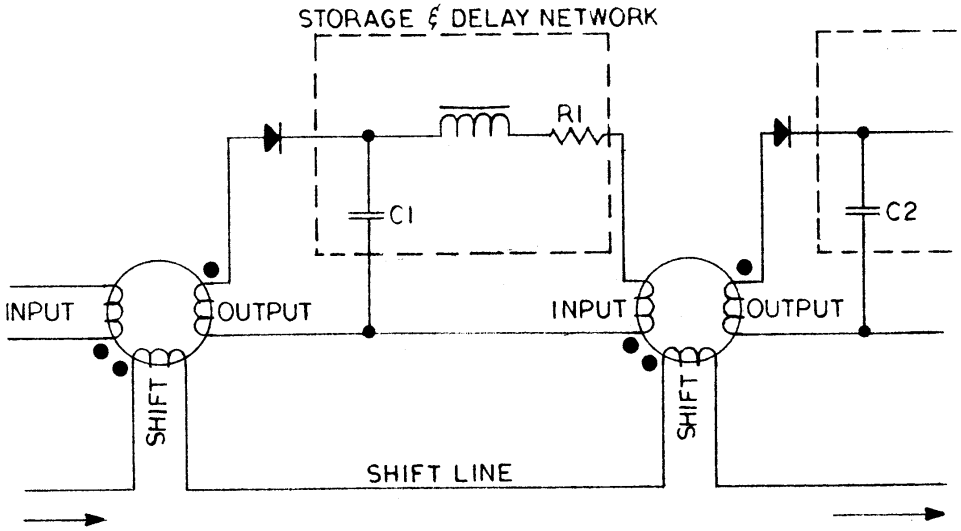

Fig. 3 - Core-Diode with Delay

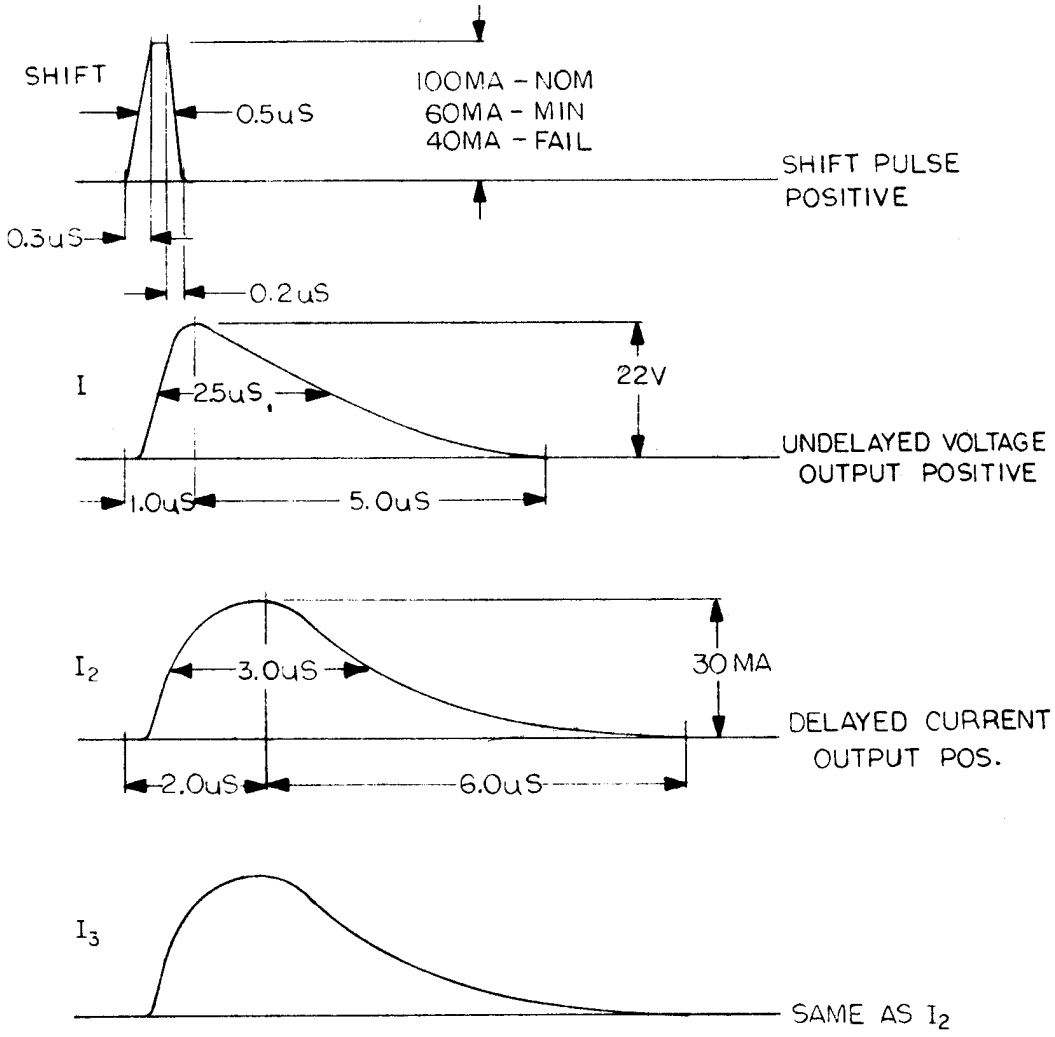

Fig. 4 - Delay Logic Timing Diagram

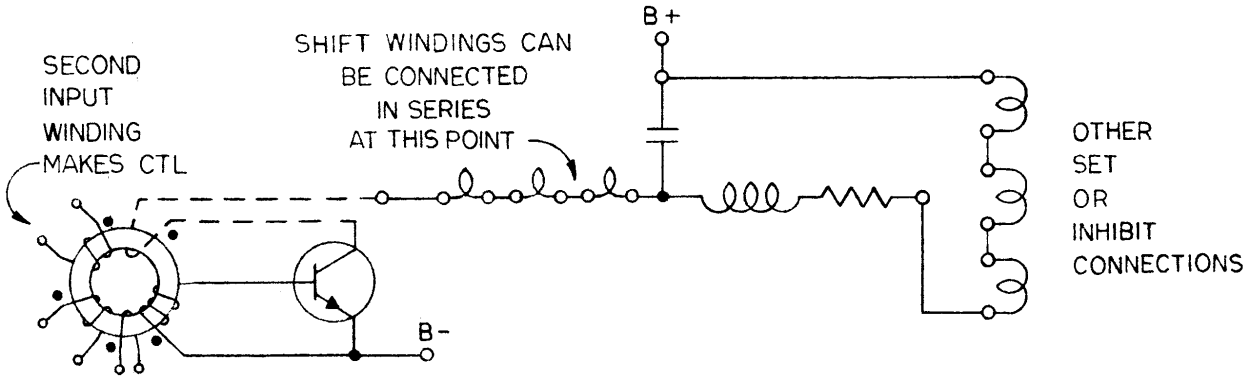

Fig. 5 - Regenerative Core Logic Schematic

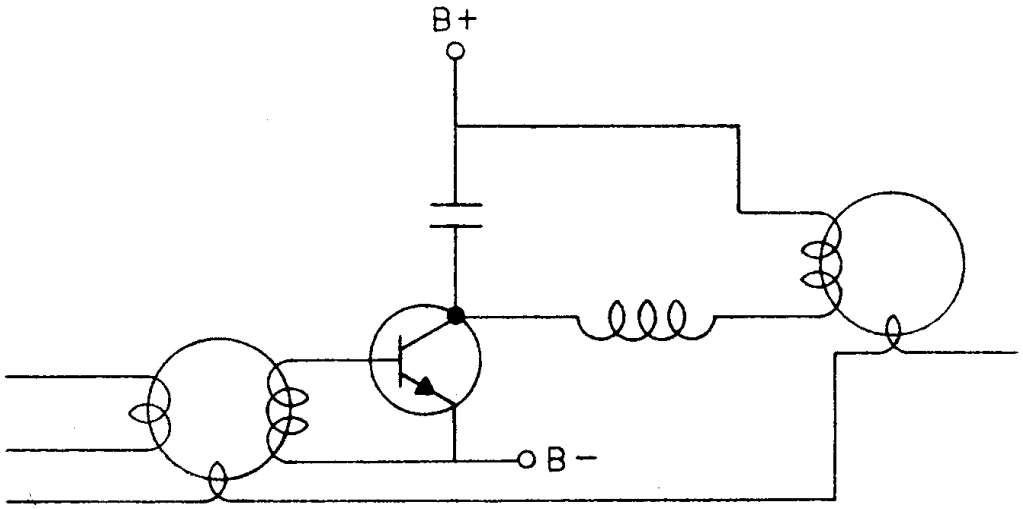

Fig. 6 - Core Transistor Non-Regenerative Logic Schematic

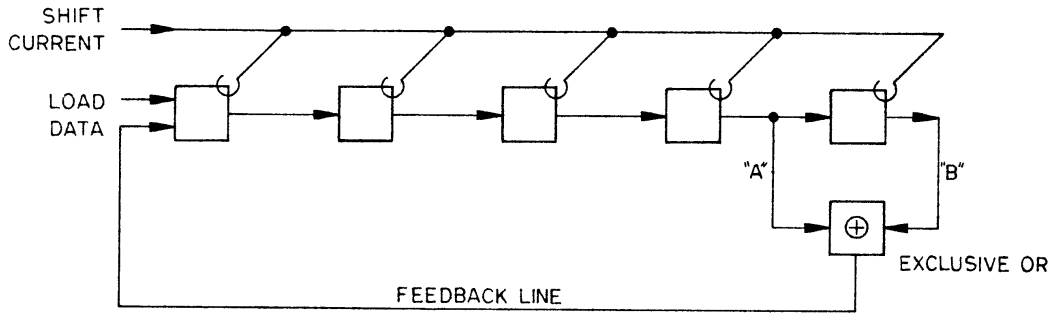

Fig. 7 - Linear Feedback Register

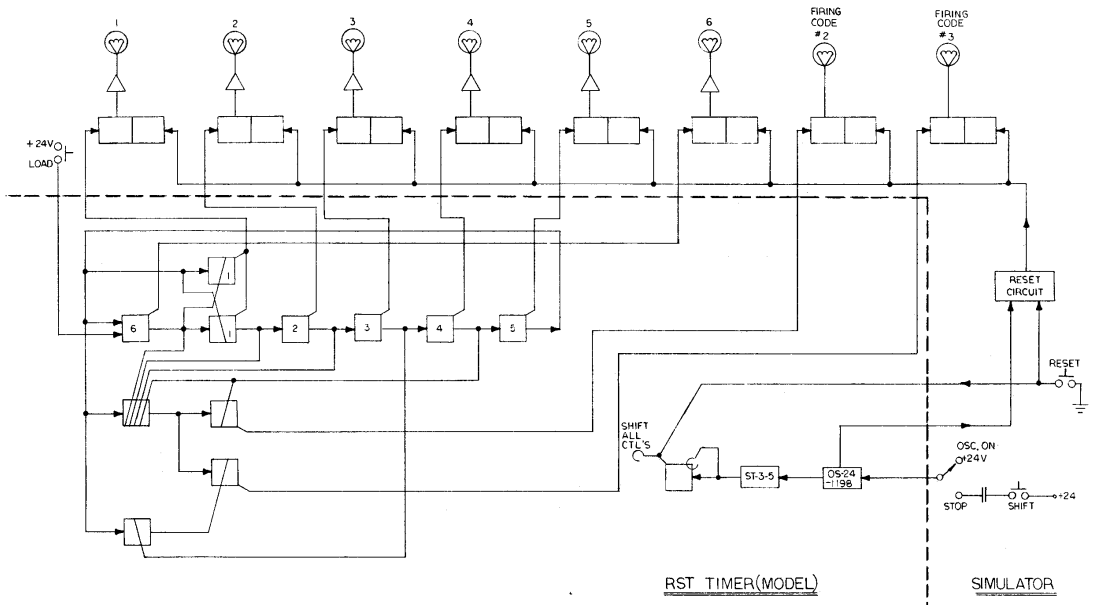

Fig. 8 - Linear Feedback Timer with Decoder

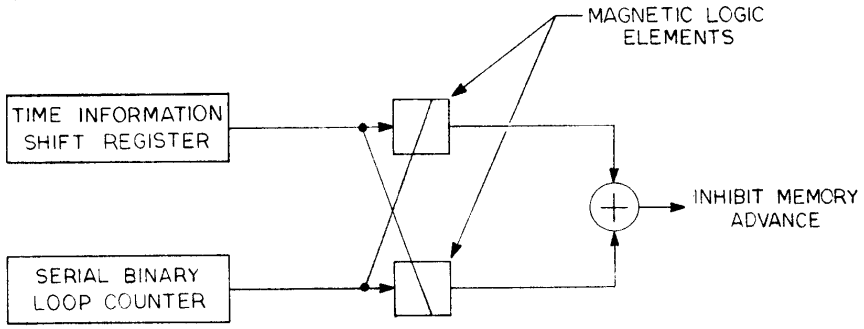

Fig. 9 - Serial Time Comparison

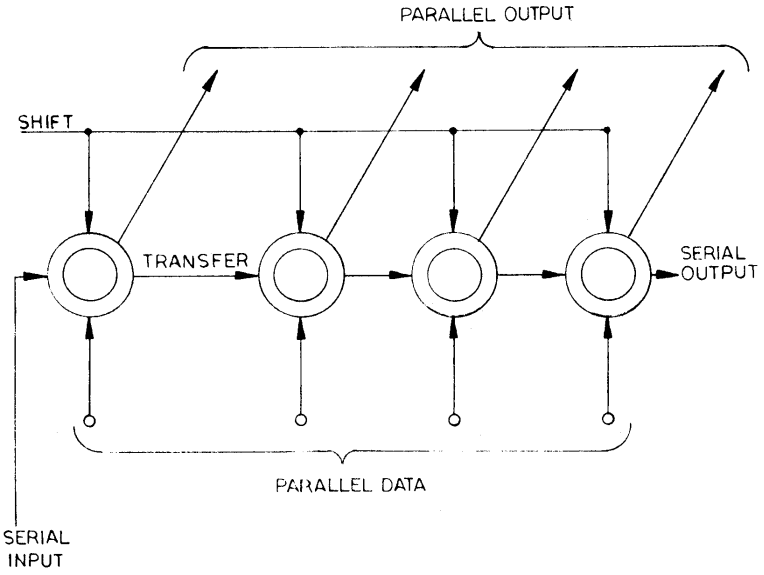

Fig.10 - Core Presetting: Parallel to Serial Conversion in a Shift Register

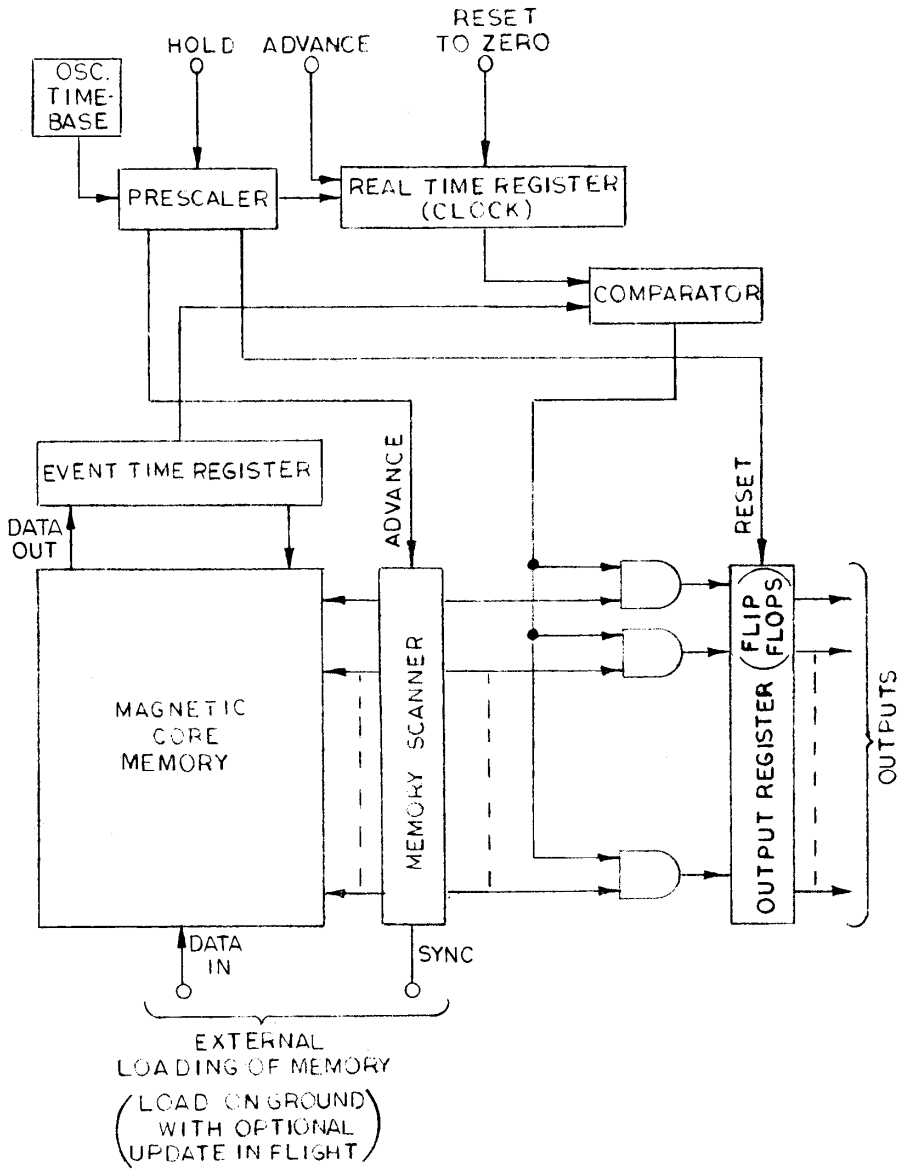

Fig. 11 - Electronic Sequence Timer with Program Memory

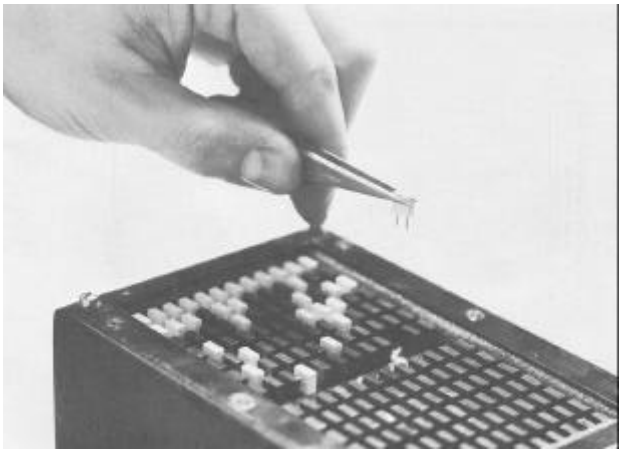

Fig. 12 - Resistor Plug Matrix Programming

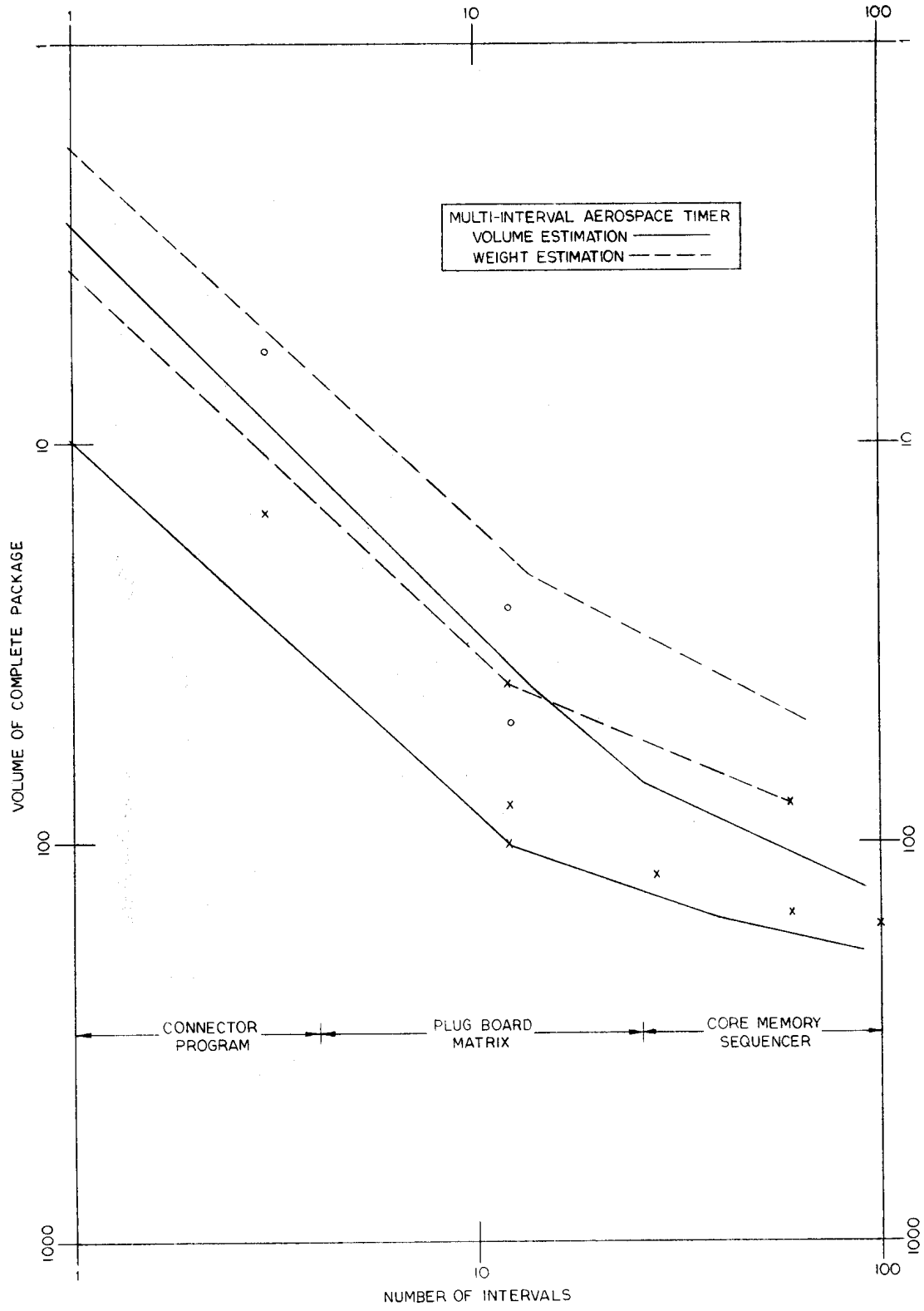

Fig. 13 - Volume and Weight Estimations

	Relative Failure Rate (16)	Relative Failure Rate (1024)	Relative Failure Rate (1x106)	Design Margin Reliability	Accuracy
MAD register	3*	3	3	1	2
2/O Core Diode	1	1	1	2	3
Core-Diode w/delay	2	2	3	2	3
Core-Transistor w/delay	2	2	2	3	3

*Rating is 3, 2, or 1 where 3 is the most reliable

Fig. 14 - Reliability Table