AN ADVANCED RECONFIGURABLE MULTI-CHANNEL COMMUNICATION TERMINAL FOR TELEMETRY APPLICATIONS BASED ON FLEXICOM 260A

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ABSTRACT

Traditional communication hardware has focused on modular architectures. Now, with the incoming high speed DSP and FPGAs a shift from traditional modular architecture to reconfigurable architecture has taken place. The nature of this architecture allows to optimize various telemetry applications in a single platform. This paper describes a reconfigurable multi channel communication system.

KEY WORDS

Reconfigurable hardware, DSP, Turbo Codes, OFDM.

INTRODUCTION

A high bandwidth reconfigurable signal processing platform is under development as part of a reconfigurable communication system research program at Navtel Systems. The objective is to develop a reconfigurable communication terminal for telemetry applications. The nature of the hardware allows to adapt different signal processing requirements during various phases of the program in order to validate each phase in a highly flexible way both in hardware and software. The hardware functional requirements are the following:

1. System simulator
2. In-built instrumentation for real time test
3. Application selectable modulation and demodulation schemes
4. Application selectable bit synchrononization schemes
5. Application selectable forward error corrector codec

6. Stream and block based signal processing

7. ASIC emulation facilities

8. High speed PCI interface

The development program is based on three phases.

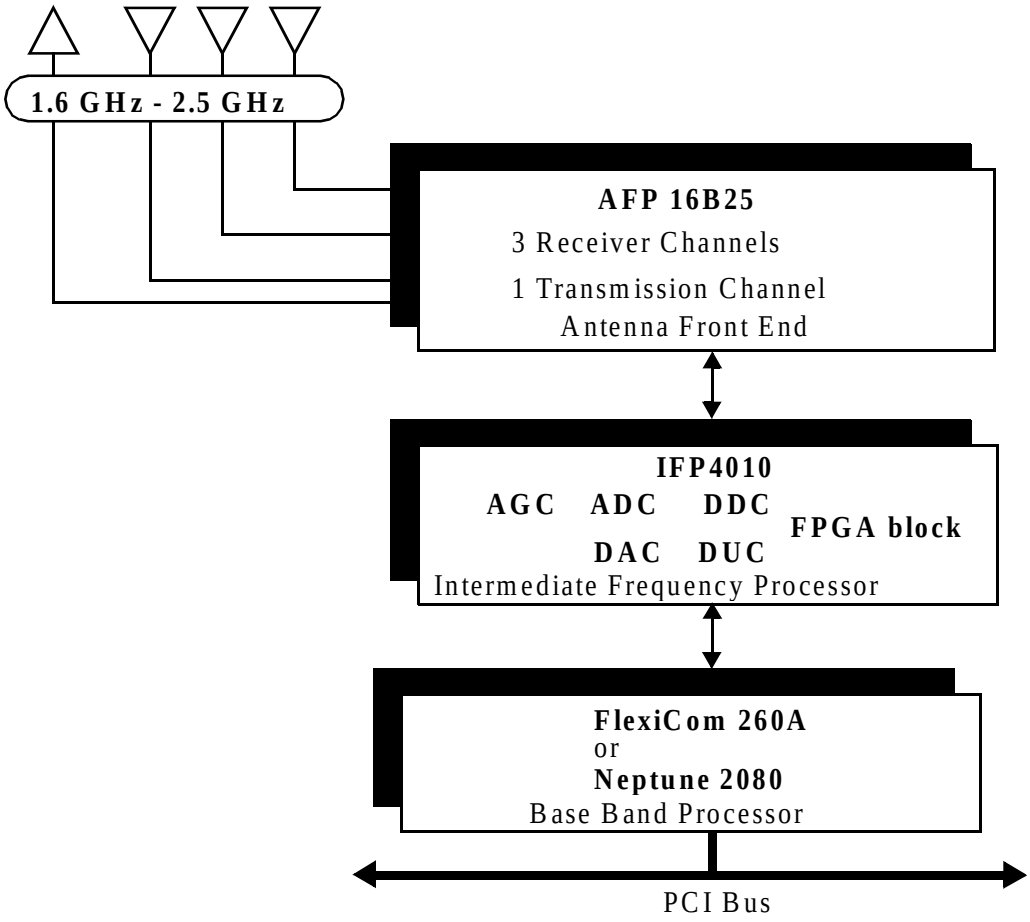
Phase I: Develop two platforms, FlexiCom 260A based on the Tiger Sharc DSP from Analog Devices™ and the 2nd platform NEPTUNE 2080 is based on the C60 DSP family from Texas instruments™.

Phase II: Development of an Intermediate Frequency Processor IFP4010. This has three receiving and one transmitting channels.

Phase III: Development of an antenna Front End Processor, AFP16B25 covering 1.6 GHz to 2.5 GHz.

HARDWARE PLATFORM OVERVIEW

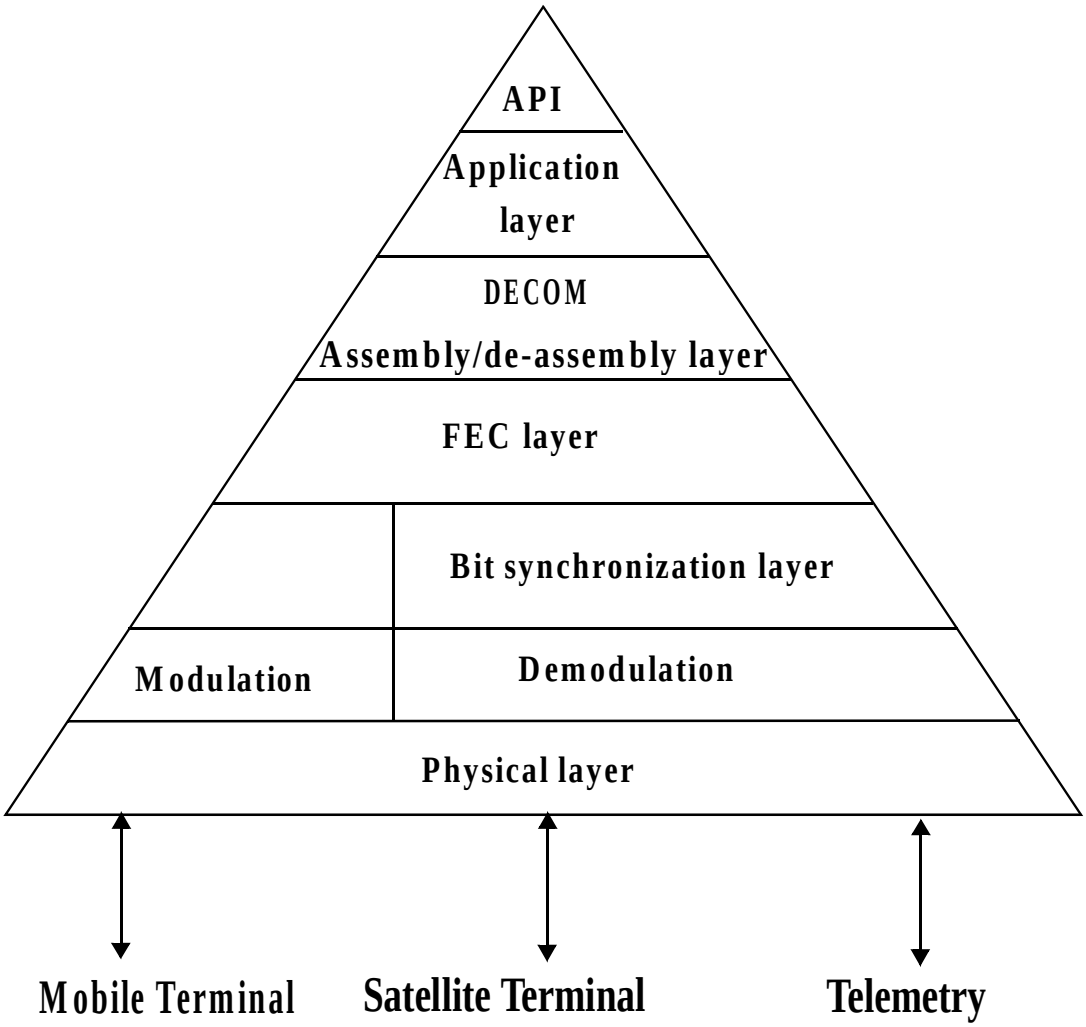
The platform is made of three parts as shown below. AFE16B25, IFP4010 and Flexicom260A or Neptune 2080. The platform constitution is given below.



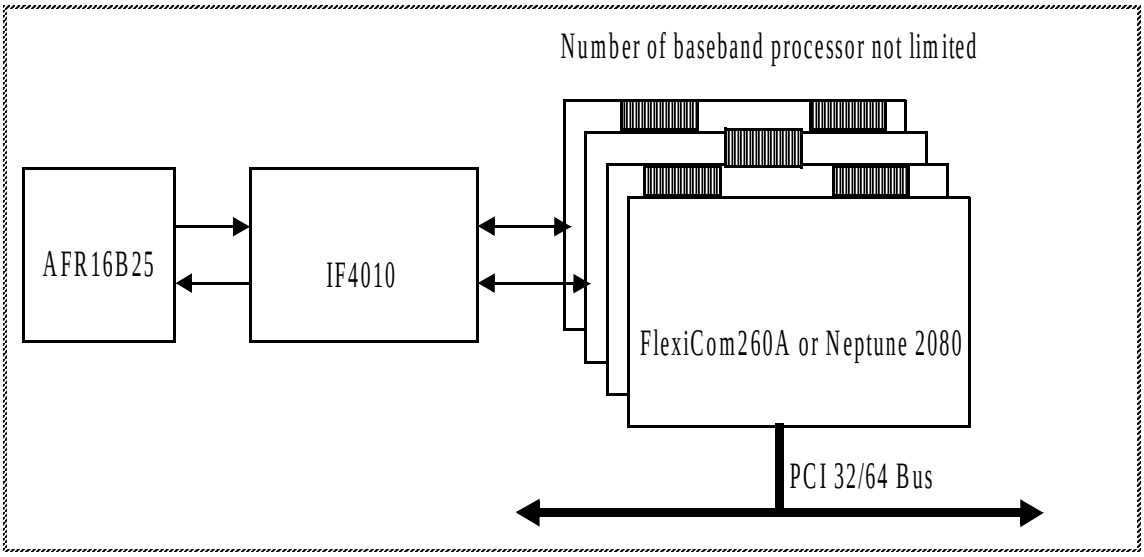
The platform hardware layer consists of multiple DSPs and high density FPGAs. This allows algorithms implementation in a flexible way for modulation schemes, bit synchronization and error correction methods. The hardware has been designed to handle block and bit stream level processing in a multimedia communication environment (Speach, Video and Data).

SYSTEM LAYERS

The platform can be considered as a set of logical layers and their constitution in a reconfigurable hardware platform is given below.



SYSTEM LEVEL INTEGRATION OVERVIEW



BASE BAND PROCESSOR RESOURCE DIFFERENCES

Table 1: Baseband Platform Comparison

Resources	Neptune 2080	Flexicom 260 A
Hardware	Reconfigurable	Reconfigurable
DSP	4 x Ti320C6201/6701	5 x Tiger Sharc
Number of channels	4	5
FPGA block I	600 K to 1200 K Gates	600 K to 1200 K Gates
FPGA block II	600 K to 1200 K Gates	600 K to 4200 K Gates
FPGA block III	1000K Gates	2000K Gates
PCI Interface	32 bit master slave	32/64 bit master slave

SIGNAL PROCESSING

Today telemetry equipment are different from what they used to be in the past due to the handling of different modulation and error correction schemes according to the channel environment. At the same time, the new equipment has to be compatible with former existing standards (eg. Concatenated coding as well as Turbo coding). The reconfigurable technology meets both requirements.

INTERMEDIATE FREQUENCY PROCESSOR IFP4010

It is made of three parts: an input IF filter followed by an input power meter, AGC, ADC, down converter module (off-the-shelf chip or implemented in FPGA). The ADC clock has been designed to enable the selection of the input clock from three possible sources :

- Fixed clock for bandpass sampling
- Closed loop control clock from the demodulation block
- OFDM clock module

The FPGA down converter is made of quadrature multipliers (the local oscillator output takes the form 0,1-1,0...), linear phase filters (the use of a half band filter reduces the computational load) and a resampler. Access to the IFP4010 is performed through any base-band channel. Under simulation mode, the up and down converter modules can be put to the loop back mode.

BASEBAND PROCESSOR

Two different platforms are available for algorithms implementation: FlexiCom 260A and Neptune 2080. The baseband processor handles

- Modulation and Demodulation (single and multi carrier)
- Bit synchronization
- Error CODEC
- De-commutation

<u>Modulation demodulation modules</u>

The reconfigurable modulation schemes allow to select the modulation format adapted for the environment : example S/N (Signal/Noise ratio). Some of the modulation schemes used in satellite and terrestrial communications are summarized below.

Table 2: Modulation schemes

Format	Application
BPSK	Space
MSK and GMSK	2G
QPSK	Satellite and 3G
8 PSK	Satellite
QAM	Microwave Digital Radio Direct Video Broadcast

The demodulation data flow chain consists of a digital down converter, a root cosine and I&D filter-block and a carrier tracking loop. The spectrum shaping filter excess bandwidth varies between 0.35 and 1. It is function of the combined effects of the transmitter and receiver channels. The reconfigurable hardware allows to set up filter tap values dynamically according to the environment. The DSP requires a hardware support when the bit rate is higher than 1Mb/s. The phase error calculation can be aided by a prediction block which estimates the possible received signal position from the timing error value. The Tiger Sharc DSP is better adapted than the Texas C60 family for the carrier phase detector, AGC, and loop filter calculation due to its floating point capability as well as its internal architecture.

OFDM IMPLEMENTATION

The OFDM is another modulation scheme finding more and more applications in the aircraft testing due to multipath effects in the telemetry channel and spectral efficiency. The system requires a linear amplifier due to multi carriers (the hardware is designed to study peak to average power reduction using coding).

The system design parameters fall into two main categories: number of carrier selection and type of channel coding. The number of carriers required is function of the bit rate, OFDM symbol rate and delay spread of the system. The type of error correction depends on the application (Viterbi-RS or Turbo codes). The channels coding with its interleavers requires a flexible memory structure but this, in turn, depends on the selected coding with its block size.

In the receiver, three Tiger Sharc^{TM} DSP with the associated FPGA block are able to handle an 8K carrier system. The required functions are synchronization, demodulation, channel estimation and equalization. The reconfigurable nature of the hardware allows to select dynamically modulation, synchronization and error correction according to channel conditions. For example, if the channel path of the receiver is good, then the system is able to use a higher modulation scheme. In order to adapt the channel, the system has to be a transreceiver for having communication with the transmitter. Flexicom 260A consists of three receiver channels and one transmission channel, in order to handle adaptive modulation schemes.

BIT SYNCHRONIZATION

The hardware has been designed to handle closed and open loop synchronization methods. Both of these structures use on-board MNCO (Modulation Numerical Control Oscillator). In the case of open loop, the MAP and Gardner's interpolation structures (no common clock between demodulator and bit synchronizer) are both possible. The MAP method requires a large number of match filters. However a reduced number of match filters can be used to make a rough estimation. This estimation is used to shift the MNCO phase and then close the loop. In the case of an interpolation method, one requires two samples from the interpolator block : one is used to strobe the data and the 2nd one is used as the mid-sample. Both samples are used to calculate the error ; the calculated error is filtered and used to control the resampler NCO. The error calculation is based on the previous symbol, the current symbol and the mid-symbol. The use of the two interpolator outputs simplifies the error calculation. The lead/lag loop filter allows to correct the frequency error. The bit synchronizer block can receive quality information from the error corrector block in order to enhance the performance in closed and open loop modes. Often, the error corrector performance is limited by the bit synchronizer. In Flexicom 260A, under the bit synchronizer mode, it is possible to reconfigure the bit synchronizer according to the channel conditions as well as improve the performance by using information coming from the error correction block.

SOFT DECISION

The MSB of the bit provides the hard decision and the remaining part of the LSB provides the confidence information. The number of soft decision bits depends on the type of error corrector used. The Turbo coding is associated with the next generation systems and one of the parameters needing to be evaluated is the number of soft bit outputs for a given application. As the number of bits increases the computational complexity increases.The reconfigurable technology allows to study this problem in a flexible manner. The Tiger Sharc processor is selected for fixed and floating point capabilities in order to evaluate the turbo decoding .

FORWARD ERROR CORRECTOR

Various error correction modes can be configured on the hardware :

- CCSDS concatenated RS - Viterbi
- CCSDS turbo codes
- Product codes (RS and turbo codes)

The on-board memory is designed to handle various types of interleavers/de-interleavers. The choice of interleaver is based on the environment and on the type of errors. Today turbo and turbo-product codes replace Viterbi-Reed Solomon combinations in many applications.

SIMULATOR AND INSTRUMENTS

The system consists of in-built instruments allowing performance measurement in terms of Bit Error or Frame Error mode. There are two possible ways to configure the hardware : either half of the system resources are used as the simulator or two base band processors are used : one as a simulator and the other one as the receiver.

CONCLUSION

This paper provides various functional signal processing modules found in emerging and legacy communication satellite and telemetry applications. Today two platforms are available to test and evaluate the performance of different algorithms. Algorithms are under test using Neptune 2080 while waiting for the Flexicom 260A platform. Early simulation results on Flexicom 260A Tiger Sharc^{TM} based DSP hardware show that it outperforms Neptune 2080 based on DSP TMS 320C6201/6701^{TM}. The FPGA family Virtex^{TM} from Xilinx with multiple DPLL facilitates the turbo decoder architecture. The hardware allows to test algorithms in C and VHDL (in a core design concept environment).

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