POSSIBILITIES OF PCM-ENCODING

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SUMMARY This paper concerns with the various possibilities to encode space-signals for PCM-telemetry. It first reviews the logic design schemes to count binary events, to read out counted numbers, to compress data by floating point representation, and to convert analog signals with large dynamic ranges to binary numbers. Then, sane technical solutions, which are under developement by DVL in cooperation with German industry, are described as examples. For these, heavy use of integrated circuits, monolythics, and hybrids was made.

1. INTRODUCTION The continuously increasing importance of particle counting experiments in space application on the one side, and the general trend to use PCM for telemetry on the other makes it advisable to review the various possibilities for PCM-encoding. We, therefore, will compare the logical encoding schemes for binary events, and study the relative advantages and disadvantages with respect to the various applications. Knowledge of these properties may be of use to select the proper system for a specific goal.

By means of this review, we will see, that some of the logical design schemes, which have hardly been practiced so far, would be of good use if proper circuitries would be available on the market.

One of these logic elements is a counter-shift flip-flop. This type of element is now under developement at DVL in cooperation with AEG-Telefunken. Its electronic design and mechanical lay out in thick film technique will be described as well as its application in a special example.

Another element is a 2 to 8 level converter, which could easily be used to telemeter scaled binary events thru analog channels without any programmer. DVL has developed such a system in cooperation with ITT-SEL. It will be described shortly.

Besides of binary events, also analog signals are preferably telemetered in PCM, as well known. One special case of continuously increasing importance is the PCN conversion of analog signals with large dynamic range. Two electronic designs will be reported on.

2. REVIEW OF P(N-ENCODING METHODS FOR BINARY EVENTS.

2.1. LOGICAL ELEMENTS USED We will describe the logic functions by means of the following 4 basic elements: flip-flop with additional set or reset-inputs, or-gate, and-gate, and inverter (fig.1). The logical function of a flip-flop depends on its feedback. As a counter stage its 2 outputs must be fed into its 2 inputs. No feedback is necessary, if the flip-flop shall be used as a shifter stage.

2.2. BINARY COUNTER There are, in principal, two different ways to telemeter binary events:

a. Transmission of each event or each 2^nth, 2^mth, etc., event immediately after it had occurred0by means of a binary signal (synchronous transmission); m, n are integers.

b. Transmission of the number of events which have been counted during a given time interval.

In both cases, except for transmission of every event, counters are necessary.

2.3. RIPPLE COUNTER (BINARY SCALER) (fig.2) - The simplest type of binary counter is shown in fig.2. This binary scaler has, as well known, the following advantages:

a. The counting result CR can be displayed easily as it is stored in a simple mathematical form

$$CR = a_0 2^0 + a_1 2^1 + \ldots + a_i 2^i + \ldots + a_{n-1} 2^{n-1} = \sum_{i=0}^{n-1} a_i 2^i,$$

where a_i is the binary status “0” or “1” of the i^{th} flip-flop.

b. The maximum frequency of the input signal decreases by a factor 2 from stage to stage. Therefore, the counter can be built out of stages with different maximum frequency responses, and different power consumptions.

c. The signal source is loaded by one flip-flop only.

d. Well developed circuits can be used.

The disadvantages are:

a. The counting results are given in a parallel form whereas telemetry requires a time sequence.

b. There is a propagation delay of $\Delta\tau$ from one stage to the other accumulating to a total delay of n $\Delta\tau$.

With respect to other possibilities for counting, compare chapter 2.2.

2.4. ASYNCHRONOUS PCM-TRANSMISSION Before we will consider the synchronous type of PCM-encoding, where in a continuous sequence various counters are read out periodically, we will discuss the asynchronous transmission. This type of transmission avoids the logical circuitry and the programmer, which are necessary for time-multiplexing.

In special cases it seems to be useful to avoid these expenses by counting each individual binary event or a multiple of it (asynchronous transmission).

Fig.3 shows the principle by an example, namely asynchronous transmission of binary events through IRIG-FM/FM-channels. The number of counter-stages are selected so that the maximum transmission-rate is compatible with the bandwidths of the various channels. This straightforward method is not sufficient, if as for channel 7, the rate of binary events varies on a wide scale. This happens very often in scientific experiments. We have then to transmit not only every 2^nth pulse, if n is designed for the maximum bitrate, but also the 2^mth, 2^kth pulses, where m and k are integers, adapted to medium and low bitrates. Therefore, additional outputs of counter stages are necessary.

In order to avoid additional expense on channels it is advisable to take advantage of the good analog transmission quality of FM/FM-IRIG channels. Here, transmission accuracy is, as well known, in the order of at least 5%. It is, therefore, no problem to use 8 discrete levels instead of 2. A resistor network (fig.4) combines 3 binary outputs to result in an 8 level system, each level representing some number out of the 2^3 possible ones. Recording occurs by converting the signal into 3 binary channels (ADC).

We have successfully used this technique for sounding rocket experiments. The electrical lay out is shown in fig. 5; two typical 8 level signals are shown in fig.6.

2.5. READ OUT SYSTEMS FOR BINARY SCALERS In most cases there are many binary scalers in one space vehicle. This requires - except for asynchronous transmission - a programmer which organises the time multiplexed read out of all scalers.

There are different ways to read out the contents of a binary scaler in a time sequence, i.e. to convert from parallel to serial, as described in the following chapters.

2.5.1. READ OUT BY AN ADDITIONAL SHIFTREGISTER (fig.7) Each stage of the binary scaler is connected with the corresponding stage of a shiftregister by a 2 leg AND-gate. The gates allow to overtake the content of the scaler into the shiftregister on command as shown in fig.7. The n binary digits representing the counting result, are available as a time sequence at the output of the register. The bitrate is given by the clock. When overtaking the content into the register it may be necessary to inhibit the scaler input. This depends upon the ratio between the maximum counting rate, the overtaking time, and the permissible bit error. If there is a set of m scalers to be read out in a sequence, two extreme possibilities for the logical location of the shiftregister are given:

a. Every scaler has its own shiftregister as shown in fig.7.

b. All m scalers use the same central shiftregister.

The more reliable solution is the first one shown in fig.7.

A set of m such devices requires the following lines:

m overtaking command lines
m time sequenced input inhibit lines
m output lines connecting the outputs with a m leg OR-gate
1 clock line.

The disadvantage is that each counter stage needs one additional 2 leg AND-gate, and one additional shifter stage.

The advantage is the relative low number of lines between the device and the central unit.

2.5.2. READ OUT-BY ADDITIONAL OR-GATES Fig.8 shows a solution which avoids the shift register by using a n leg OR-gate. Each stage of the binary scaler is connected with the corresponding leg of the OR-gate by a 2 leg AND-gate. The counting result is available at the output of the n leg OR-gate if the n 2 leg AND-gates are clocked in sequence. The bitrate is given by the sequence at the gate inputs 1 to n.

If there is a set of m scalers to be read out into a sequence there are two extreme possibilities for the logical location of the additional OR-gate:

a. Every scaler has its own n leg OR-gate

b. all m scalers use the same central m X n leg OR-gate.

By using the first solution the sequencer has to generate time sequenced read out signals on n lines as shown in fig.8. After finishing the read out period for one scaler the n lines must be switched to the next scaler etc. In addition the input and output inhibit must be switched.

Therefore, the following lines are necessary:

n x m time sequenced lines to the AND-gates

m time sequenced input-output inhibit lines

m output lines.

For the second solution - all m scalers use the same central m x n leg OR-gate - the same number of lines is necessary. Use of the second solution is not advisable from the reliability point of view as malfunction of only one element may cause the interruption of the whole data transmission.

2.5.3. READ OUT BY AN OVERFLOW METHOD The disadvantage of the last solution is avoided by the following one, which will be applied by ITT-SEL in the first German satellite “AZUR” (fig.9).

The overflow of a binary scaler is used to transfer the content of the scaler to an auxiliary scaler. It can be shared by a large number of scalers. The problem of parallel to serial conversion is then reduced to a single counter, namely the auxiliary counter. Transfer is performed in the following manner: After the counting period is finished the binary counter is connected with a clock line. This clock line is also gated with the auxiliary scaler(a backward counter). The backward counter counts clock pulses until overflow occurs in the binary counter. The content representing the counting result is transferred to the auxiliary counter in this way. In the worst case 2n clock pulses are necessary on the clock line.

If the corresponding time is too long, both counters can be splitted for the read-out period as shown in fig.10. The read out time is now $2x2^{n/2}$ clock pulses if both parts are read out in serial, or $2^{n/2}$ if both parts are read out in parallel.

As shown in fig.10, each part of the splitted counter needs two 2 leg AND-gates, one 2 leg OR-gate, and one additional flip-flop.

In general, if a set of m scalers splitted in k parts is used, the following number of lines is necessary:

m inhibit lines
mxk clock lines
mxk lines to the k backward counters.

The disadvantage is the long read out time.

The advantage is that this system can be built with standard elements, and that it is of good use for read out of many scalers.

2.5.4. READ OUT BY MEANS OF DELAY UNITS This solution (fig.11) can be used if the flip-flop has an additional reset input R.

The n flip-flops are combined to a ripple counter. The reset inputs are supplied by n-1 delay units. As shown in fig.11, the counting result will be obtained at the output of the last stage if the clock line is pulsed by n pulses. During the read out period this device acts like a shiftregister. If a set of m scalers is used the following lines are necessary:

m inhibit lines
m output lines
1 clock line.

If the delays can be built very simple this arrangement will be very reliable.

2.5.5. COUNTER-SHIFTREGISTER As shown in fig.1 the same flip-flop can be used either as a counter stage or as a shifter stage by changing the feedback. This property is used for the solution shown in fig.12. During the measuring period the flip-flops are connected as a ripple counter by the n-1 additional gates located between the flip-flops. If the potential at the switch line is changed during the read out period the gates connect the flip-flops as a shiftregister, and n clock pulses shift the counting result out of the scaler.

As shown in fig.12 the input- and output inhibit pulses have the same duration as the pulse at the switching line. Therefore this device needs only the following number of lines if a set of m scalers is used.

M inhibit - switch lines
m output lines
1 clock line.

The additional gates and their connections are of disadvantage.

A more reliable device because of the additional gates being combined with the flip-flops in hybrid technique is discussed in greater detail in the following chapter.

2.5.6. EXAMPLE OF A COUNTER-SHIFTREGISTER In order to simplify the circuit diagram of the CS-register, special flip-flops have been developed for application in encoding systems.

a. Circuit diagram of CS-flip-flops:

If the network (fig.13a) is added to an ordinary shift flip-flop (fig.13a,b) CS-flip-flop is formed (fig.13c). The operation can be easily explained as follows:

Shift mode - The control voltage U is positive, therefore D4 and DS are cut off. Pulses going thru C_E cannot arrive at the base of either Tr 1 or Tr 2. The remaining circuitry shows the wellknown shift flip-flop.

Count mode - No shift pulses are applied to pin S, U is zero. Pulses thru C_3 overrule pulses thru R_5 or R_6. Therefore, the result is the picture of an ordinary ripple counter flip-flop.

Electrical lay-out - Two types of CS-flip-flops exist to meet different requirements.

Low frequency type:		
	R_C	1o k
	R_B	68 k
	R_E	39 k
	R_S	39 k
	C_B	33 pF
	C_s	33 pF
	C_Z	12 pF
	Tr 1,2	2 N 7o9
	Diodes	DY 6245

High frequency type:	R_C	3.3 k
	R_B	12 k
	R_E	6.8 k
	R_S	6.8
	C_B	3c pF
	C_S	12 pF
	C_Z	12 pF
	Tr 1,2	2 N 7o9
	Diodes	DY 6245.

c Performance

Low frequency type:	supply voltage	3v ± 2o %
	power consumption	1.3 mw
	max count frequency	6oo kc
	max shift frequency	3oo kc
	temperature range	-4o°C ... +8o°C
	input pulse	2 ... 2.5 v
		3oo nsec
	output pulse	2 ... 2.5 v
		12o nsec

High frequency type:	supply voltage	3v ± 2o %
	power consumption	3.3 mw
	max count frequency	3 mc
	max shift frequency	1.5 mc
	temperature range	-4o°C ... +8o°C
	input pulse	2 ... 2.5 v
		1oo nsec
	output pulse	2 ... 2.5 v
		5o nsec

d. Mechanical lay-out

Based on prototypes of DVL the CS-flip-flops have been manufactured by Telefunken in thick film technique (fig.14). One package contains two CS-flip-flops and has the following dimensions:

length	27 mm
height	13 mm
depth	3 mm.

e. Example for encoding system

Fig.15 shows the block diagram of a simple P04 encoder based on CS-registers. It consists of eight CS-registers, a buffer shift register and a central control electronics.

CS-register: Each register consists of 16 flip-flops. Count time is 0.022 sec, read out time 0.2 msec. The read out process of the second register starts 12.8 msec after that of the first; similarity, the time gaps between the read out processes of the other channels are multiples of 12.8 msec, giving a total cycle length of 8x12.8 msec = 0.1024 sec.

Buffer register: The read-out signal of the CS-register consists of eight 200/usec - bursts separated by a time zap of 12.6 msec. Each burst carries the information of a 16-stage binary number. In order to smooth out the pulse rate density equally over the cycle length a buffer is enclosed between the CS-register and the transmission line (p.e. FM/FM-telemetry). 8x16 pulses are now equally distributed over the 0.1024 sec cycle length giving a buffer shift pulse rate of 1.25 kc.

Control electronics: The control electronics driven by an880 kc clock provides the CS-register and the buffer with shift, reset, and countshift control pulses in the correct sequence. A glance on the block diagram (fig.16) shows the straightforward philosophy of the circuit and demonstrates the fact that the simplification of the basic register mechanism goes hand in hand with a reduction of the remaining electronics.

2.6. FEED-BACK-SHIFT-REGISTER Counting of binary events cannot only be performed by scalers, as described before, but by any type of storage system, which is able to uniquely map all numbers up to the maximum number of events to be counted.

As one technical solution which is of practical interest we will now discuss the linear feedback-shift-register.

The principle is shown in fig.17. 2^n different binary combinations are possible, if feedback is performed properly.* Therefore, a n-stage feedback-shift-register can be used to count up to 2^n binary events. Coding is in this case, of course, different from the common binary code. This might be a disadvantage. Of benefit is, that the content of the register can easily be obtained as a time sequence just by feeding n pulses into the clockline. So, read out is as simple as with counter-shift-registers. One has, however,

* "Analysis and synthesis of linear and non-linear shift register generators" by Thos. A. ROBERTS, International Telemetering Conference, London, 1963, Vol. 1, p. 390 - 399

take into account that for feedback-shift-registers all register stages must be designed for the maximum counting frequency.

The clockline needs a fan out of n because all clock inputs of the n flip-flops are connected.

As another feature the delay time for this counter is only $\Delta\tau$ instead of n $\Delta\tau$ by the ripple counter. All stages are switched simultaneously. This fact makes this counting especially useful for programmers, where delays between the individual steps may cause spikes at the output of connected gates; see fig.18.

2.7. DATA COMPRESSION BY FLOATING POINT REPRESENTATION In general, the encoding system connecting the outputs of the particle counting experiments with the transmitting system must be as simple as possible. That means the number of components, connections, etc. has to be a minimum.

However sometimes there may be good reason for data compression in the spacecraft itself, for example, limited transmitter power and storage capacity of the memory systems used. One straightforward method to compress the data is the conversion of numbers into a floating point representation. Here from the total number n of stages, only the very limited number m (mantissa) of binary stages (7 for example in the case of 1% accuracy) is requested, as far as accuracy is concerned. In addition, it is necessary to indicate the position of the most important bit $\neq 0$, i.e. the exponent. For a n stage register with m stages requested for a mantissa the exponent requires $\log_2(n-m)$ binary stages.

There are two conversion methods:

a. The binary events are counted as described above and converted into a logarithmic form after the parallel to serial conversion (sequential conversion).

b. The particles are counted directly in a logarithmic form (direct conversion).

2.7.1. SEQUENTIAL CONVERSION The binary sequence is shifted into a shiftregister with m-1 stages as shown in fig.19. An overflow of this register stops to shift the counting result and connects an additional scaler with the remaining clockpulses. This number of clock pulses equals (n-m) and determines the range of the mantissa. The register may have m-1 stages only, because the first value of the mantissa is 11111, in the most cases. If there is a “1” it is indicated in the exponent scaler. Mantissa and exponent can be read out in one of the ways described above.

2.7.2. DIRECT METHOD Counting directly in a logarithmic form can be done as shown in fig.20. A counter representing the mantissa counts every binary event until overflow occurs. This overflow switches a gate network in such a way that the mantissa scaler counts every second event now. The next overflow of the mantissa counter switches the gates again so, that the mantissa scaler counts every fourth event and so on. An additional scaler counts the number of overflows of the mantissa scaler and represents the range of the mantissa. Also this scaler is responsible for switching the gates in such a way that the input of the mantissa scaler is connected with the outputs of an additional counter. This counter is an usual binary counter.

To read out the counting result from both scalers - mantissa and exponent one of the methods described above can be used.

3. PCM ENCODING OF ANALOG SIGNALS So far we have only considered binary events. As there is a general tendency to transmit also analog signals in PCM one special case of increasing importance shall be discussed:

Conversion of CW-signals with large dynamic range. We will constrain ourselves to this case. With respect to the very interesting alternative, PCM encoding of analog pulse signals with large dynamic range, we only want to refer to[**]

3.1. SATURATING AMPLIFIER CONCEPT Conversion of the analog form into a digital format requires an A/D-converter whose unity step should be smaller than the smallest signal variation of interest. This variation is usually given by the dynamic signal range and its accuracy at the lowest amplitude. To convert a signal with a dynamic range of p-bits and an accuracy of m-bits we need a m+p bit ADC.

$$n = m+p$$

$m = \log_2$ of the accuracy
$p = \log_2$ of the dynamic range.

If m becomes large, much of the accuracy of the analog to digital converter is waisted, apart from the problems presented by high resolution ADCs in space environment.

The situation can be improved by using a logarithmic amplifier in front of the ADC in space environment, but:

[**] "A three parameter pulse height analyzer and coincidence system for satellite cosmic ray studies"; by S. Way, D. Stilwell, and S.L. Jones, IEEE Transactions on nuclear science, Febr. 1966, p. 523-532

a. a logarithmic amplifier contains non-linear analog elements of poor stability,

b. ADC accuracy is still waisted to accomodate the “exponential part” of the logarithmised signal.

Some kind of range switching will solve the problem. Simple voltage deviders are not feasible in space application since they diminish the dynamic range because of the input offset voltage and the output swing of the operational amplifiers being used.

The saturating amplifier concept (fig.21) uses several low amplifying (eight times for instance) stages in series. Depending on the magnitude of the input signal the amplifiers saturate one after the other, beginning with the last one. Saturation is sensed by Schmitt triggers and the last not saturated amplifier is gated to the ADC by an analog switch. The number of this amplifier is encoded. Since it specifies the magnitude of the signal, it may be regarded as exponent while the ADC generates the mantissa.

Fig.22 explains the situation for a two-stage amplifier with a stage amplification of 4. The broken line is obtained by joining the exponent as the most significant bits to the mantissa, It is a straight line approximation of the logarithm. The dynamic range of the mantissa output is equal to the stage amplification, since the next stage is switched on when the signal gets lower. The ADC has therefore to have n’ bits:

$$n' = A_1 + m$$

n’ = number of bits of the ADC using saturating amplifiers,
A_1 = dynamic range of one stage (bit) or 1092 of the stage amplification,
m = $\log_2$ of the required accuracy.

The total dynamic range is:

$$p = A_1 (M+l)$$

M =number of stages.

The relation between the number of bits gained in the ADC and the number of amplifying stages which enables to find the best combination is therefore:

$$n - n' = p+m - (_{A1+m}) = p-A_1$$
$$= A_1M$$

n-n’ = decrease of the required number of bits of the ADC.

As an example, a 3 stage amplifier with a stage amplification of 8, connected to a 10-bit ADC thus giving a 7-bit (o.8%) resolution over a 9-bit (1:512) range is under

development at DVL. The encoder is constructed in cooperation with Telefunken in thick-film technique.

3.2. A COMBINED RAMP SUCCESSIVE-APPROXIMATION ANALOG-TO-DIGITAL CONVERTER FOR SPACE APPLICATION In some cases, especially in space application, there is a need for a simple ADC resolving about 14 bits. Such an ADC may have quite poor long term stability, since the experimenter frequently uses the last bits of precision only to monitor the short time variations of the physical function to be investigated.

Under these circumstances, a conversion principle may be used as it is illustrated in fig.23. Two 3-bit ramp encoders (3-bits shown for simplicity reason) are connected in "series" to form a 6-bit ADC. The first encoder, called the coarse one, generates an ascending staircase, which is stopped as usual when it intersects the signal level. The difference between the signal and this level is fed to the second, the fine, ramp ADC, which has an input swing of one coarse step and which generates a descending staircase down to the signal level. Its starting pulse is derived from stop pulse of the coarse counter.

Fig.24 shows the block diagram for a combined converter consisting of two separate ramp ADCs using the same comparator. Two identical digital-to-analog converters are coupled over the resistor R, which reduces the voltage level. The DAC for the coarse steps must be eather of high precision, or a calibration table must be used for decoding. Since the fine counter counts in the opposite direction its output has to be inverted to form a normal binary word.

A considerable increase in speed over the pure ramp ADC results in using two ramps in series. For instance a 14 bit ramp has about 16000 steps (16384), whereas two 7 bit ramp ADCs have a total of 512 steps, i.e. a 1:64 decrease in aperture time can be gained.

A 14 bit combined ADC has been constructed by Telefunken to instrument the electronics of a satellite experiment made by DVL. The ADC consists of five thick-film flatpacks, as one ot which is shown in fig.25.

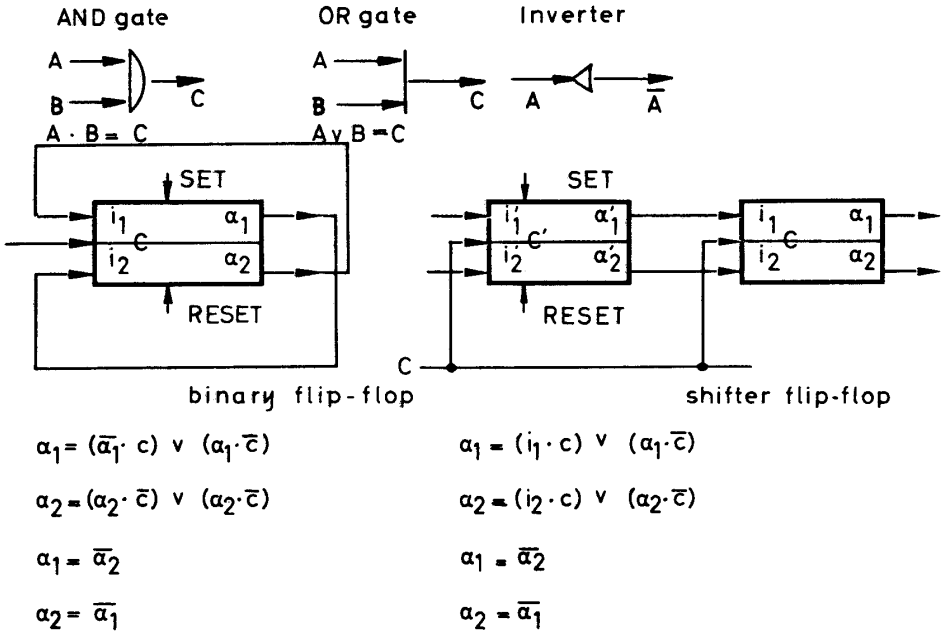


Figure 1 - Logical elements used

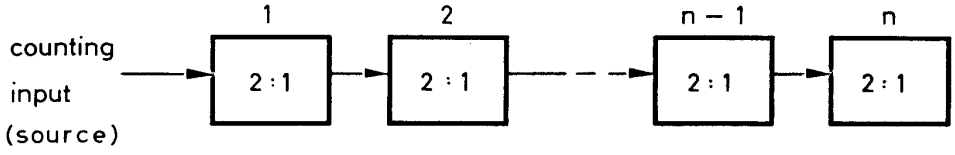


Figure 2 - Ripple Counter

n = number of stages

M = maximum counting result = 2"

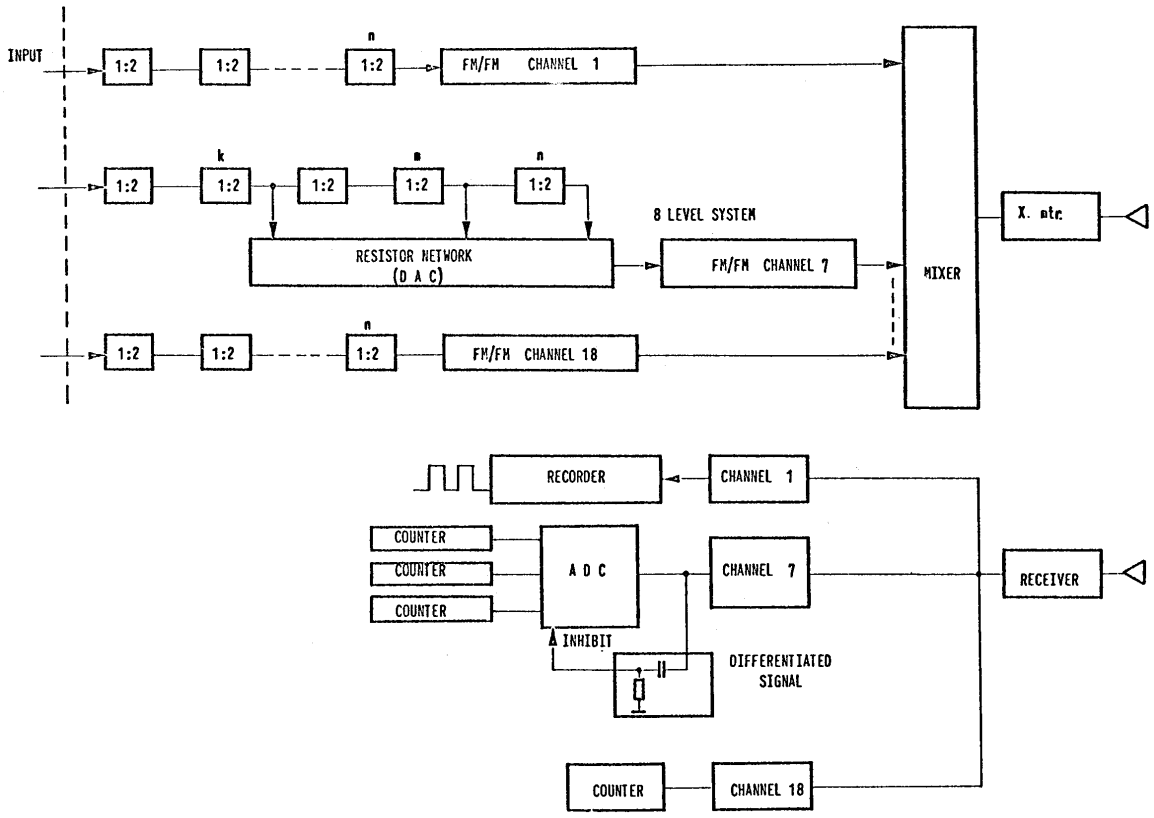
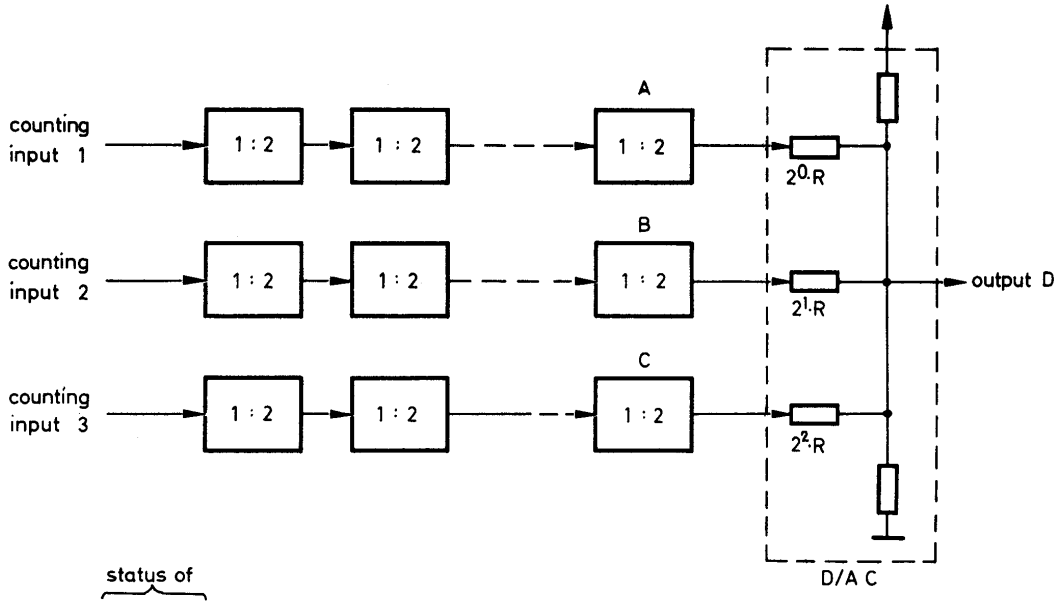


Figure 3



status of A B C	D for example
0 0 0	0,5
0 0 1	1,0
0 1 0	1,5
0 1 1	2,0
1 0 0	2,5
1 0 1	3,0
1 1 0	3,5
1 1 1	4.0

Figure 4 - Conversion from a binary to an 8 level system

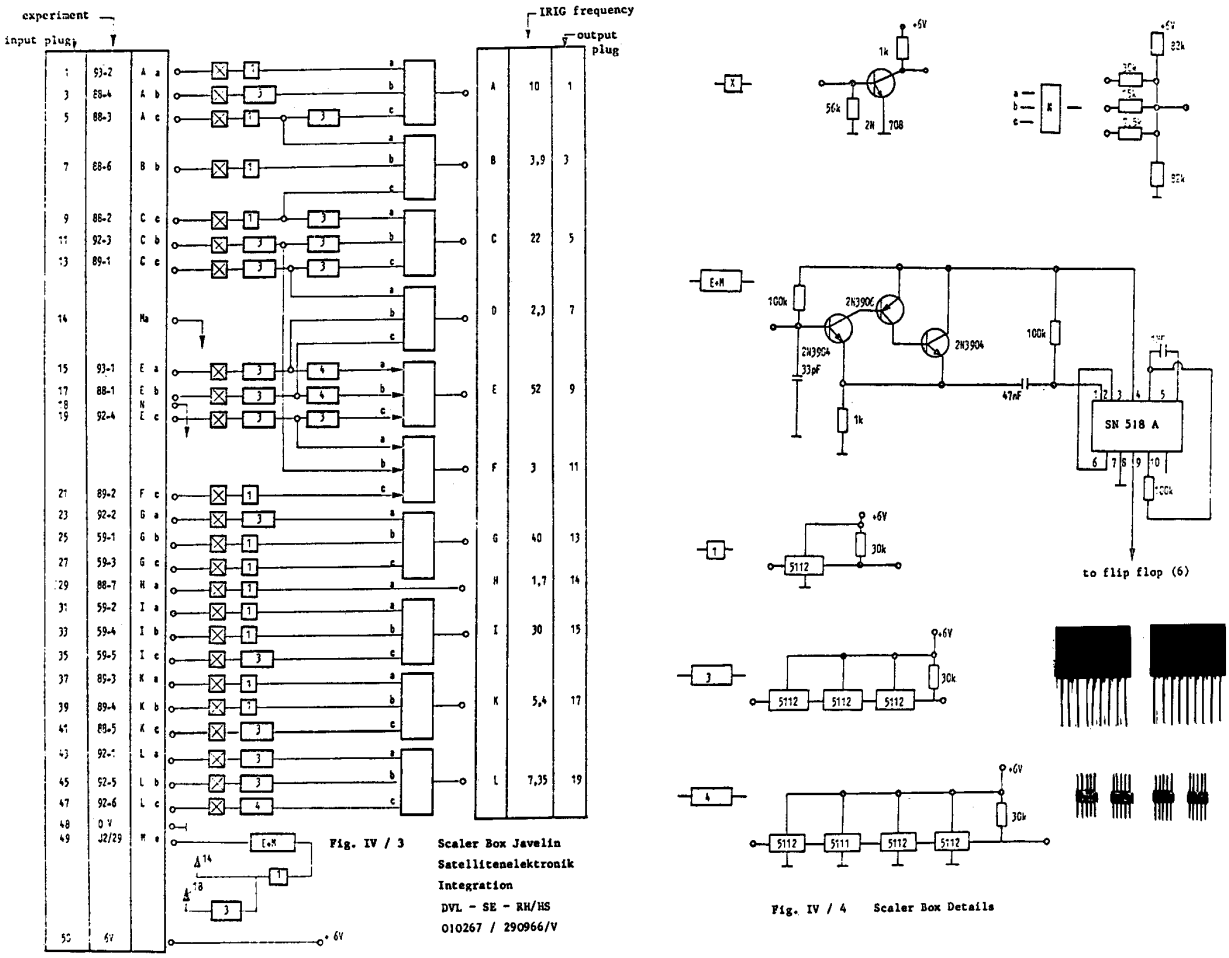


Figure 5 - 8 - Level Telemetry System

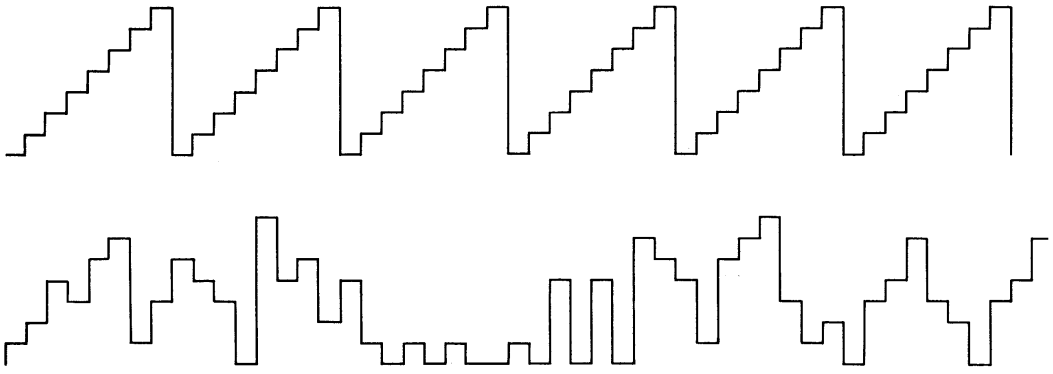
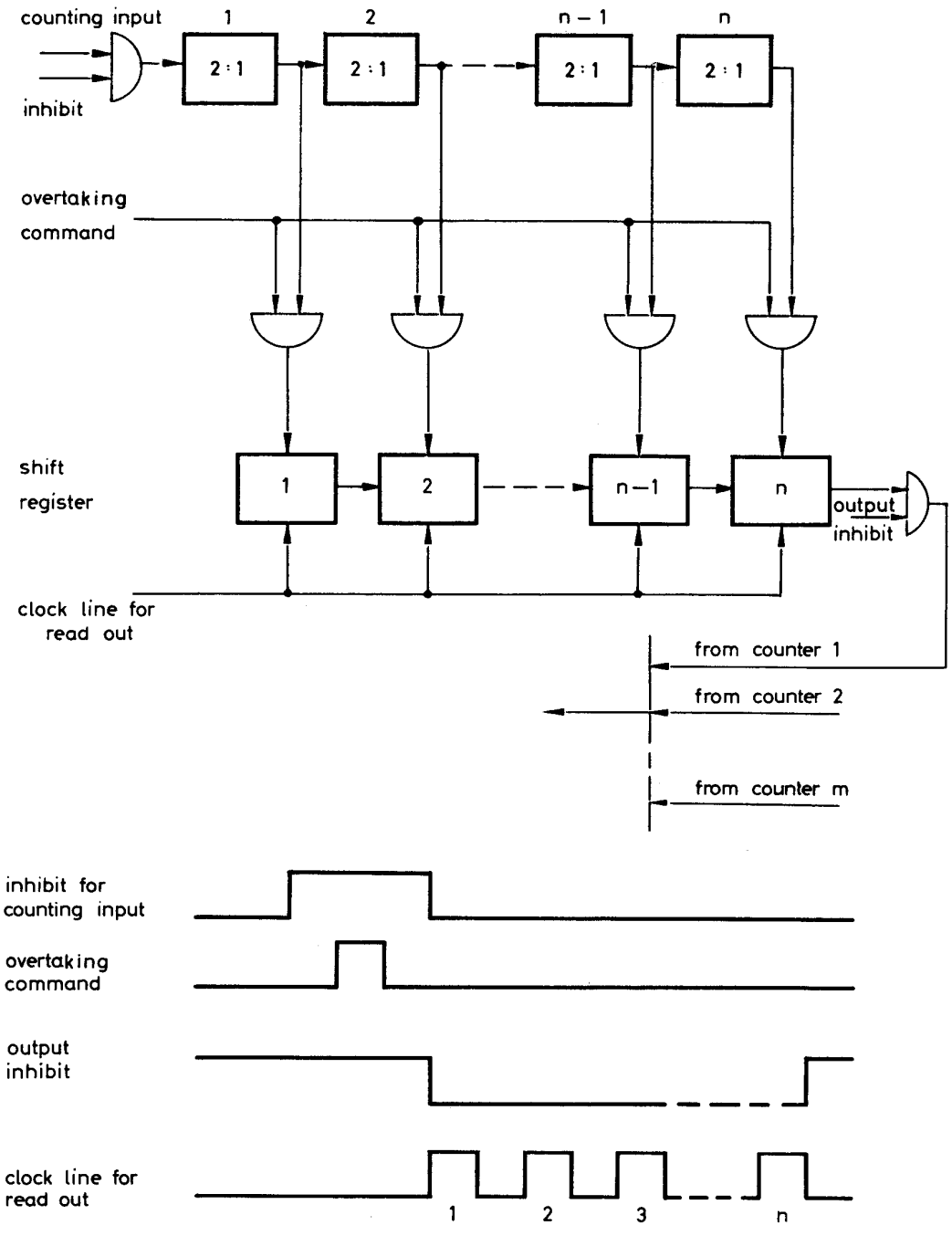


Figure 6 - Typical 8 - Level - Waveforms



pulse pattern for each of the m scalers

Figure 7 - Read Out System, Shiftregister

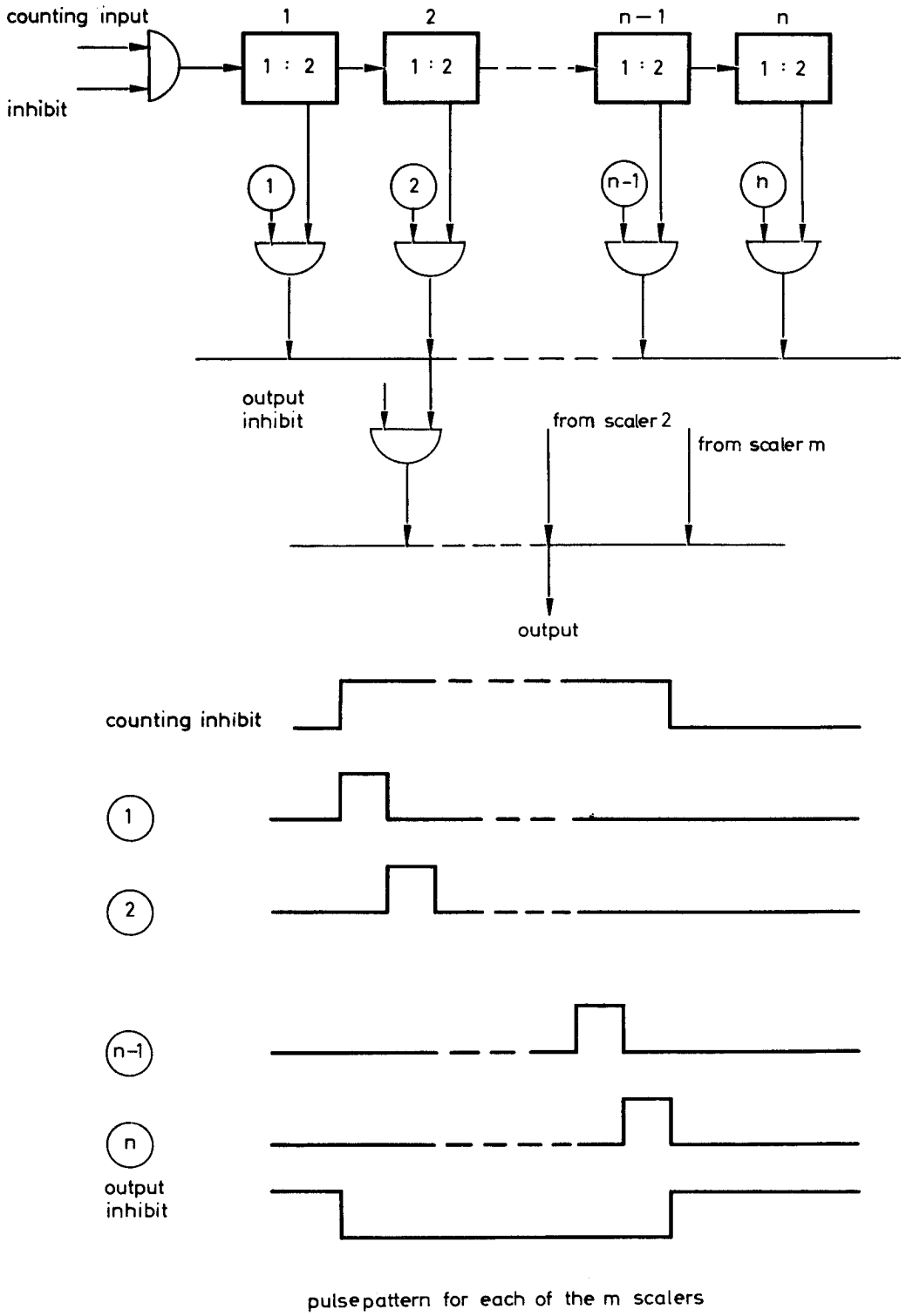


Figure 8 - Read Out Systems, OR - Gates

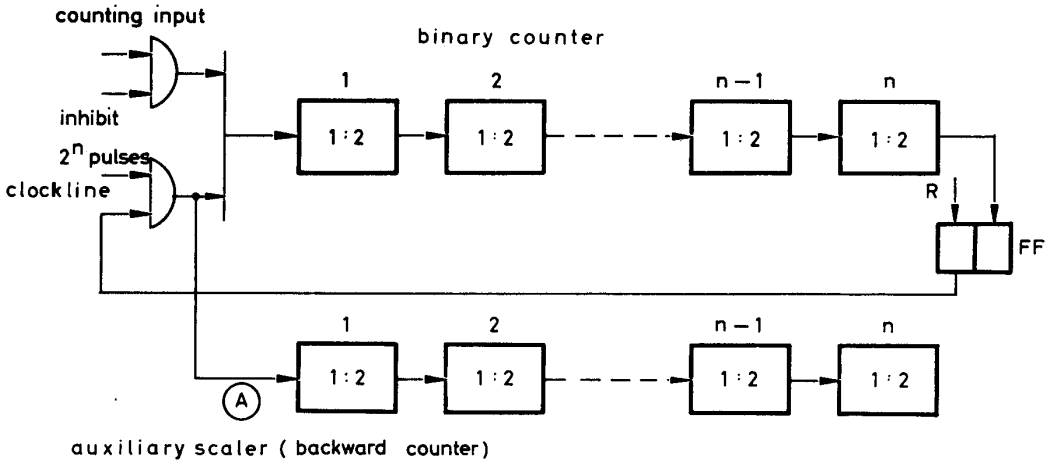


Fig. 9 Overflow System

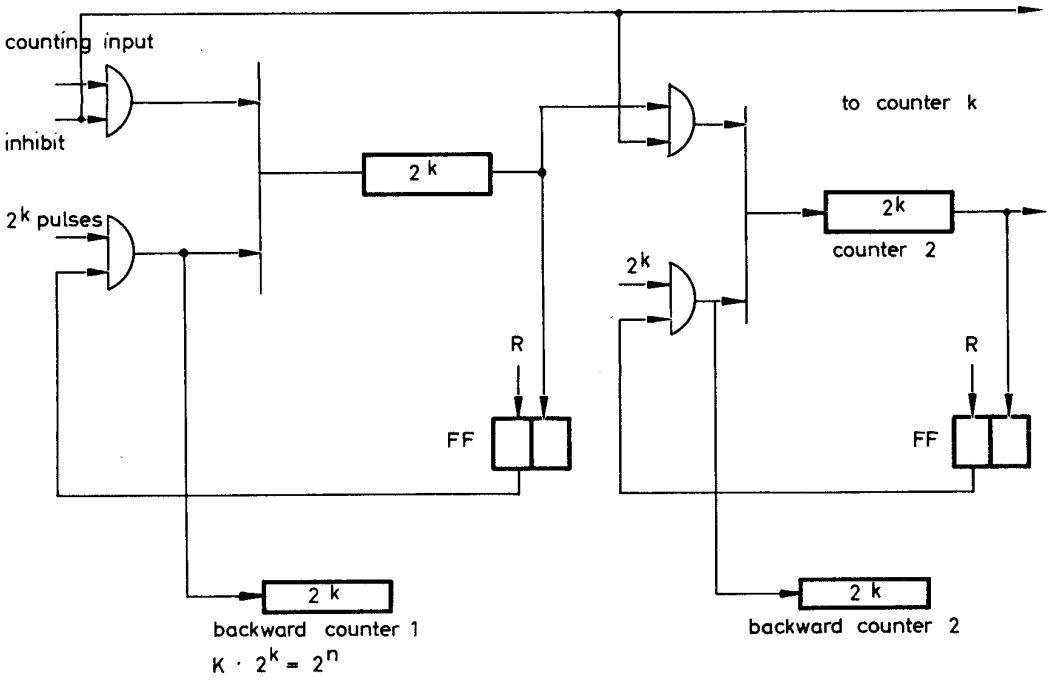


Figure 10 - Splitted Overflow System

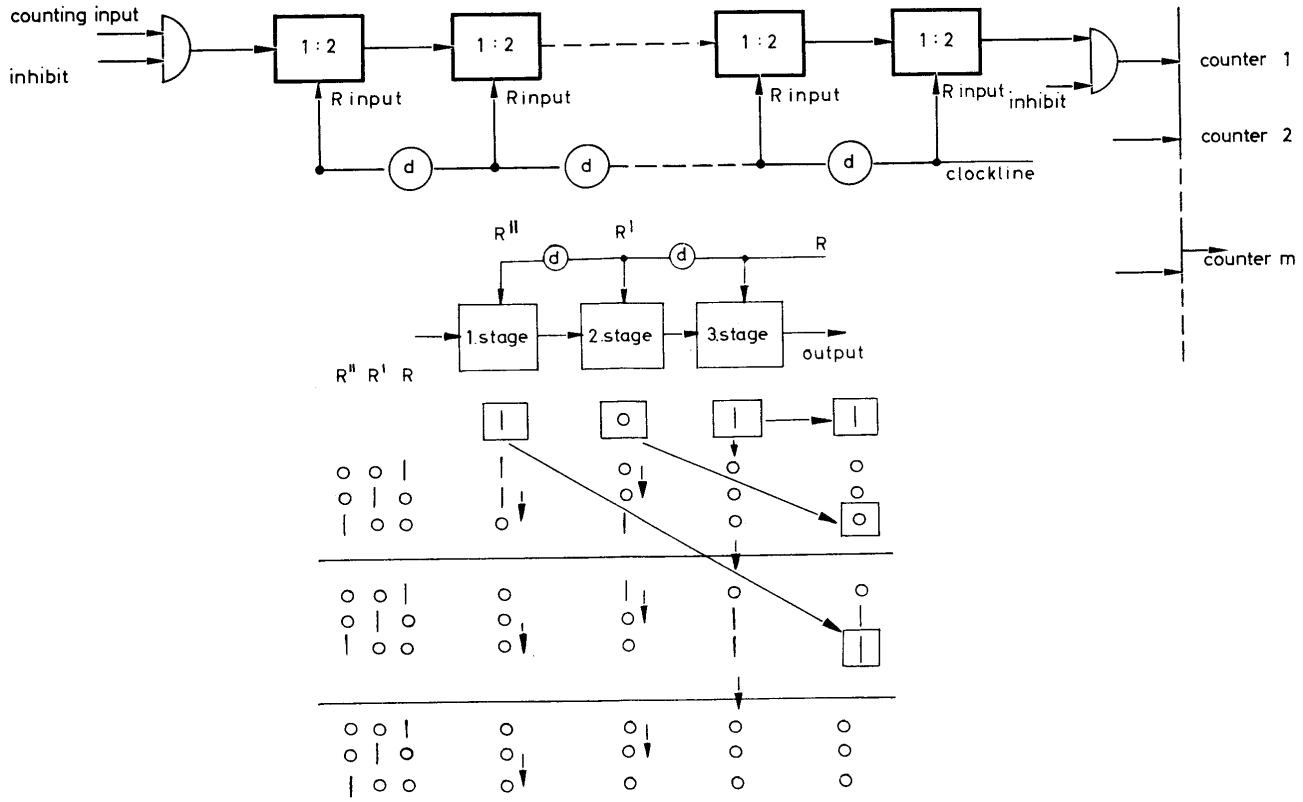


Figure 11 - Binary Counter with Delay Units

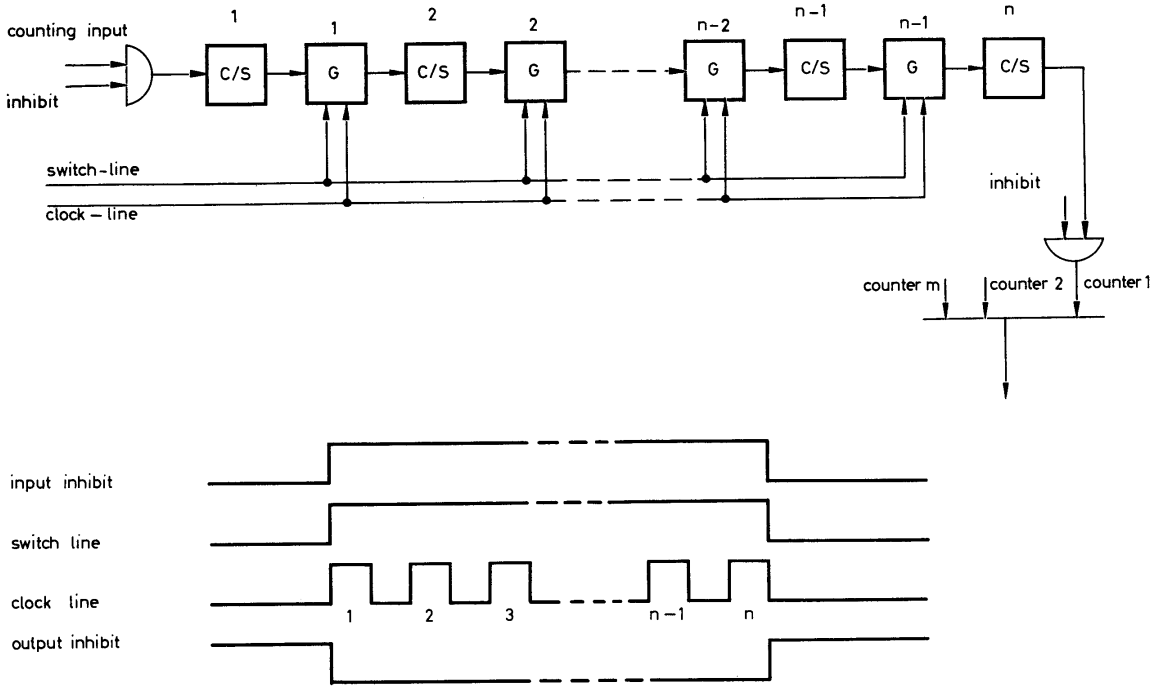


Figure 12 - Counter Shift Register

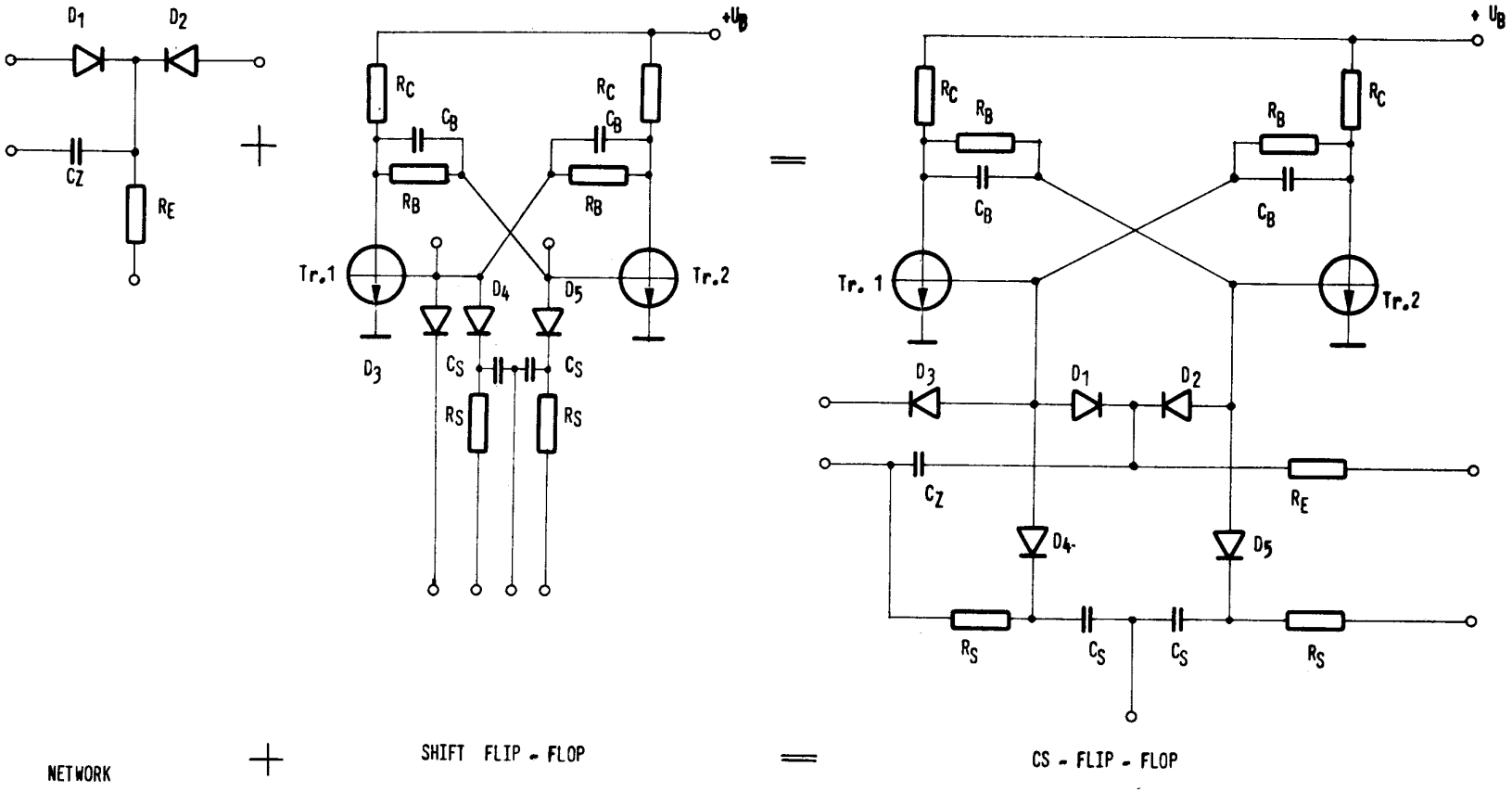


Figure 13 (a) **Figure 13 (b)** **Figure 13 (c)**

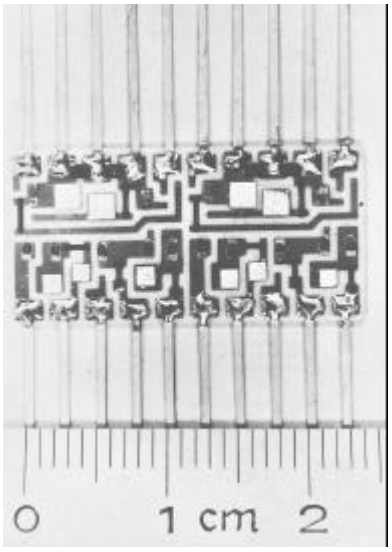


Figure 14 - Two C S - Flipflops
In Thick Film Technique (Telefunken)

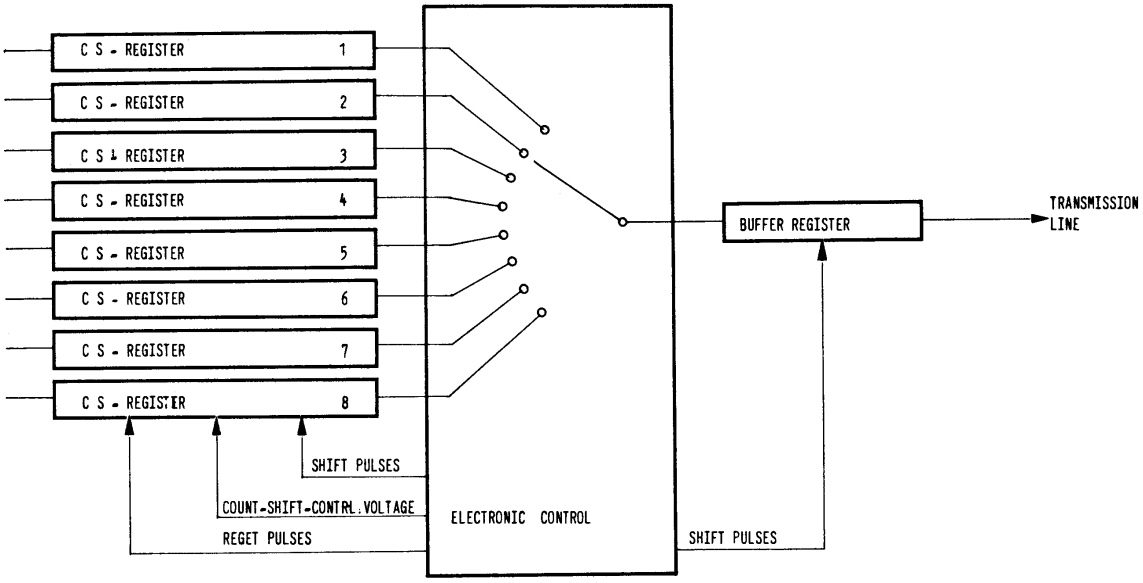


Figure 15

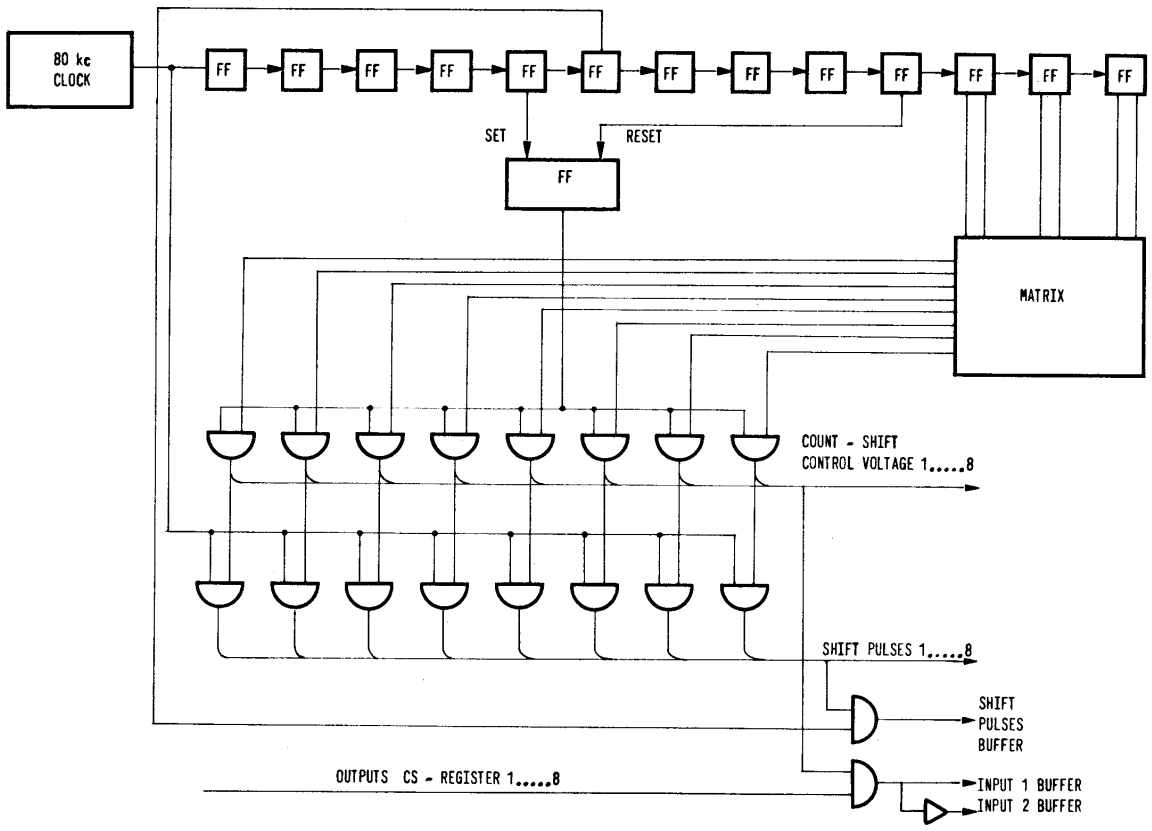


Figure 16

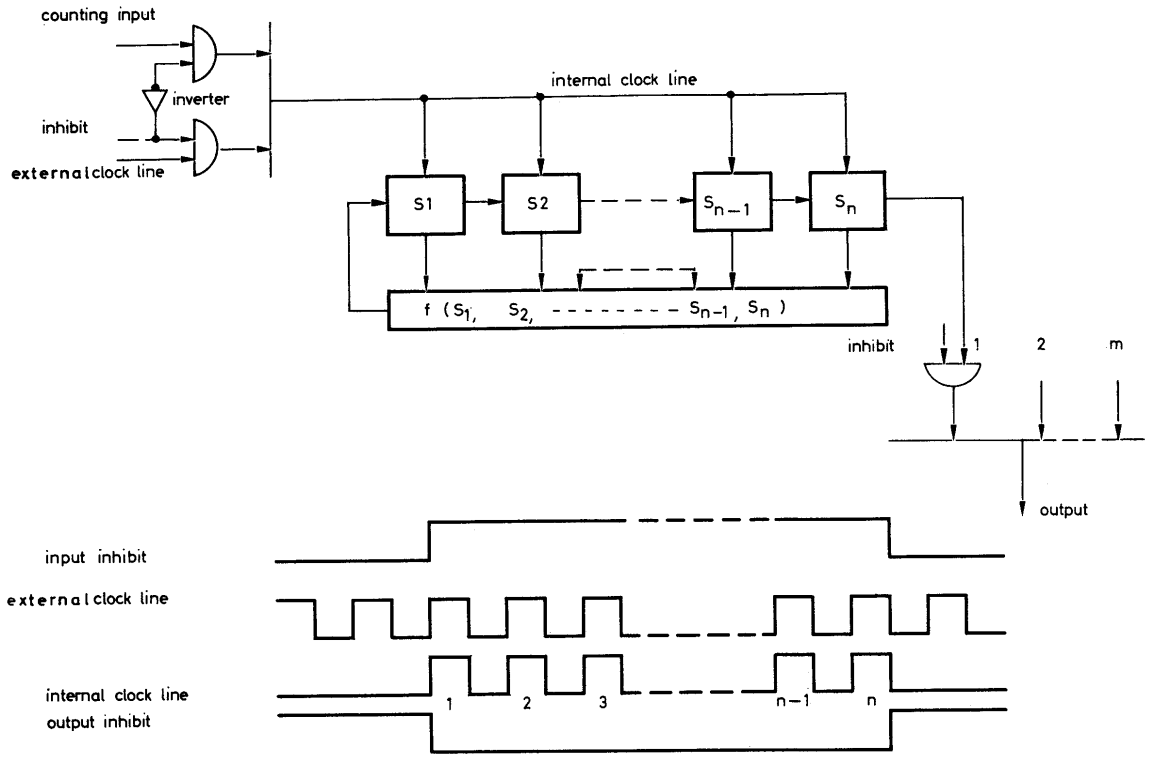


Figure 17 - Shiftregister with Feedback System

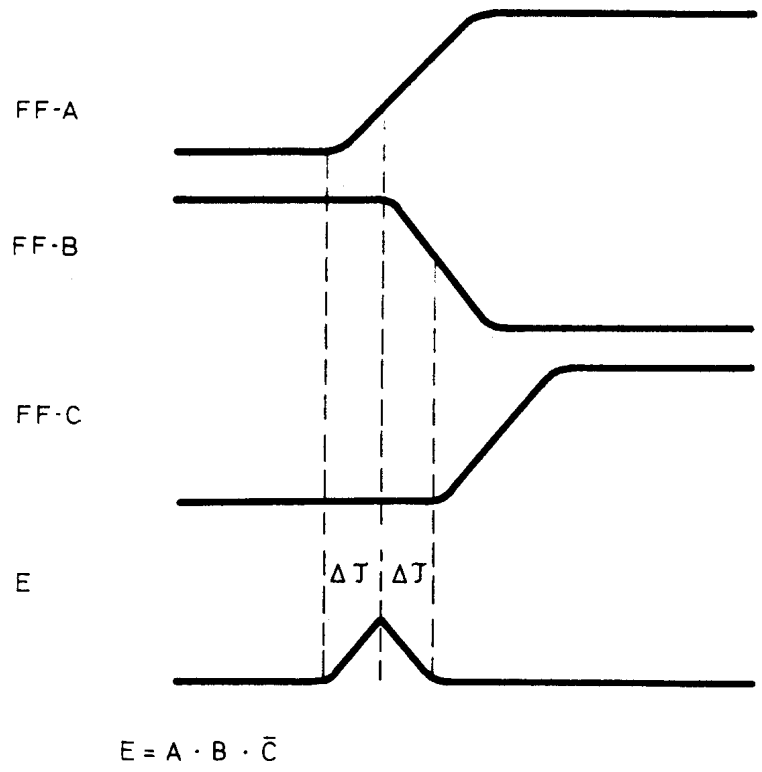


Fig 18 a - Spikes are generated (Binary Counter)

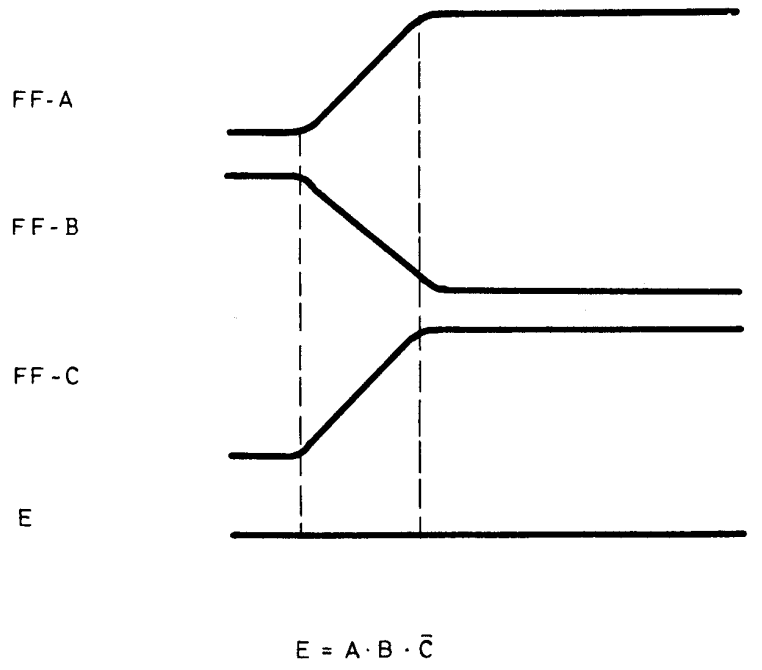


Figure 18 (b)- No Spikes are generated (Shiftregister)

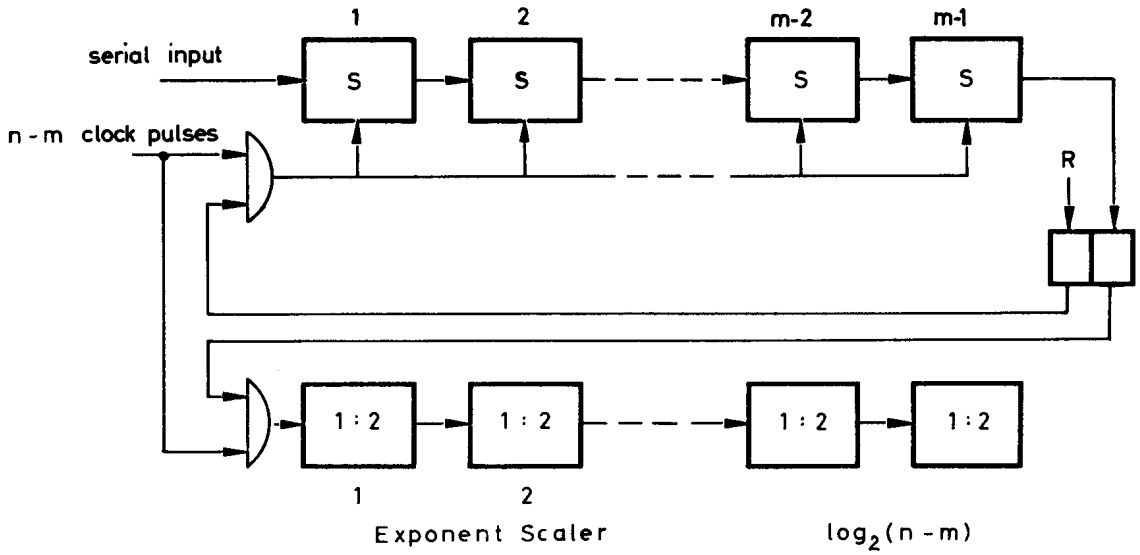


Figure 19 - Circuit for Logarithmic Compression

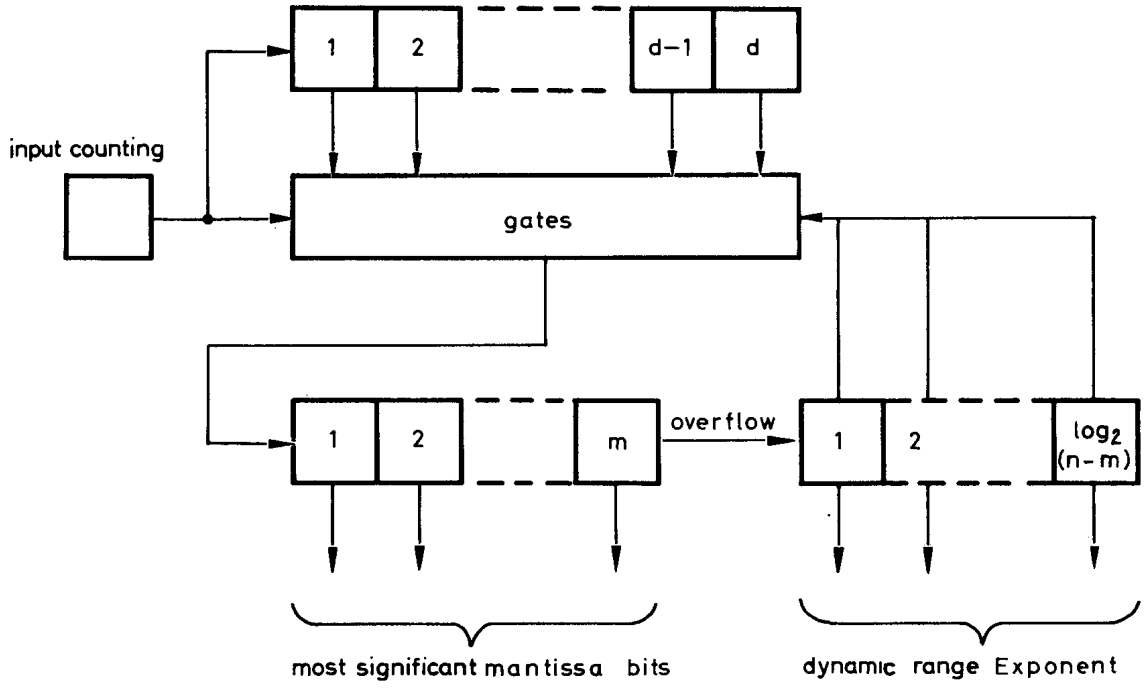


Figure 20 - Logarithmic Counting System

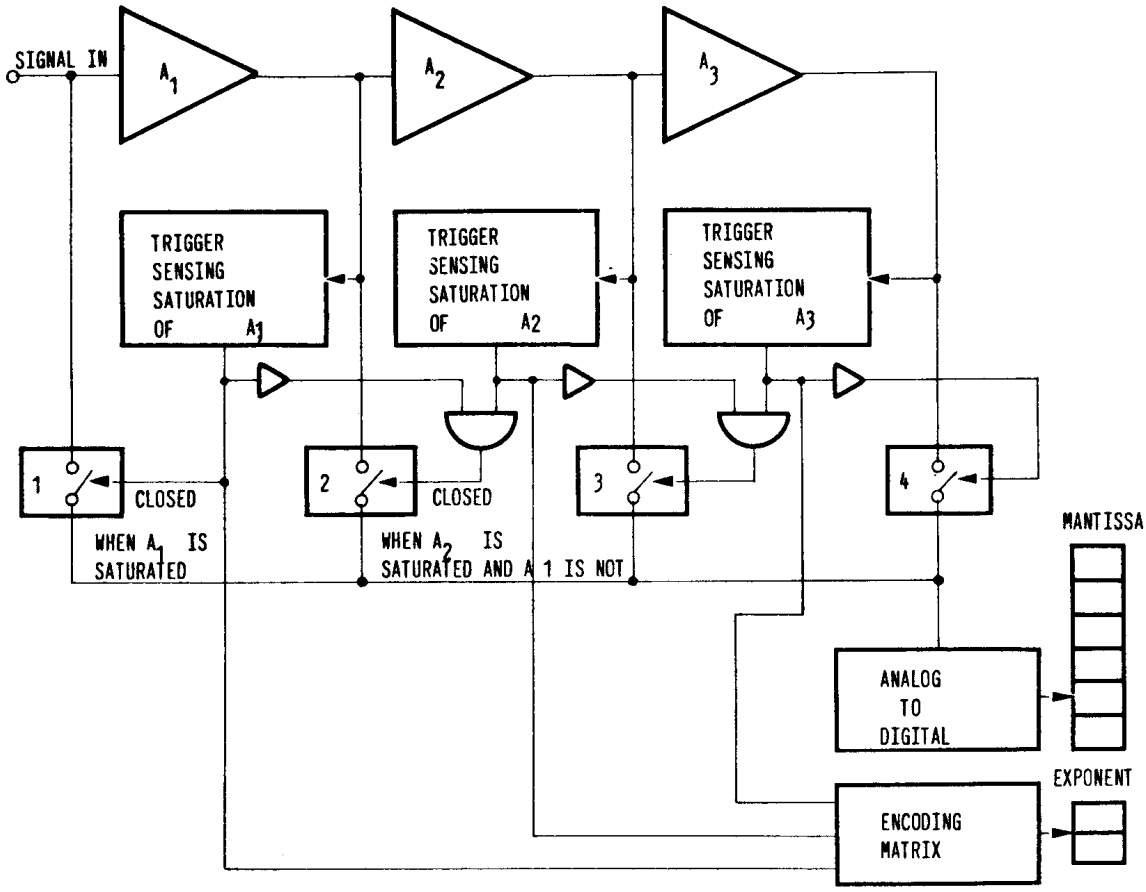


Figure 21 - The Saturating Amplifier Concept

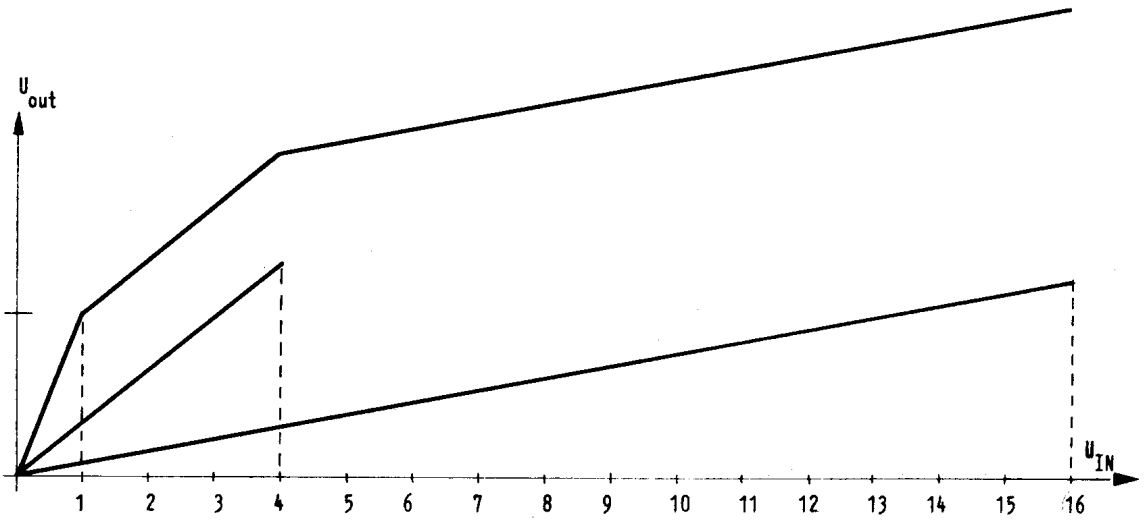


Figure 22 - Characteristics for a 2 Stage Saturating Amplifier with a Stage Amplification of 4 and Corresponding Straight - Line Approximation of the Logarithm

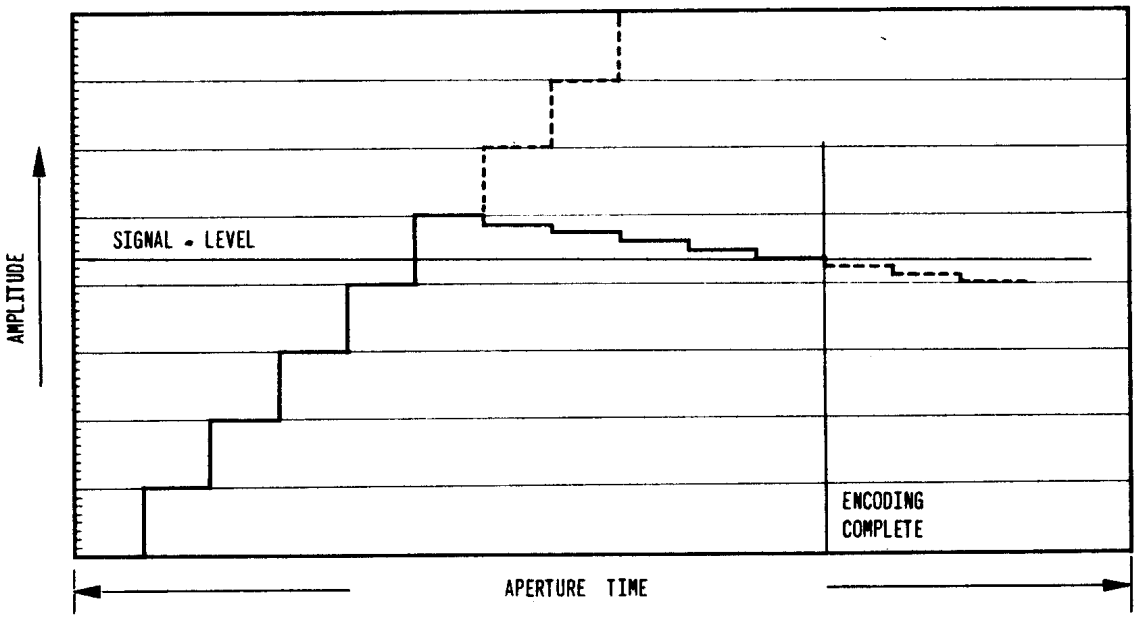


Figure 23 - 6 Bit Combined A D C Consisting of Two 3-bit Ramp ADCs

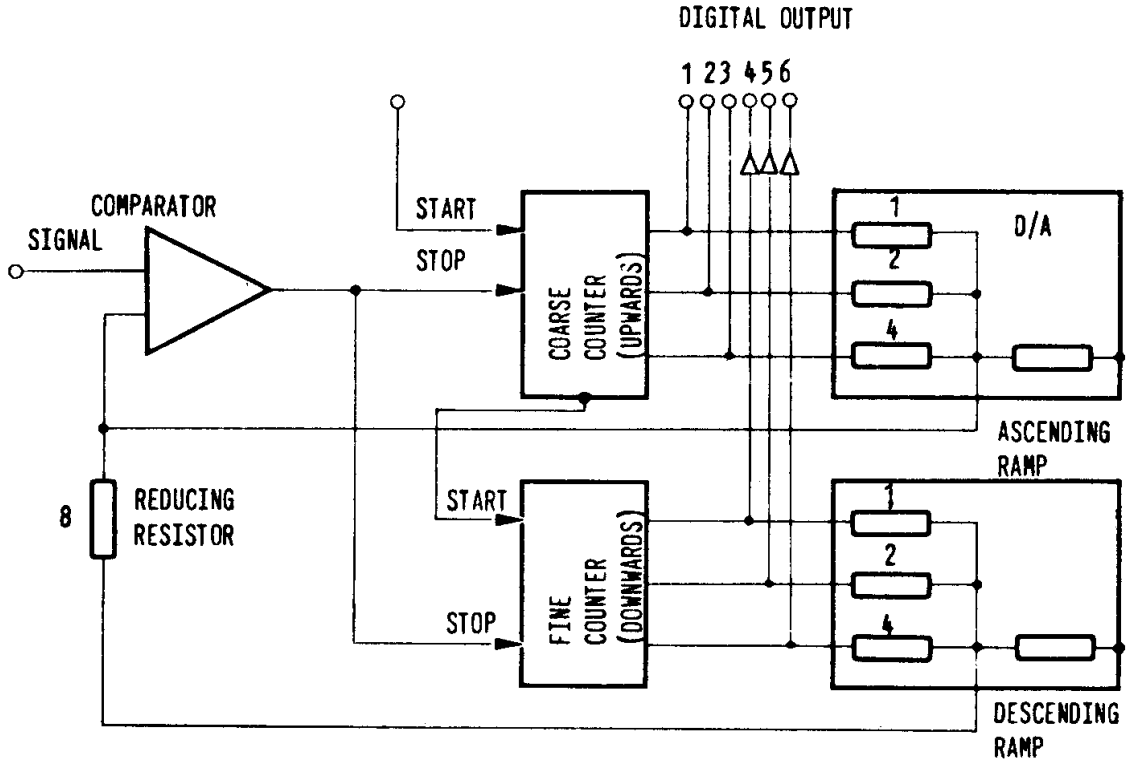


Figure 24 - Block Diagram of the Encoder

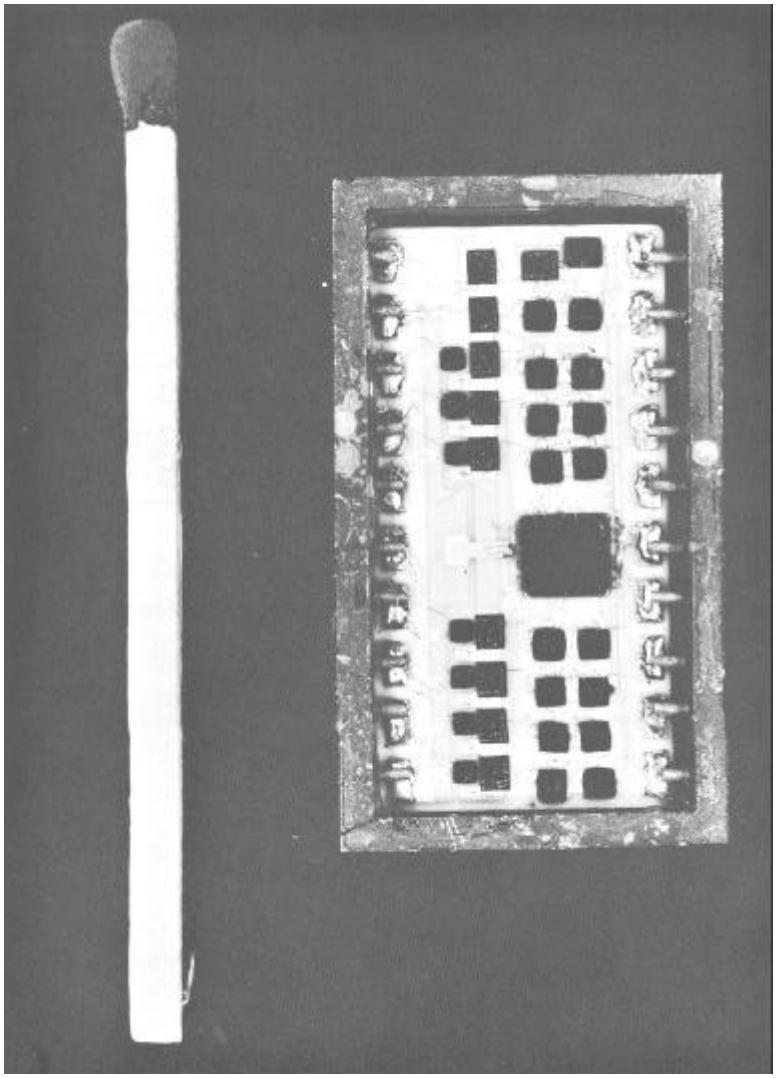


Figure 25 - One of the 5 Thick-Film Flatpacks Comprising a 14 Bit ADC