ADAPTIVE PCM PATTERN SYNCHRONIZATION

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Summary The trend toward more automated PCM decommutation systems demands less operator intervention in their operation. A weak link in this progression has been in the implementation of group synchronizer strategy. A new synchronizer has been developed based on the optimum properties of sequential probability ratio testing which requires only one program based on required worst case decision error probabilities and which is independent of the PCM format being synchronized. A mathematical model is formulated which accurately describes the operating characteristics of this technique. These operating characteristics are then compared to conventional synchronizer characteristics which demonstrate the superiority of this approach. The decision process described inherently adapts to signal conditions by making decisions faster and with less chance of error as bit error rate decreases. Only the Check Mode is discussed, but the same techniques apply to the Lock Mode.

Introduction Pattern synchronization of PCM formats is a statistical problem which must be solved before organized data can be supplied as an output from a telemetry ground system. The standard approach to solving this problem is to identify a probable synchronization word location in a Search mode and then to statistically verify the location to some criteria in a Check mode. Following verification, the Lock or Maintenance mode monitors the selected location against a separate criteria and reverts the System to Search when synchronization is lost. This paper develops a sequential probability ratio test (SPRT) decicision process for pattern synchronizers which makes decisions in less time and with greater probability of correct decision than conventional techniques. The SPRT is not format dependent and inherently adapts to bit error rate. As a result, the number of samples required to verify a sync location automatically decreases as the bit error rate decreases. Only the Check mode is considered but the same approach is directly applicable to the Lock mode. Also the SPRT technique may be used in Search mode if the data stream is word organized.

The decision process required in the Check Mode can be diagrammed as in Figure 1 . The pattern location being tested can be the correct location, (hypothesis H_1 true), or an

incorrect location, (hypothesis H_0 true). Testing can result in two kinds of errors; if H_1 is true there is a probability β that it will be rejected and if H_0 is true there is a probability α that it will be accepted. All decision processes are subject to the decision error probabilities α and β and the choice of one process over another should be made on the basis of the time required for completion of the test for a given strength (α, β). A faster, more efficient synchronizer decision process results in less loss of data.

Conventional synchronizers attempt to solve the synchronization problem by requiring sync patterns to meet a selected threshold tolerance a selected number of consecutive times. There are several disadvantages to this philosophy:

1. Detailed analyses must be made before proper error limits can be determined for near optimum synchronization under adverse and varying noise conditions.

2. The system is committed for a particular setup even though the actual noise environment encountered is better than the expected environment. This results in an unnecessarily long verification period (Check mode) and loss of frames of otherwise good data before the Lock mode is achieved.

3. Conventional synchronizer strategy is format dependent because of the group-by-group techniques employed in standard synchronizer mode logic. The statistical decisions required of group synchronizers, however, do not have any inherent format dependence.

The last statement is the key to the limitations of conventional techniques. By using serial pattern correlation the problem reduces to making decisions on serial digital sequences which appear the same to the synchronizer regardless of the format.

Sequential Probability Ratio Test (SPRT) Wald[1] has shown that a SPRT of strength (α, β) for testing hypothesis Hi against an alternate hypothesis Ho is defined by the inequality

$$\frac{\alpha}{1-\beta} < \frac{P_{1n}}{P_{0n}} < \frac{1-\alpha}{\beta} \quad . \tag{1}$$

P_{in} is the probability that H_1 is true after " n" samples and P_{0n} is the probability that H_0 is true after " n" samples. For each " n" the probability ratio is evaluated and compared to the inequality bounds. If the probability ratio after the " nth" sample equals or exceeds $(1-\alpha)/\beta$ then H_1 is accepted. Likewise, if the probability ratio is less than or equal to $\alpha/1-\beta$, H_0 is accepted. If neither of the inequality bounds is met then another sample is

[1] Abraham Wald, "Sequential Analysis", John Wiley and Sons, Inc., New York, N.Y., 1947

taken and the decision process is repeated. Wald and Wolfowitz[2] have proved that no test of strength (α, β) can be devised that requires fewer average number of samples " n" than the SPRT.

In the case of PCM pattern synchronization, H_1 is the hypothesis that the pattern being tested is the true pattern with a bit error probability of ϵ and H_0 is the hypothesis that the pattern being tested is from the data stream. If random data and synchronization patterns with statistically independent bit errors are assumed then the probability functions P_{0n} and P_{1n} are described by binominal functions. Using these assumptions, after " n" samples of serial pattern correlation ΣJ errors occur and $\Sigma I = n-\Sigma J$ bits correlate, the SPRT is defined by the inequality

$$\frac{\alpha}{1-\beta} < \frac{\epsilon_0^{\Sigma J}(1-\epsilon_0)^{\Sigma I}}{(.5)^{\Sigma J}(1-.5)^{\Sigma I}} < \frac{1-\alpha}{\beta} \quad . \tag{2}$$

Taking the logarithm of (2) and dividing by $1n\ 2(1-\epsilon_0)$ results in

$$\frac{1n\ \frac{\alpha}{1-\beta}}{1n\ 2(1-\epsilon_0)} < \Sigma I + \frac{1n\ 2\epsilon_0}{1n\ 2(1-\epsilon_0)}\ \Sigma J < \frac{1n\ \frac{1-\alpha}{\beta}}{1n\ 2(1-\epsilon_0)} \quad . \tag{3}$$

Note that α and β, the two required decision error probabilities, are constants and ϵ_0 is the worst case bit error rate of the input data, also a constant. When α and β are made equal the result is

$$-L < \Sigma I - K\Sigma J < +L \quad , \tag{4}$$

where

$$L = \frac{1n\ \frac{1-\alpha}{\beta}}{1n\ 2(1-\epsilon_0)} = -\frac{1n\ \frac{\alpha}{1-\beta}}{1n\ 2(1-\epsilon_0)} \quad , \tag{5}$$

and

$$K = -\frac{1n\ 2\epsilon_0}{1n\ 2(1-\epsilon_0)} \quad . \tag{6}$$

Figure 2 plots K as a function of ϵ_0. Typical PCM systems require syncronization capability of formats with bit error rates approaching 10%. Hardware simplicity suggests

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[2] A. Wald and J. Wolfowitz, " Optimum Character of the Sequential Probability Ratio Sequential Test" , Ann. Math. Stat. , Volume 19, pp 326-339; 1948

that constants K and L be restricted to integers. Therefore, K is chosen as 3 corresponding to worst case bit error rates ϵ_0 of 8%. L is readily computed from (5).

The decision process of the sequential probability ratio test defined by (4) above is described as follows. Each bit correlation increments an accumulator by one and each bit error decrements an accumulator by K. The resultant total is compared to the limits ± L. If +L is equalled or exceeded a " Go to Lock" (accept H_1) decision is made and if the total is less than or equal to -L a "Return to Search" or reject decision (accept H_0) is made. if the inequality bounds are not exceeded another pattern bit is tested and the process repeats. Figure 3 is a flow chart of this decision process. The block diagram of the hardware required to implement the SPRT is shown in Figure 4 and is basically an arithmetic accumulator with a limit detector.

Operating Characteristics of the SPRT The preceding discussion presents the foundation for sequential probability ratio testing as applied to PCM pattern synchronization. Additional information is required in order to compare SPRT with conventional synchronizer strategy. How many sync pattern bits must be tested before a decision is made and how do error rates other than the worst case error rate ϵ_0. effect the operation? Approximate answers of these questions can be derived by extending the previous results. Study of (4) reveals, however, that this SPRT is directly analogous to classical one dimensional random walk problems. Solutions to these problems are readily computed using matrix techniques.

The matrix representation of the SPRT is

$$[S_{ij}]^n \; [{}_0C_k] = [S_{ij}] \; [{}_{n-1}C_k] = [{}_nC_k] \quad , \tag{7}$$

where: n = sample number being tested,

i, j, k have values between $+L$ and $-L$,

$${}_0C_k = \begin{cases} 1, & k = 0 \\ 0, & k \neq 0 \end{cases} ,$$

$$S_{i,j} = 1, \quad i = j = L \text{ or } -L ,$$

$$S_{i,i-1} = \begin{cases} 1-\epsilon, & i \neq -L \text{ or } -L+1 , \\ 0, & i = -L+1 , \end{cases}$$

$$S_{i,i+K} = \epsilon, \quad -L+1 \leq i \leq L-K-1,$$

$$S_{-L,j} = \epsilon, \quad -L+1 \leq j \leq -L+K,$$

and all other entries are 0.

Matrices $[S_{ij}]$ and $[{}_0C_k]$ are constructed in FigLire 5 for the case L = 8 and K = 3. Each element ${}_nC_k$ in the column matrix $[{}_nC_k]$ is the probability that the sequential tester has a count of k after the nth sample has been tested. Thus ${}_nC_L$ is the cumulative probability than an accept decision has been made by the nth sample and ${}_nC_{-L}$ is the cumulative probability that a reject decision has been made.

The values ${}_nC_L$ and ${}_nC_{-L}$ for various weighting factors K and limits L have been computed using a digital computer. The limiting values of these parameters correspond to and 1-β and β respectively when the true sync (ϵ = bit error rate) location is being tested and to α and 1-α respectively when random data (ϵ = . 5) is being tested. Figure 6 plots β and α computed from this model versus limit L for the case K = 3 and the actual bit error rate equals 8%.

Also plotted is α and β versus L predicted by analysis (equation 5) for the same conditions. The third characteristic is a convenient approximation to any of these curves. The approximation is justified on the basis that test control is required only for order of magnitude change in decision error probability and therefore the little differences in the curves can be neglected. Thus the approximation curve is a conservative estimate of the decision error probability for the stated conditions. Note that each increment of 4 results, very nearly, in an order of magnitude change of decision error probability. By restricting the limits ± L of sequential testing to multiples of 4 and defining the programmed limit P_L = .25L, the decision error probability can be approximated by

$$\alpha = \beta = 10^{-P_L} \quad \text{for } K = 3, \ \epsilon = 8\%. \tag{8}$$

As stated earlier there is no PCM format dependence in sequential testing. Selecting K = 3 in the hardware design of the SPRT, the only synchronizer strategy required is selection of P_L. The selection of the worst case decision error rate bound follows from equation (8). If a and p are required to be 10^{-3} or 10^{-6}, P_L is simply 3 or 6.

The cumulative probability of decision error as a function the number of bits checked n is plotted in Figure 7 for the conditions K = 3, P_L = 3 and ϵ = .5 (data stream), . 08, . 05, and . 01 to a resolution of $\leq 1 \times 10^{-4}$. The adaptive nature of sequential testing is apparent from these curves. If the actual bit error rate decreases from the worst case error rate Eo = 8%, decisions are made faster (fewer bits checked) and with less chance of error (β decreases). The test is not committed for a certain length of time (bits or patterns checked). Even at ϵ = 8% these is a 35% probability that a correct accept decision will be made by testing only 12 bits.

Figure 8 plots cumulative probabilities of decisions as a function of n for $\epsilon = 8\%$ and different programmed limits P_L. The effect of increased P_L is to increase the number of bits tested for the same probability of decision but to decrease β. Convenient approximations to n for given cumulative probabilities of correct decision (H_1 true) are indicated by the dotted contours.

Comparison of Sequential Testing With Conventional Synchronizer Strategy

Conventional synchronizer strategy in the Check Mode requires each of X consecutive patterns to correlate within τ errors for a " Go to Lock" decision. Any pattern with more than τ errors causes a " Return to Search" decision. If $P_{1,\tau,\epsilon}$ is defined as the probability that the true pattern (H_1 true) with an error rate of ϵ has τ of fewer errors and $P_{0,\tau,.5}$ is defined as the probability that a location in the data stream (H_0 true) has T or fewer errors then

$$\beta = 1 - \left[P_{1,\tau,\epsilon}\right]^X , \tag{9}$$

and

$$\alpha = \left[P_{0,\tau,.5}\right]^X ,$$

where

$$P_{1,\tau,\epsilon} = \sum_{i=0}^{\tau} \binom{\ell}{i} (1-\epsilon)^{\ell - i} \epsilon^i ,$$

and

$$P_{0,\tau,.5} = \sum_{j=0}^{\tau} \binom{\ell}{i} [.5]^{\ell} ,$$

and

ℓ = pattern length.

Using these relationships, X and τ can generally be determined for a required test strength of (α, β).

The following minimum settings are required in a conventional synchronizer at an 8% bit error rate for maximum α and β of 10^{-3} and 10^{-4} .

TABLE I.
Conventional Synchronizer Settings for
Given Test Strength (α, β)

Format 1	Conventional Synchronizer Settings			
	α and $\beta = 10^{-3}$ max.		α and $\beta = 10^{-4}$ max.	
	τ Errors	X Frames	τ Errors	X Frames
16-bit pattern	6	5	10	10
24-bit pattern	7	2	9	4

Corresponding strategy of the sequential tester is simply $P_L = 3$ or 4. Note that initialization of the sequential tester is independent of format (pattern length). Speed of the sequential test is indicated in Tables II and III.

TABLE II.
Sequential Test Speed at 8% Bit Error Rate

Format 1	% of Tests Complete	
	α and $\beta = 10^{-3}$ max. $P_L = 3$	α and $\beta = 10^{-4}$ max. $P_L = 4$
16-bit pattern	64% in 1 frame 97% in 2 frames 99.8% in 3 frames	26% in 1 frame 90% in 2 frames 99% in 3 frames
24-bit pattern	90% in 1 frame 99.8% in 2 frames	71% in 1 frame 99% in 2 frames

TABLE III.
Sequential Test Speed at 1% Bit Error Rate

Format	% of Tests Complete	
	α and $\beta = 10^{-3}$ max. $P_L = 3$	α and $\beta = 10^{-4}$ max. $P_L = 4$
16-bit pattern	99% in 1 frame	85% in 1 frame 99.999% in 2 frames
24-bit pattern	99.99 % in 1 frame	99.8% in 1 frame

Conventional synchronizers are commited to test for X frames for an accept HI decision regardless of the incoming bit error rate whereas the sequential tester will adapt by making faster and " surer" accept decisions as the error rate decreases.

Conclusions The mathematical foundation for the design of a probability ratio sequential tester applied to PCM pattern synchronization has been presented and a model was formulated which describes the operating characteristics. These characteristics, when compared with conventional synchronizer strategy can be summed up as follows:

1. Sequential tester decisions are made much faster, on the average, than with conventional techniques.
2. Sequential testers inherently adapt to the signal quality conditions eliminating the requirement for operator intervention during operation for optimum performance.
3. Only one program is required for sequential tester initialization and that program is directly derived from required worst case decision error probabilities.
4. Initialization of the sequential tester is independent of format parameters.
5. More synchronized data is available for output because of the faster decisions.

While only application of sequential testing to synchronizer Check mode has been discussed, these same techniques can be applied to other modes and digital test problems such as data quality testing.

Acknowledgment The author wishes to acknowledge the contributions of his associates at Dynatronics which led to this development and in particular to P. Mallory for many valuable discussions and suggestion of the matrix model.

	H_1 True	H_0 True
Accept Decision	$1-\beta$	α
Reject Decision	β	$1-\alpha$

Fig. 1 - Synchronizer Decision Probabilities

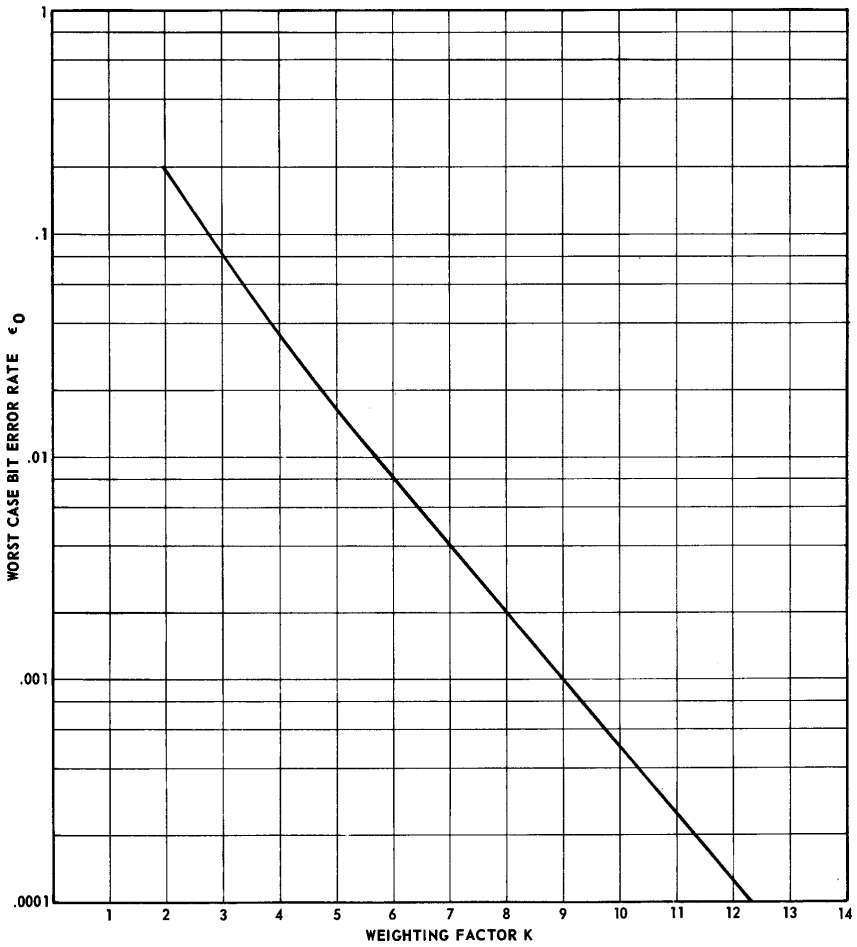

Fig. 2 - Weighting Factor K as Function of Worst Case Bit Error Rate

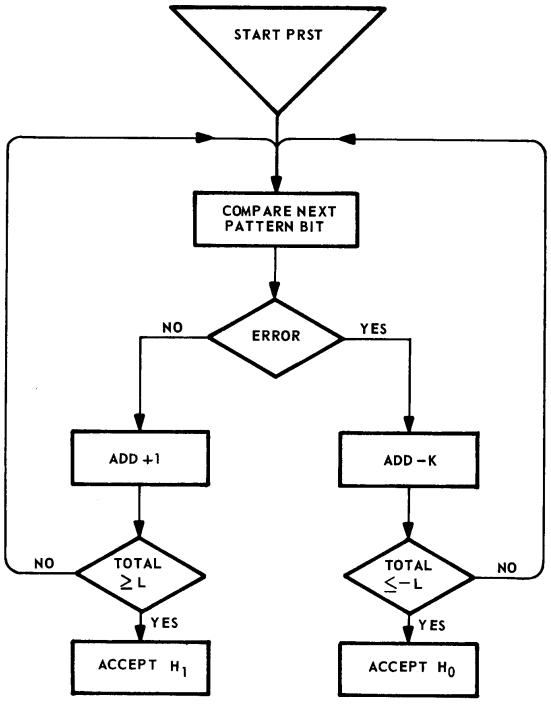

Fig. 3 - SPRT Flow Chart

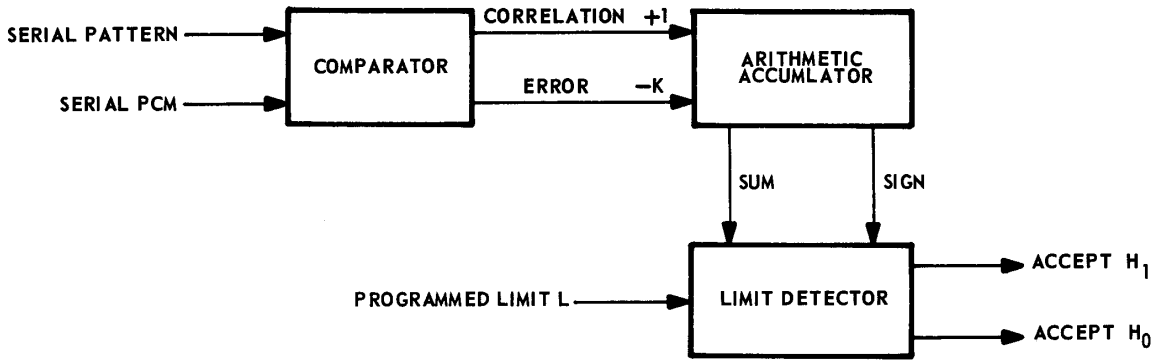

Fig. 4 - SPRT Block Diagram

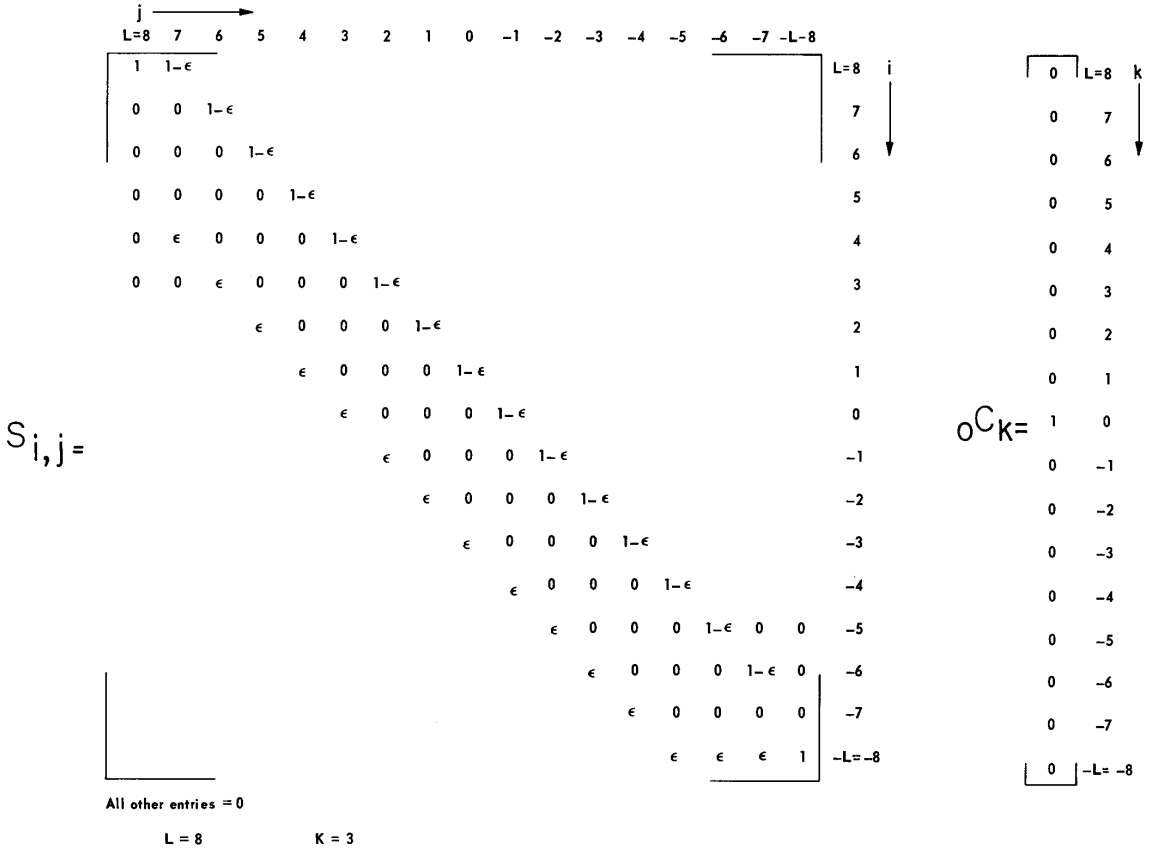

Fig. 5 - SPRT Matrices

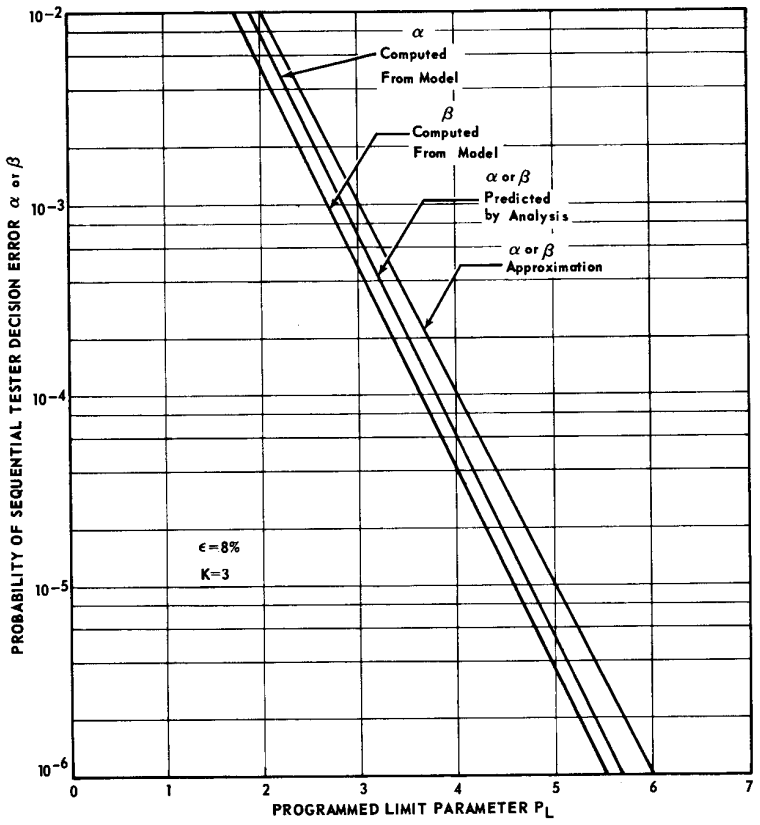

Fig. 6 - α and β as Function of Programmed Limit Parameter P_L

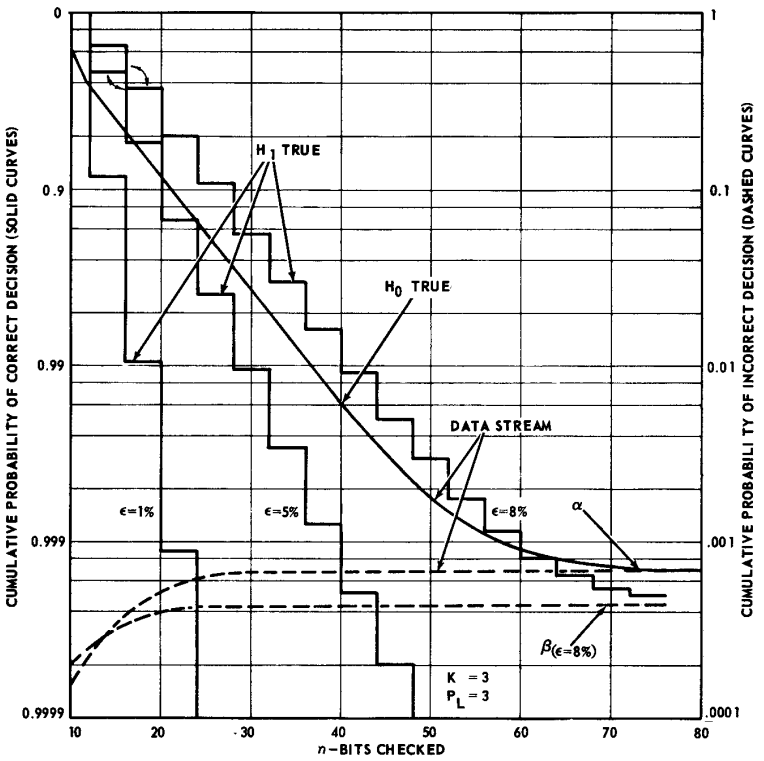

Fig. 7 - SPRT Decision Speed for Different Error Rates and K=3

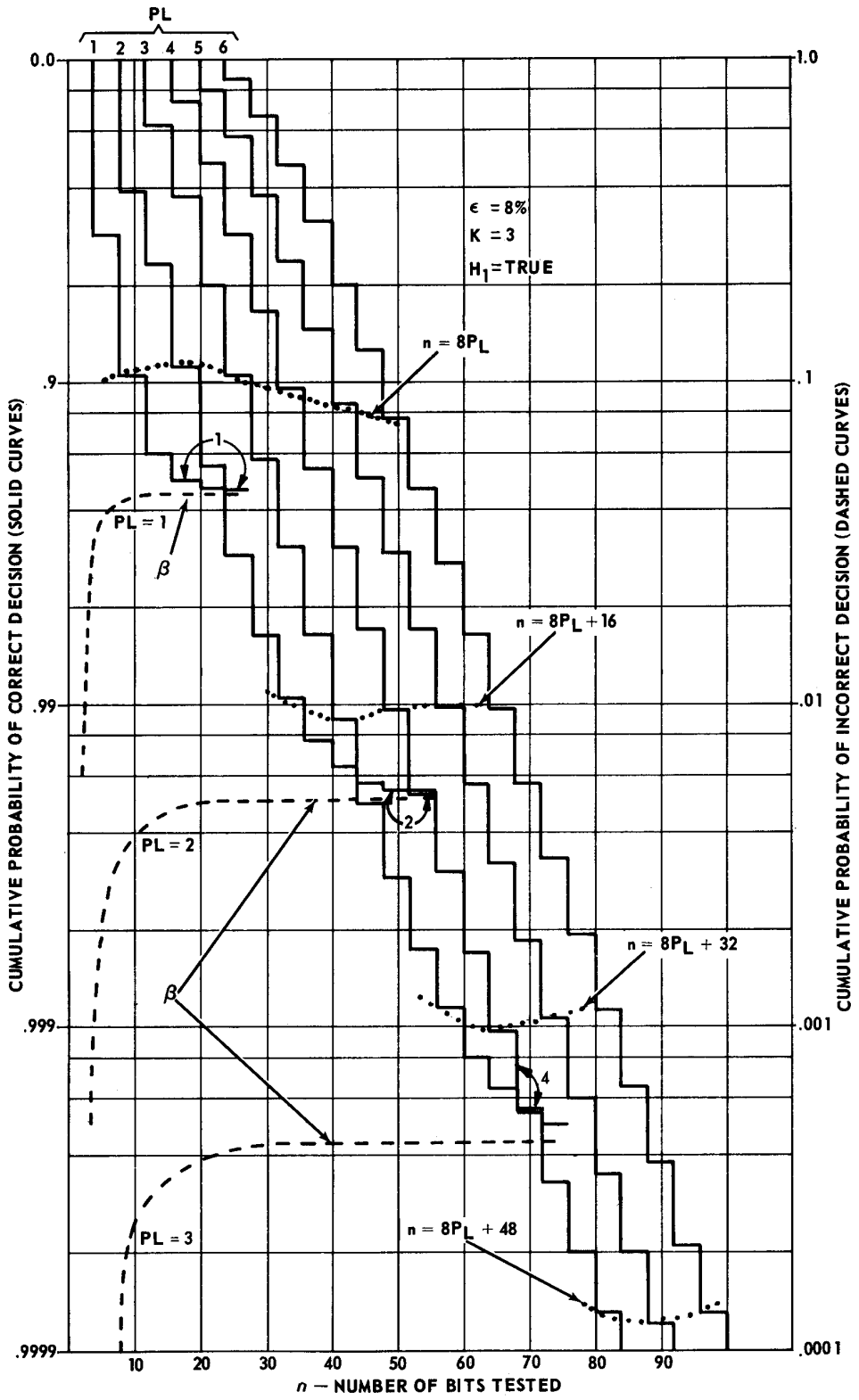

Fig. 8 - SPRT Decision Speed for Different Programmed Limits P_L