A TRANSMITTER CHIP SET FOR WIRELESS TELEMETRY APPLICATIONS

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ABSTRACT

M/A-COM, Inc. has developed a highly integrated transmitter chip set for wireless telemetry applications under a U.S. Army Development Contract. The chip set is comprised of a voltage controlled oscillator (VCO), a silicon synthesizer/phase locked loop (PLL), and a family of power amplifiers (PA's). The chip-set is designed to operate over the military L and S Band frequencies as well as the lower commercial ISM band. Using these components, M/A-COM has produced IRIG compliant transmitter modules for ballistic telemetry applications. These modules have been successfully flight tested by the Army Research Laboratory at Aberdeen Proving Ground, Maryland. This paper reviews the transmitter system architecture and presents test data for the transmitter module and individual components.

KEY WORDS

Transmitter, telemetry, munitions, high-g, voltage controlled oscillators

INTRODUCTION

In order to provide for the testing and evaluation of both standard and smart munitions, the U. S. Army's Hardened Subminiature Telemetry and Sensor System (HSTSS) program has developed a new generation of devices and subsystems for in-flight instrumentation. Gun launched systems experience high accelerations (high-g) during launch and are difficult to instrument. Rockets, although they experience less acceleration at launch, also have a severe environment due to vibration. Both are a challenge to instrument with today's commercial products due to volume constraints, system performance requirements, and budgetary issues.

Under the HSTSS program, M/A-COM has developed a very rugged, small, low cost, low power transmitter chip set for ballistic telemetry applications. This chip set architecture approach allows for embedded instrumentation solutions as well as retrofitting existing munitions with on-board measurement systems. Although some commercial transmitters exist for these types of applications, they typically are large in size, fixed in form factor, expensive, and limited in performance. In order to provide greater packaging and system design flexibility, a highly integrated transmitter chip set is required. The chip set is comprised of four major subsystems. They include a phase locked loop (PLL) chip, voltage controlled oscillator (VCO), a reference oscillator, and a family of power amplifiers (PA's). This paper reviews the transmitter architecture and design criteria for each subcomponent. In addition, the design of an integrated transmitter module with flight test data is discussed.

TRANSMITTER SYSTEM SPECIFICATIONS

The transmitter system design was driven from the contract specifications developed by a tri-service team of engineers. General specifications come from the IRIG 106-96 Telemetry Standards. A listing of these major parameters can be found in reference 1.

OPERATIONAL OVERVIEW

The transmitter chip set is comprised of a PLL, VCO, and a family of PA's. The PA's are available in 100 mW, 250 mW, 1W, and 2W ratings. A block diagram of the transmitter system is shown in figure 1. The VCO is the primary frequency source and is available in both L-Band and S-Band versions. The VCO can be used in two operational configurations, free running or phase locked. For free running operation the VCO is coupled directly with a PA. This type of inexpensive configuration can be used for extremely limited volume applications. In the free running mode, the 0.002% stability specification is not met until the system is allowed to warm up. This will be discussed further in the Module section of the paper.

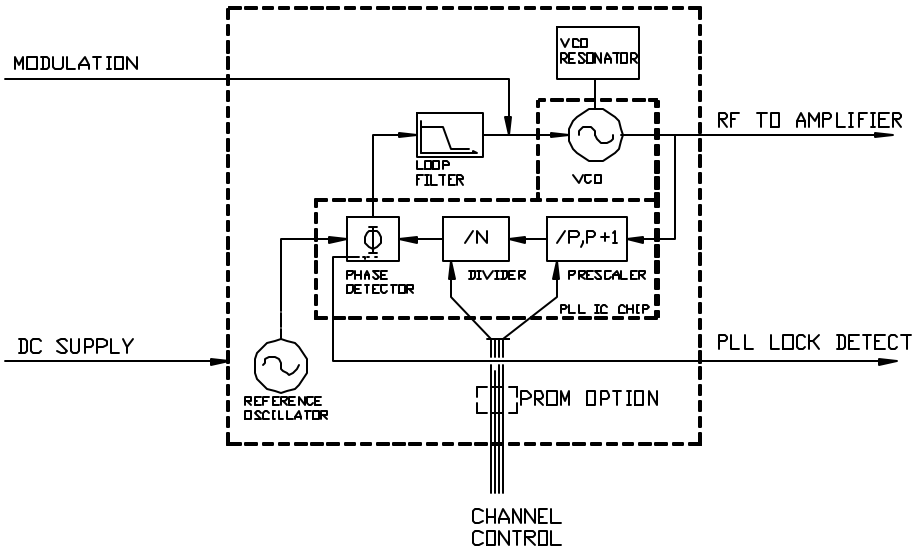

Figure 1. Frequency Source Block Diagram

The second configuration is the phase locked frequency source, with reference oscillator and phase locked VCO. For this configuration, the operator can program the carrier frequency using a four-wire bus. Programming can be accomplished by hardwiring the control lines or by using a micro-programmer. Sixteen steps are available in increments of 0.5 MHz steps in the L-band and the lower and upper S-bands. In this configuration the 0.002% stability requirement is easily met. To make the chip set even more versatile, the components are available in both die and surface mount packages. With this type of architecture the telemetry engineer can optimize the transmitter based on the system requirements.

MODULATOR/PLL

A block diagram of the PLL is shown in Figure 2. A "pulse swallowing architecture" is used to condition the RF signal for the phase/frequency detector. Both frequency band selection and channelization is parallel-programmed (Ref 2).

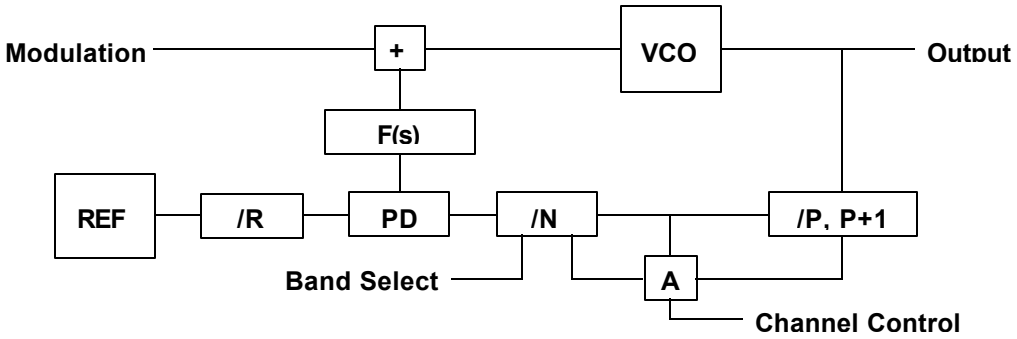

Figure 2. Topology for Phase Locked Loop Circuit.

PHASE DETECTOR/LOOP FILTER: The IRIG specifications require frequencies centered on 0.5 MHz. Thus the phase detector (PD) frequency is 500 kHz. The PD is a phase-frequency type detector, which allows for fast acquisition (high bandwidth) and narrow bandwidth tracking. The tracking bandwidth chosen is 1 kHz and the acquisition bandwidth is 10 kHz. Given these parameters and ~10 milliseconds relaxation time for the crystal reference oscillator, the overall system is expected to acquire lock in less than 20 milliseconds. The loop filter will use externally loadable components for maximum flexibility in integration.

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Dividers /Channelization: The topology in Figure 2 uses a dual modulus prescaler. By controlling both the A register and the N register, the three bands of operation and 16 required channels in each band can be synthesized. In order to accommodate the desired channels within the desired bands of operation, a "pulse swallowing" architecture was utilized to properly condition the RF signal for the Phase/Frequency Detector. With this architecture, the three major functional blocks (prescaler, swallow counter and divide-by-N divider) work together to produce a total divide ratio (M) as follows:

$$M = P*N+N$$

Where P = prescaler divide ratio
N = divide-by-n ratio
A = number of prescaler output periods the swallow counter "swallows" (i.e. the number of periods the output of the swallow counter remains "true" (HIGH)

Table 1 shows portions of the lower S-band channel scheme using 1 MHz spacing on 0.5 MHz channel centers. For applications not having external logic or controllers programming is accomplished by hard wiring the registers for a specific frequency.

Channel	PD Frequency (MHz)	P	N	N BINARY	A	A BINARY (Channel Select)	PLL Output Frequency (MHz)
1	0.5	32	140	10001100	1	00001	2240.5
2	0.5	32	140	10001100	3	00011	2241.5
3	0.5	32	140	10001100	5	00101	2242.5
4	0.5	32	140	10001100	7	00111	2243.5
…	…	…	…	…	…	…	…
14	0.5	32	140	10001100	27	11011	2253.5
15	0.5	32	140	10001100	29	11101	2254.5
16	0.5	32	140	10001100	31	11111	2255.5

Table 1. Channelization for Lower S- Band, 1 MHz Steps.

The PLL IC has been fabricated using a 0.35 um CMOS process. In addition to a 16-channel version a 32-channel version has also been design and fabricated. Additional features of the PLL include an on-chip op-amp and oscillator circuitry. The Op-amp allows for modulation injection (FM or FSK). The on-board oscillator works with either a 10MHz or 20 MHz external crystal resonator. This function can be bypassed if an external reference oscillator is desired. Both devices will be available in die and QSOP-28 SMT plastic package. The die size for each device is 2.3 mm x 1.9 mm.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

Two VCO chips, L-Band & S-Band, have been designed and fabricated using Indium Gallium Phosphide Heterojuction Bipolar Transistor (InGaP HBT) technology. InGaP HBT technology was chosen because it offers low phase noise, high linearity, thermal ruggedness, and single supply operation. The specifications that drive the VCO design are shown in Table 2. The device was designed with an on-chip varactor that can be bypassed by separating an air bridge on the die. Frequency is set using an off-chip resonator circuit. Loading options for varactor and resonator allow the VCO linearity and frequency to be finely tuned across L or S bands. Packaged devices include the resonator circuits which can be factory set based on customer applications. The VCO's are available in die and FQFP-N 4.0 mm plastic packages. The die size for each VCO is 1 mm square. A graph showing frequency vs. tuning voltage for lower S-band operation is shown in figure 3.

Specification	Unit	Value	Comment
Frequency Range	MHz	1435 – 1535 2200 – 2400	Tune with external resonator elements. Internal varactor may be bypassed.
Tuning Voltage	volts	0.5 - 3.0	
RF output power	dBm	10	Minimum
Supply Voltage	volts	3	Allow 20 % drop while operational
Operating temperature	degrees C	-40 to +85	

Table 2. Partial Table of VCO Specifications.

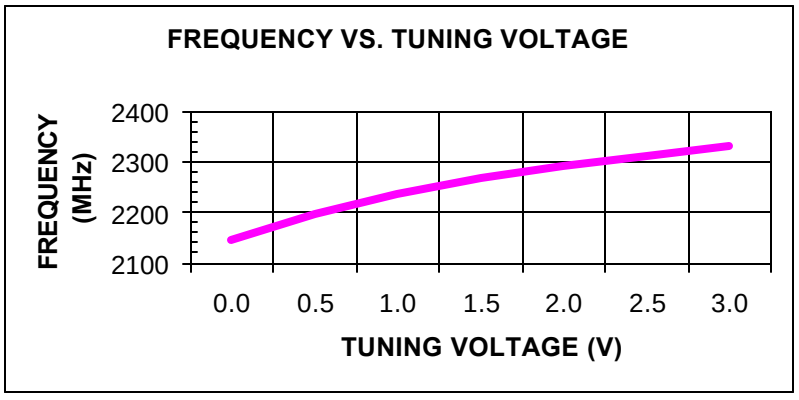

Figure 3. Frequency vs.Tuning Voltage for Lower S-band Operation

POWER AMPLIFIERS

A family of power amplifiers (PA's) has been developed to provide 100mW, 250mW, 1W and 2W nominal output power. By providing flexibility in the PA selection the user is able to optimize between power supply and link budget requirements.

100mW and 250 mW Low Power Amplifiers: Two separate chips for L and S band operation have been designed and fabricated for each nominal power level using InGaP HBT technology. Both devices are internally matched to 50 ohms at input and output (<2:1 VSWR). They are designed to use the 10mW output from the VCO as their input drive. By varying the bias conditions, the saturated output power of these devices may be tailored for various applications. The devices require minimal external components for bypassing, and are available in die and FQFP-N 4.0mm plastic packages. The die size for each device is 1.3 mm x 1.0 mm. Figure 4 shows lower S-band performance of power output (P_{OUT}) and current (I_{DD}) vs. power in (P_{IN}) for the 250mW devices.

1W/2W Power Amplifier: This device is a two-stage power amplifier constructed using a mature 0.5 um GaAs MESFET processes. Separate devices have been designed for L and S band operation. The chip employs a fully matched 50-Ohm input and output network and decoupled gate and drain bias networks. When operated at 5 volts the device provides 1-watt of output power and when operated at 8 volts provides 2-watts of output power. The efficiency is better than 30% in each mode of operation. The device is available in both die and a bolt down CR-15 ceramic package. The U.S. Army Research Lab has shown the packaged device to repeatedly survive 30,000 g shock loads.

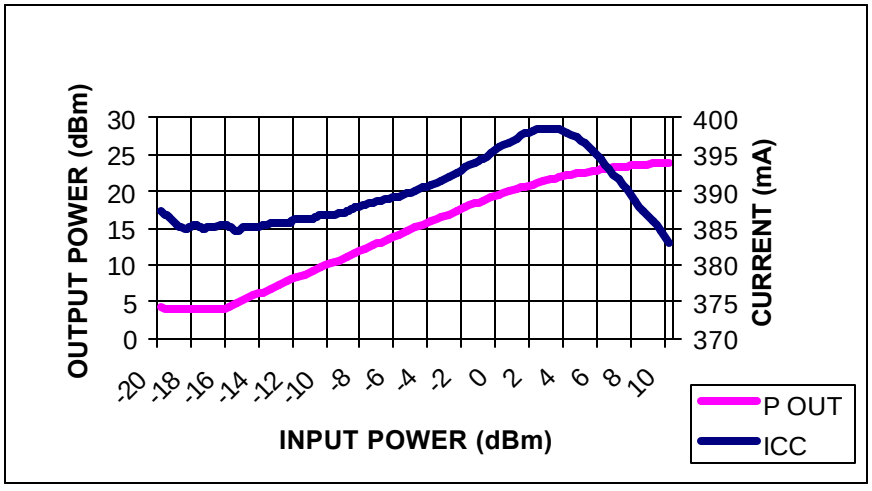

Figure 4. P_{OUT} & I_{DD} vs. P_{IN} for Lower S-Band 250mW PA devices.

QUARTZ REFERENCE OSCILLATOR

The task of meeting the IRIG 106-96 ±20 ppm frequency-stability over temperature requirement is the duty of the reference oscillator. However, providing small, reliable, and affordable quartz crystal reference oscillators for high-shock applications has been an on-going challenge. The Statek Corporation has developed both a quartz crystal resonator and a quartz crystal oscillator specifically for high-shock telemetry applications. These components provide frequency control for the HSTSS transmitter and clocking for the HSTSS data acquisition chip set.

The key to designing a resonator that can survive extremely high-shock levels is to make it small. This reduces its total mass so that it less likely to dismount and it reduces the stress within the crystal so that it is less susceptible to breakage. This size to ruggedness relationship is fortunate as miniaturization is one of the goals of the HSTSS program.

Statek's resonator design is an AT-strip quartz crystal resonator housed in a CX4HG package (0.197"L x 0.072"W x 0.045"H). Further, for additional ruggedness, the crystal is mounted to the ceramic package at both ends of the strip. This reduces the amount that the crystal can flex, and thereby further reduces the stress within the crystal. Being very small, these crystals have a motional capacitance of about 1.4 fF, a shunt capacitance of about 0.88 pF, and a resistance of about 35 to 120 ohms. Despite their small size, the crystal Q is in the range of 50,000 to 150,000.

Statek's high-shock oscillator (HGXO), which uses the high-shock quartz resonator, has a footprint of 5.0 mm x 7.5 mm and height of less than 2.5 mm. Operating at 3.0 V, it has a square-wave output, typically consumes less than 3 mA, and remains within 20 ppm of 20 MHz over the -40°C to +85°C temperature range. As required by the HSTSS program, this oscillator has survived shock testing to 100,000 G's.

TRANSMITTER MODULE

A transmitter module has been design to demonstrate the chip-set functionality. The form factor of the module was chosen to fit into a standard NATO artillery fuze housing. The module dimensions are 28.6 mm in diameter and 6.0 mm in height (with RF shield). The module can be configured to operate in either free running or phased locked mode for either the L or S band operation, and can be built with either the 100mW or 250mW PA. The module operating voltage is 2.85V – 3.15V. Data captured using a Modulation Domain analyzer at the Army Research Lab shows the transmitter system achieves 0.002% stability in less than 500 µs after initial power is applied. This is shown in figure 5.

The transmitter module is designed using both surface mount and chip & wire technology. The module is built on FR-4 substrate material and uses coplanar wave-guide for controlled impedance lines. At the time of this writing, over 100 modules have been delivered to the Army for ballistic telemetry applications. A picture of the module without the RF shield is shown in figure 6.

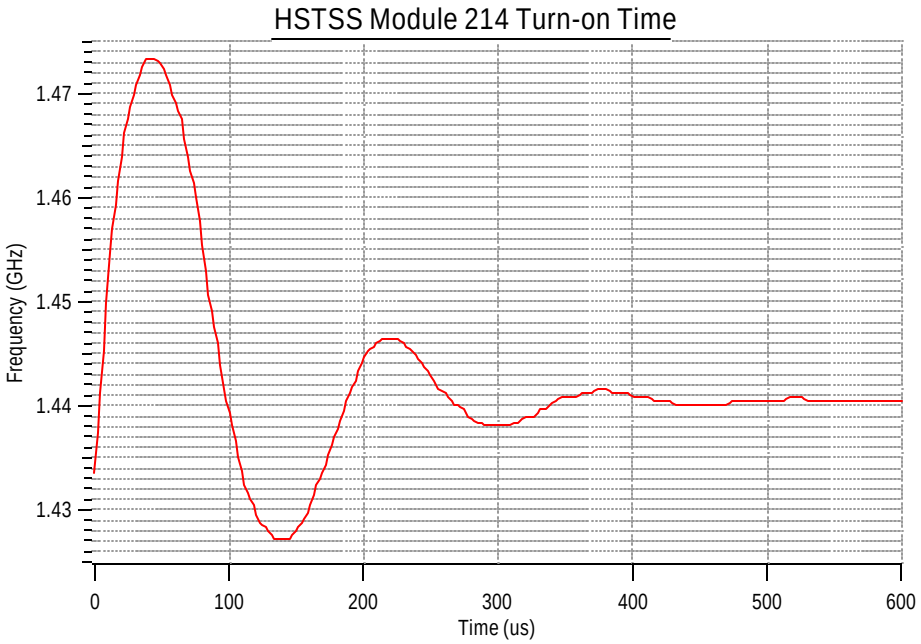

Figure 5. Turn-on time for Phase Locked L-Band Transmitter

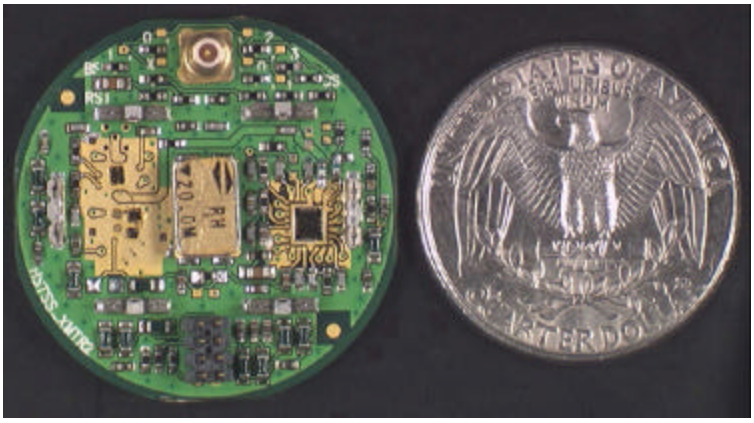

Figure 6. Photograph of transmitter module

APPLICATION TEST DATA

Under the HSTSS program, M/A-COM has worked directly with the Army Research Lab on qualifying the components and microelectronic assembly techniques for high-g environments. To date, nearly all of the components have been tested to 30,000 g or greater. In order to meet this requirement, both robust design practice and extensive reliability testing has been used (Ref 4,5, & 6)

In December of 2000, two protoptype phased locked L-Band transmitter modules were flight tested on 105-mm artillery projectiles. The transmitters were packaged in a standard NATO nose-fuze along with other HSTSS developed subsystems. The estimated setback acceleration was 16,000g. In-bore balloting was measured and showed peaks of around 1000 g with spikes reaching 2000 g. The spin rate for each round was in excess of 300 rps. The rounds were fired nearly straight up which resulted in the projectiles striking the ground base first, allowing recover of the rounds. In both cases the transmitter and accompanying subsystems not only survived the 16,000 g launch but also were still operational after impact. Setback and balloting accelerations measured from the on-board instrumentation system are shown in figures 7 and 8.

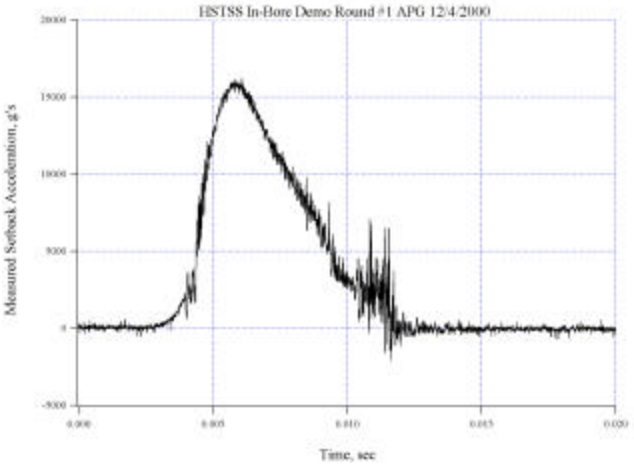

Figure 7. Setback Acceleration Data

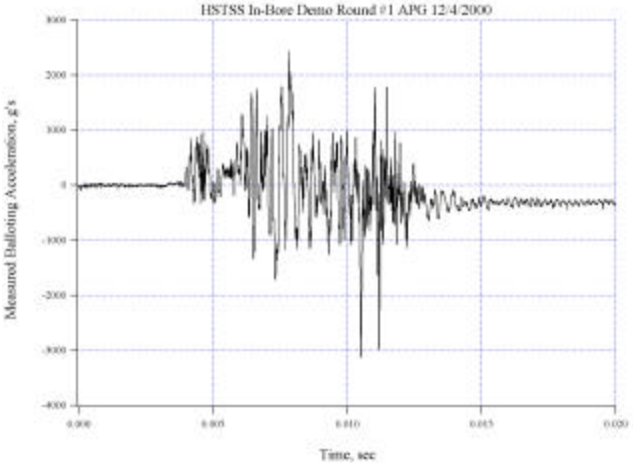

Figure 8. In-bore balloting data

SUMMARY

The M/A-COM transmitter chip set is providing the telemetry engineer with unprecedented design flexibility. It has a frequency response better than 10 MHz, programmable deviation sensitivity, in-band channel selectivity for both L and S bands, and a choice of power amplifiers. When used with a 20-ppm resonator the transmitter is IRIG 106-96 compatible. All integrated circuits for this chip set will be available in both die form and surface mount packages offering maximum system integration flexibility. The estimated die sizes and supply requirements for each component are summarized in Table 3.

	Size (mm)	Supply Voltage (Vdc)	Supply Current (mA)
VCO	1.0 x 1.0	3	30
PLL	3.3 x 1.9	3	25
100 mW	1.3 x 1.0	3	150
250 mW	1.0 x 1.5	3	350
2 W	3.0 x 2.5	8 (2W) & 5 (1W)	950

Table 3. Summary of Chip Sizes and Power Requirements.

In addition, new state of the art PA devices are being considered for 0.5 and 1.0 watt applications. M/A-COM's Indium Gallium Phosphide (InGaP) bipolar HBT technology and self-aligned MSAG MESFET technologies are both under evaluation for realizing these devices. These technologies will maximize performance while reducing component size and cost.

In this paper, the design and operation of a highly integrated, low cost transmitter chip-set was discussed. Details of the PLL, VCO, PA, and reference oscillator components were reviewed and a sample module assembly was discussed. This development effort represents a major advancement in the area of ballistic telemetry. The flexible architecture allows munition developers to integrate the instrumentation system with the on-board guidance, navigation and inertial measurement systems, thus providing an embedded instrumentation system. In addition to munitions testing the transmitter chip set is ideally suited for vehicle, airframe, and soldier training applications.

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