A PULSE-CODE-MODULATION (PCM) TELEMETRY SYSTEM UTILIZING MULTIPLE INTEGRATED CIRCUIT TECHNOLOGIES

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Summary This paper describes a Pulse-Code-Modulation (PCM) Telemetry System contained on a module that is unique in several ways:

1. Uses all Integrated Circuits (Ics).
2. Integrates many IC types and technologies for superior system physical, environmental, and performance characteristics.
3. Multiplexer section:

    a. Uses one type of IC (MCIS multifunction IC)
    b. Is bipolar (both positive and negative voltages can be multiplexed)
    c. Accepts low- or high-voltage inputs (±51.1 mv to ±5.11 v)
    d. Is extremely small and compact (5 ICs total, provides 48-channel multiplexing)
    e. Accepts both differential and single ended channels
    f. Is controlled by random or sequential addressing modes

4. Amplifier section:

    a. Has high input impedance (100 meg ohms)
    b. Has high common mode rejection (to 120 db)
    c. Has gain (1 or 100)
    d. Has sample and hold capability

5. Analog-to-Digital Converter (ADC) section:

    a. Is bipolar (both positive and negative voltages can be converted)
    b. Has high accuracy (10 bits)
    c. Uses current summation with successive approximation
    d. Has high speed (up to 1 MHz)

System Description This all-integrated circuit PCM Telemetry System accepts analog voltages of different ranges and polarity, multiplexes these voltages, amplifies and holds, and converts these voltages to digital values for transmission. Figure 1 shows a block diagram of the PCM Telemetry System. The system is capable of accepting 48 channels of information and providing 6 bits of address, if desirous, and 10 bits of magnitude information for transmission. The PCM Telemetry System utilizes many new integrated circuit technologies and types. Specifically, the following integrated circuits are utilized:

1. Metal Oxide Semiconductor (MOS)
2. Thin Film
3. Hybrid (thin film and semiconductor chips)
4. Polyisolated Compatible Linear Monolithic Semiconductor
5. Digital Monolithic Semiconductor

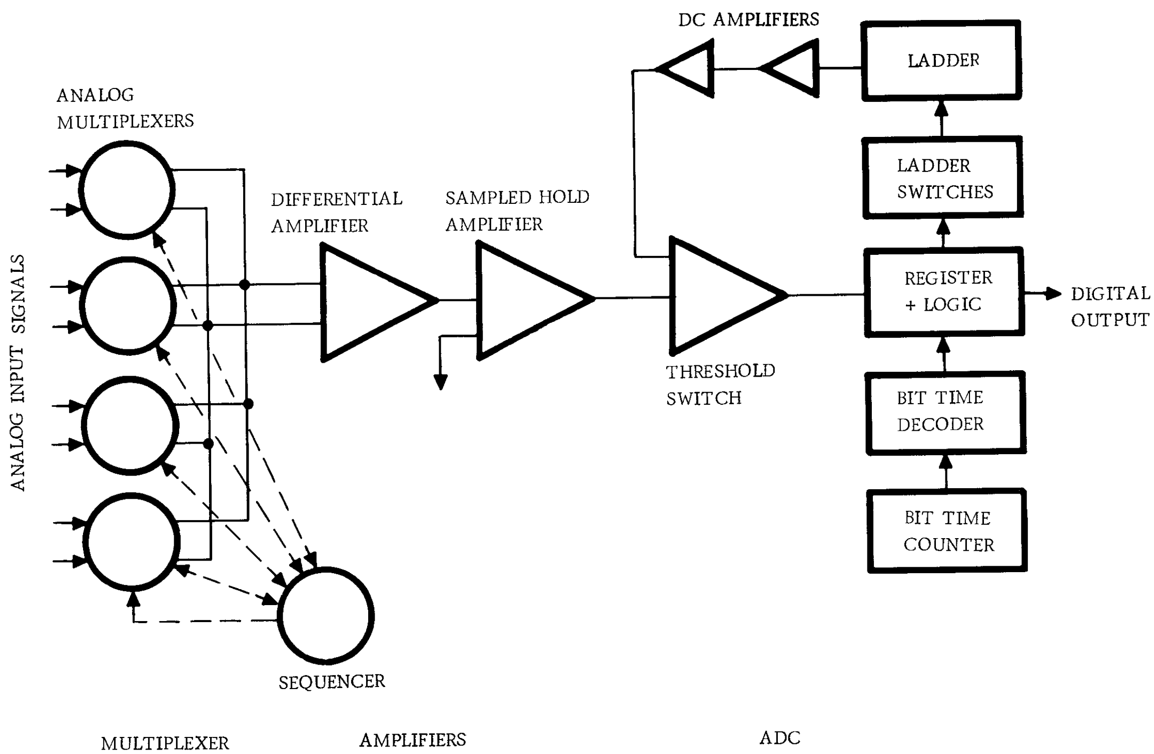

Figure 1. PCM Telemetry System Block Diagram

These technologies are interconnected to perform the PCM telemetry function. For convenience of description, the PCM Telemetry System is divided into three sections: Multiplexer, Amplifier, and ADC sections. These sections are mounted on one module (Figure 2). Each of these sections utilizes different technologies.

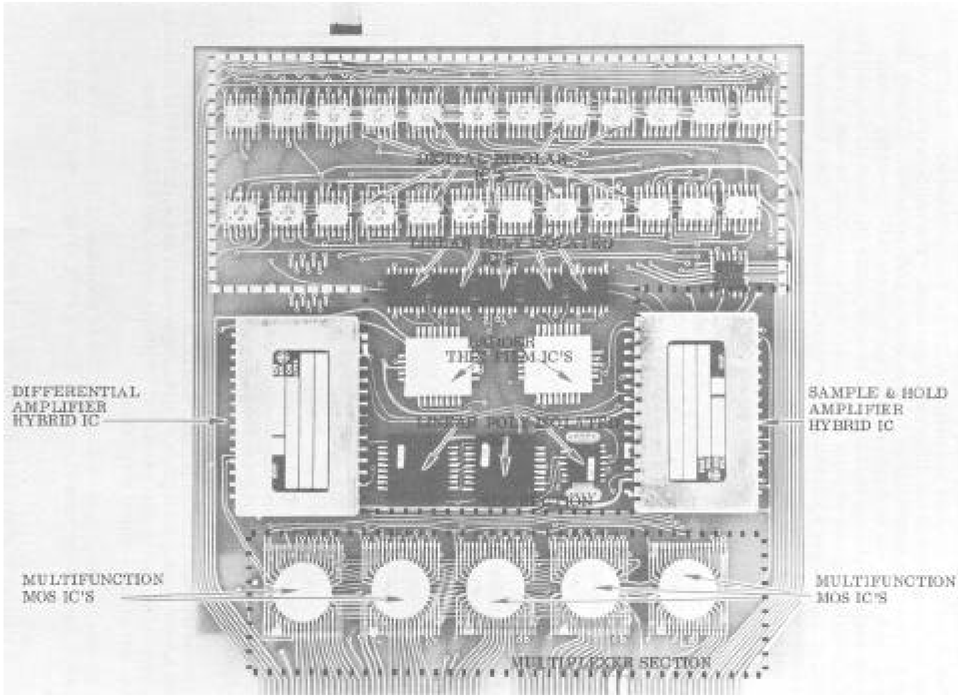

Figure 2. PCM Telemetry Module

Multiplexer Section The multiplexer section (see Figure 1) of the PCM Telemetry System multiplexes 32 single ended and 16 differential input channels. These channels can accept either a ±5.11 volts or ±51.1 millivolts full-range analog voltage. One level of multiplexing is used. The section consists of five identical MOS integrated circuits each containing 300 MOS transistors of various transconductances. Four ICs are wired to perform an analog multiplexer function; the 5th IC is used to provide sequencing or selection of the other four ICs. Two of the four circuits are programmed for single ended operation; the other two are programmed for differential operation. The multiplexer section operates in either the sequential or random access address modes. During the sequential mode, the end of digitization signal from the ADC provides a clock input to the analog switching MOS ICs. A counter within the MOS IC sequentially step the channels. An end-of-scan signal from the active MOS is sent to the 5th or sequencer MOS IC for addressing the next multiplexer IC. This sequence continues repeatedly through all channels and ICs. During the random access mode of operation, a digital address word controls the multiplexer channel selection. This word can address any channel in any order for any length of time.

The MOS Multifunction IC is exclusively used in the multiplexer. MOS is an excellent technology for low level, low offset, and micromin multiplexing. The MOS IC incorporates static logic in contrast to dynamic logic that is implemented in many new MOS ICs. Figure 3 is a block diagram of the MOS Multifunction IC. Figure 4 is a photo enlargement of the IC. This IC has a capability of multiplexing 16 single ended, or 8 differential analog signals. The IC can switch analog signals to the maximum full range

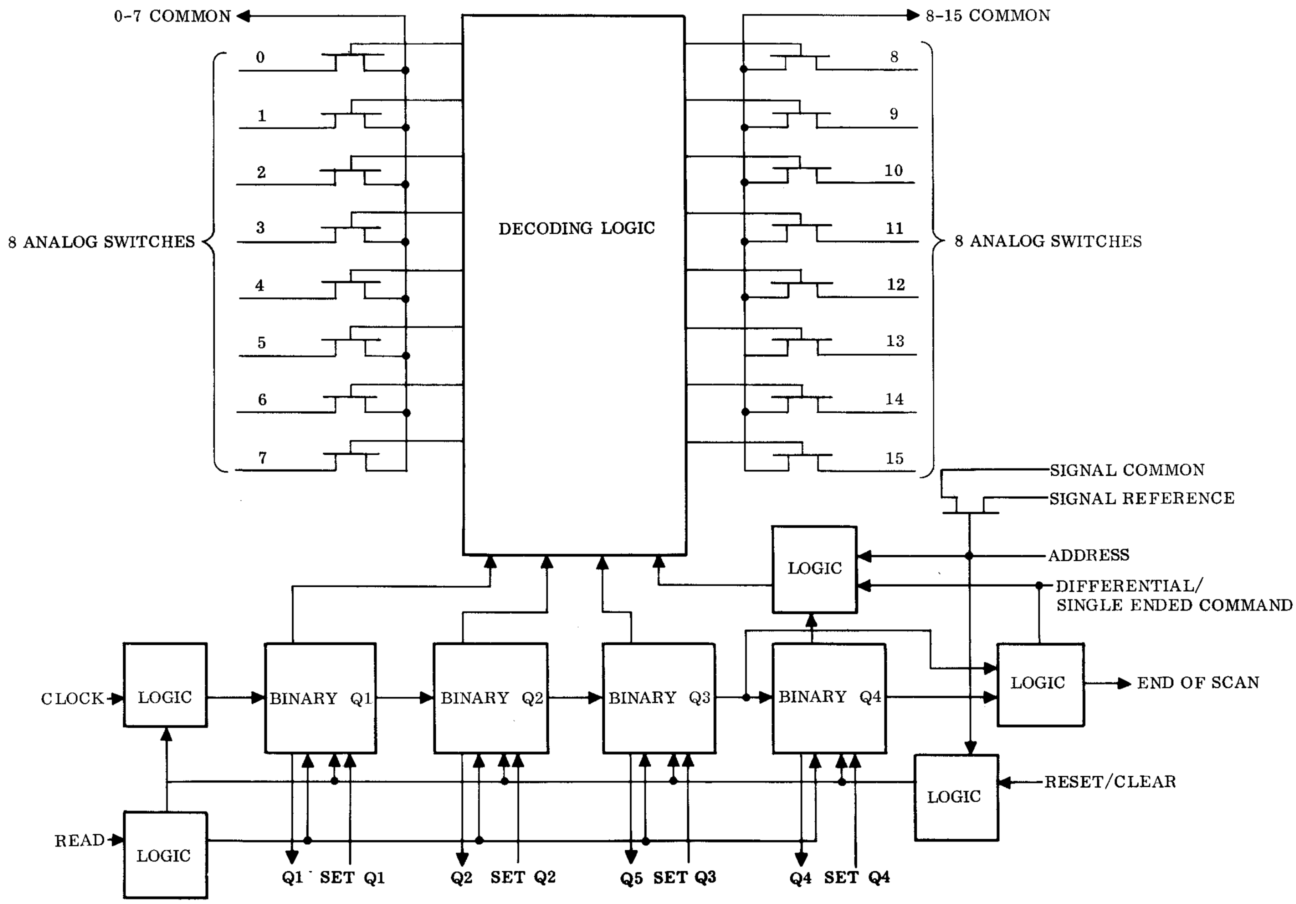

Figure 3. MOS Integrated Circuit Block Diagram

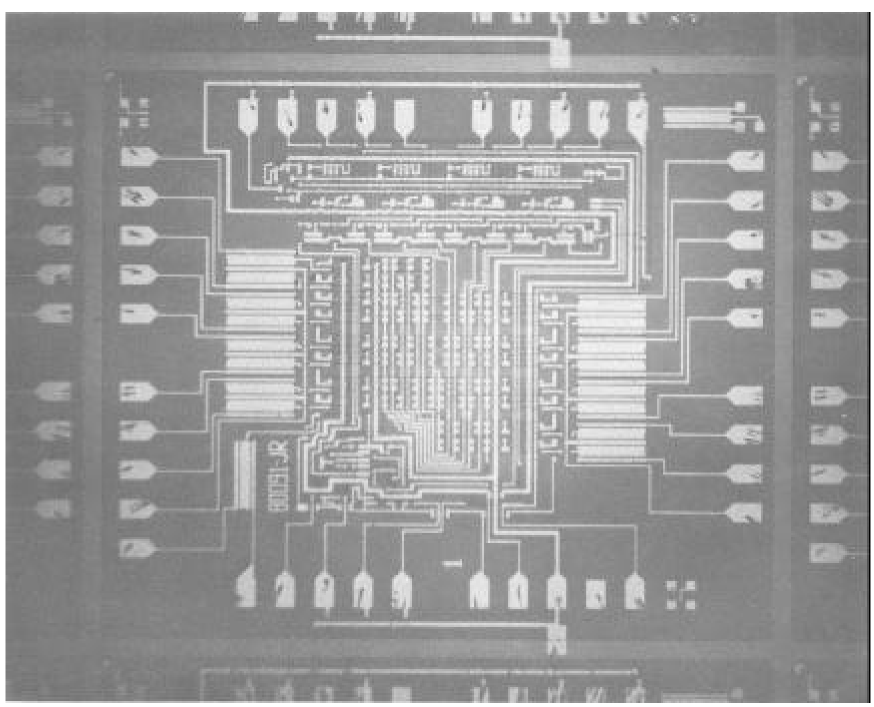

Figure 4. MOS Integrated Circuit Photograph (Highly Magnified)

of +10 volts (with substrate at greater than +10 volts dc) to -5 volts. These ICs are also able to switch accurately low level (microvolt) analog signals. The IC includes a 4-bit binary ripple counter and the necessary decoding logic to decode all 16 counter states. When the IC is addressed, each state activates one switch during the single-ended mode while two switches are simultaneously closed during the differential mode. The additional capability of randomly accessing any channel has been provided within the IC.

A 17th analog switch is provided as a reference for single ended operation. The binaries can be used as a module 16-binary ripple counter or as a copy register. The outputs of these binaries are also available. Provisions included in the MOS are: (1) an address command which must be in the true state for any switch to be operated, (2) an end of scan output, (3) a clear command input, (4) a read command input, and (5) a clock input. The MOS IC uses typically, -25 volts, -14 volts, and +7 volts. The power dissipation is less than 200 millwatts per IC. The analog switch has a typical “ON” resistance at +10 volts of 2 50 ohms, and an “ON” resistance of approximately 1.4K at -5 volts. The switches can operate up to at least 250 Kilohertz. However, the counter has been operated successfully above 1 Megahertz.

Within the Telemetry module, the MOS IC is used in three applications: (1) as a random access analog multiplexer of 16-single ended and 8-differential channels, (2) as a sequential analog commutator of 16-single ended and 8-differential channels, and (3) as a digital programmer.

One IC selects one of four multiplexer ICs in sequence or by random access. In addition to these three uses of the MOS IC in a PCM system, this IC can be used as:

1. A counter to count up to any number up to 16
2. A 4-bit binary decoder
3. An analog function generator
4. A parallel to serial converter of 16 bits
5. A 16-bit code generator
6. A 4-bit storage register
7. A universal logic building block

The analog function generator application has been demonstrated in the laboratory by applying different voltages on the various input lines. The smoothness of the function can be increased by the series addition of several of these MOS ICs. Two functions can be simultaneously generated by use of the differential command at a sacrifice of the resolution available from one IC.

The counter application has also been demonstrated in the laboratory. This application is performed by selecting the output of a particular switch and feeding it back to the clear input of the binary counter. Thus, when the switch output goes logically true the counter is cleared at the selected count.

This IC can be used as a universal logic building block since any minterm of the four storage elements may be mechanized. Thus, 2^{16} functions may be derived. These minterms are formed by connecting the MOS switch outputs external to the IC.

Amplifier Section The amplifier section consists of a differential amplifier and a sample of hold amplifier. These amplifiers are mechanized using hybrid integrated circuit technologies. The transistor, diode, and capacitor chips are mounted on an alumina substrate and ultrasonically bonded to gold interconnection leads. Deposited nichrome resistors are used. This technology was used for the amplifier section to achieve high performance. Other advantages of this technology are:

1. Low-cost prototype development
2. Short development schedule
3. Small size relative to discrete circuitry
4. High reliability through minimization of solder interconnections
5. Dynamic trim capability which eliminates potentiometers
6. Use of nichrome resistors for resistance ratio tracking and temperature coefficient tracking

The differential amplifier (Figure 5) is used for up to 120 db common mode noise rejection and amplification of 100 for low-level analog levels. In addition, the amplifier provides a 100 megohm input impedance. Open loop differential voltage gain is 25,000 and the common mode voltage range is +15 volts to -10 volts. The equivalent input offset voltage is 0.1 millivolt total, and the temperature coefficient is 5.0 microvolts per degree centigrade.

The sample and hold amplifier is similar in design to the differential amplifier and is used for operation at the design frequency of the PCM system to hold varying analog input signals during the digitization time. The sample period is 20 microseconds and the hold period is 44 microseconds. Both the differential amplifier and the sample hold amplifier uses a 3/4 X 1-1/2-inch die and are mounted in a 30 lead (with 100 mil spacing) 1 X 2-inch metal package.

Analog-To-Digital Converter Section A 10-bit current summation successive approximation Analog-To-Digital Converter (ADC) is used in the PCM System. The system accuracy using the ADC is within ±0.1%, ±1/2 least significant bit. The converter linear circuits utilizes the poly-isolated compatible monolithic semiconductor technology

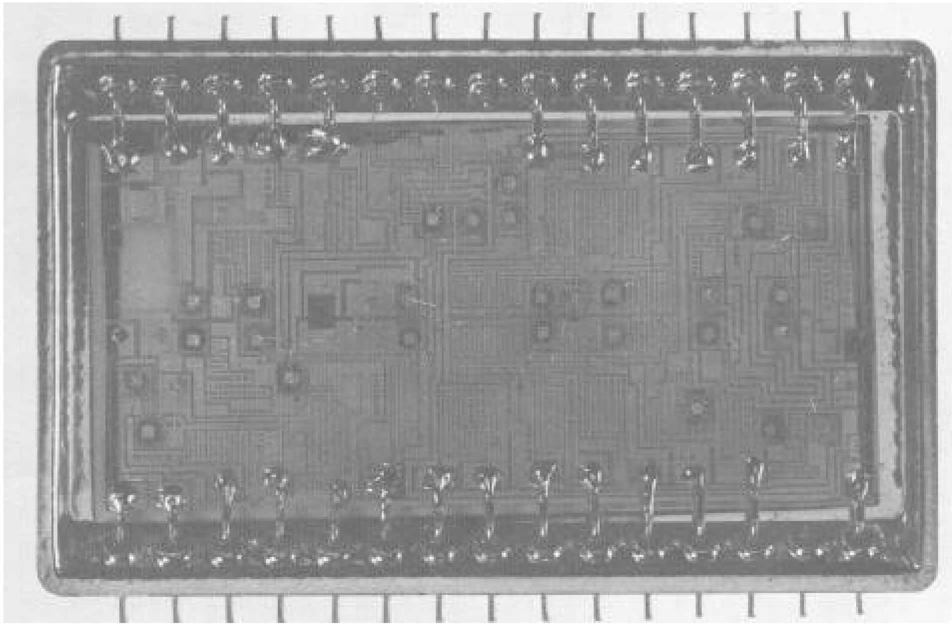

Figure 5. Differential Amplifier Photograph

to reduce parasitic capacitance and achieve high operating speeds. Two d-c amplifiers, one threshold switch, 5-ladder switch, and two thinfilm ladder ICs make up the analog portion of the converter. The digital portion of the converter is implemented using 24-digital transistor-transistor logic (TTL) ICs. These ICs are low cost, and readily available. The convertor uses one monostable multivibrator.

The ADC design is unique in two ways. First, the 10-bit ladder is divided into two identical 5-bit ladder thin-film ICs. Thin-film technology is used to obtain resistance ratio and temperature coefficient tracking during temperature changes. A resistance divider within the IC is used to divide down the reference voltage of the most significant 5 bits by 32 (the decimal magnitude of 5 bits). Using this as a reference, which is buffered, for the reference voltage onthe least significant 5 bits, results in a simpler and easier method to fabricate an IC ladder and provides better ADC performance. Since current summation ADCs use ladder legs that increase in resistance binarily from most to least significant bits, this design keeps the RC time constant sufficiently low to ensure an ADC of desired speed. The ADC has performed satisfactorily up to 1 Megahertz, but is operated in this PCM System at a 250 Kilohertz bit clock frequency.

The second unique design is the ladder current switching. The ladder legs are switched out of the current summation mode by a doubled shunting technique which reduces the offset voltage (or current) to a lower valve than that used in a single switch.

The d-c amplifier circuits are unique, containing a 60 X 75 mil silicon chip placed on an alumina chip containing the summing, feedback, and offset compensation thin-film resistors. MOS compatible capacitors on silicon wafer are used for frequency compensation.

The amplifiers have the following specifications:

Imput Power:	200 milliwatts
D-C Input Bias Current:	600 nanoamps
Input Differential Offset Voltage:	1 millivolt
Output Common Mode Voltage:	±1 volt
Maximum Output Signal Swing:	±7 volts
Open-Loop Difference Voltage Gain: = 15,000 volts per volt	
Frequency Cutoff:	1 Kilohertz
Common Mode Voltage Gain = 0. 5 volt per volt	
Common Mode Input Limits:	±5 volts
Power Supply Requirements:	E + = 14 volts, E - = -14 volts
Package:	18 lead 1/2" X 1/2" flat pack

The threshold switch IC uses a 60 X 52 mil silicon chip and has the following specifications:

Input Threshold Voltage:	±0. 5 millivolt
Propogation Delay Time:	40 nanoseconds
Input Common Mode Voltage Limits:	±5 volts
Output Voltage Levels:	Standard digital 0 to 3.5 volts
Input Power:	260 millivolts
Voltage Gain:	2000 volts per volt
Input D-C Offset Voltage:	±0. 5 millivolt
Package:	1/4" X 1/4" Flat Pack

The thin-film ladder IC uses a 270 X 320 mil nichrome deposited alumina chip. Resistive ratios are trimmed to ±0.02 percent. The temperature coefficient is +20 ppm per degree centigrade. A 26 lead 1/2" X 1/2" flat pack is used to house the chip. Included within the chip is the reference divider and two equal resistors as source and feedback (gain of 1) resistors for the first d-c amplifier.

Two ladder switches are included in each IC package. A 50 X 55 mil silicon chip is used. The ladder switch IC has the following specifications:

Input Power:	23.5 millivolts
Turn-on Propogation Delay:	30 nanoseconds
Turn-off Propogation Delay:	60 nanoseconds
Output Saturation Voltage:	2 millivolts

Output Leakage Current:	5 nanoamps
Package:	1/4: X 1/4" flat pack

Conclusion The telemetry system has been successful in showing the feasibility, practicality, and desirability of an all-integrated circuit PCM System consisting of both analog and digital circuitry. The PCM System can be operated by plugging it into an attache case containing controls and displays for demonstration (Figures 6 and 7). Although quantitative information is not available, the exclusive use of ICs should prove to be more reliable and less costly than existing systems.

After completion of any development project, there are many ideas on how the system may be improved. This project was no exception. An even smaller PCM System can be composed simply by slight redesigns in the logic. The MOS Multifunction IC could be used to eliminate 12 digital ICs associated with the bit counter and decoding gates. The elimination of one d-c amplifier is feasible. Other designs requiring new MOS ICs are centered about using 2 or 3 ICs only for the complete ADC.

Figure 6. PCM Telemetry Demonstrator

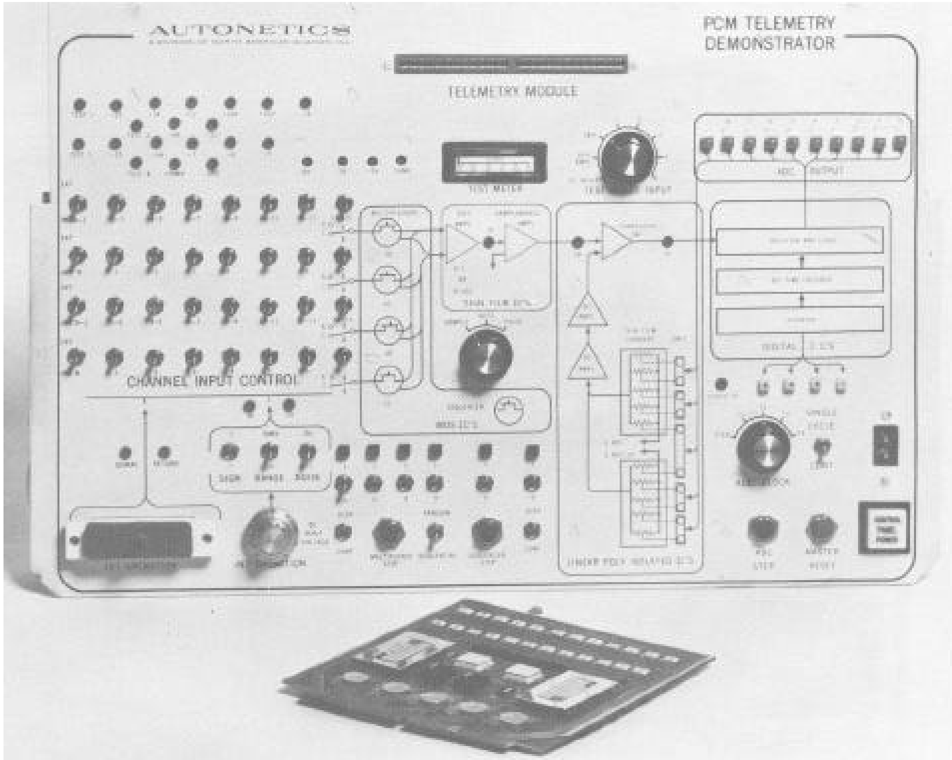

Figure 7. PCM Telemetry Demonstrator Control Panel