A FAMILY OF LINEAR INTEGRATED CIRCUITS FOR TELEMETRY

M. B. RUDIN and R. L. O'DAY
Fairchild Semiconductor
Palo Alto, California

Summary Advances in monolithic circuit and process techniques are making available a steadily increasing number of linear integrated circuits especially applicable to telemetry systems. This paper reviews the principal types of telemetry systems--PCM, PAM, PDM, and FM/FM. It demonstrates that a compatible family of monolithic IC's in various stages of development at Fairchild can perform most of the circuit functions required by these systems--namely: (1) signal conditioning amplifiers, (2) multiplexer, (3) sample and hold, (4) unity gain A/D buffer amplifier, (5) A/D and PDM comparator, (6) D/A reference and switches, (7) D/A summing amplifier. In addition, future integration of functions not performed by the above circuits is discussed.

Introduction The coarse performance parameter tolerances of early integrated circuits precluded their effective use for linear functions, especially in telemetry systems where signal fidelity is paramount. In recent years, linear integrated circuits (LIC's) suitable for uses in many systems have co-me on the market, but they have not in general been fully satisfactory for many telemetry applications. However, this has not been because of an inherent limitation of IC's. New producible LIC technologies and compatible circuit techniques have been needed to capitalize on the built-in matching of IC elements, and to solve or circumvent the well-known IC limitations with respect to variety of compatible elements.

It is the purpose of this paper to introduce and describe a family of LIC's under various stages of development at Fairchild which are expected to finally overcome the significant obstacles to the use of IC's in the more voluminous applications in telemetry systems, and to indicate the directions which future developments are likely to take in attempting to satisfy the needs of the telemetry industry. The advanced performance of these circuits is the result of new semiconductor and thin film technologies in conjunction with circuit techniques tailored to the peculiarities of these technologies.

This paper is organized as follows:

1. Telemetry Requirements on Circuits.
2. The New Family of Monolithic IC's for Telemetry.
3. Future LIC's for Telemetry.
4. Conclusion.

Telemetry Requirements on Circuits It is a common fact that the principal baseband signal multiplexing techniques used in telemetry today are, in descending order of popularity: PCM, FM subcarriers, PAM, and PDM, with PCM becoming more dominant with each passing year. From the standpoint of the semiconductor IC manufacturer seeking those linear or hybrid functions presenting the largest potential market, the above four system configurations were dissected into blocks potentially suitable for monolithic integration. The result is shown in Figure 1–1(a) the remote data acquisition multiplexing and transmitting system, 1(b) the receiving, demultiplexing, recording, and display system.

Figure 1 clearly illustrates two important conclusions on which functions are most attractive for monolithic integration from the standpoint of volume usage. First, it illustrates the varying degrees of commonality between the multiplexing schemes. The inputs and outputs have completely common functions--i.e., signal conditioners and displays. A time division multiplexer and demultiplexer is common to the three time division systems. A precision comparator is needed for both P CM and PDM encoders. Second, those functions closer to the input and outout are more numerous because they are not multiplexed.

Other important considerations, from the, standpoint of the IC manufacturer, are (1) the greater number of systems and the higher value of miniaturization and maintenance-free reliability normally associated with the remote acquisition system, and (2) the greater difficulty and expense in building higher frequency and/or higher power IC's.

For the foregoing reasons, the signal conditioners are inherently the premium targets for integration, the multiplexer and VCO's are next, and the PCM and FM/FM decoding blocks (D/A and FM discriminators) are close behind. Other linear Functions are not initially as interesting for integration, with one possible exception. This is the precision encoder comparator, which -may be used as (1) a multiplexer gate in an interesting new form of PCM or PDM system 1/ , or (2) in a local encoder serving individual transducers or small channel groups. Both of these applications are part of a new system trend toward increased paralleling of lower cost miniature hardware in exchange for reduced cabling and better reliability.

The primary requirements for each of the blocks identified by asterisk (*) in Figure 1--i.e., those functions targeted for LIC development--were estimated. These requirements are tabulated in Figures 2-5; the basis for them is discussed in the following paragraphs.

Signal Conditioning

Signal conditioning has been divided into the “Preamplifier” or front end section emphasizing total input offset and noise minimization, and the signal processing section emphasizing frequency and amplitude transformations. The requirements for these blocks can range as broadly as the vast variety of transducers whose outputs may feed the signal conditioner. This would seem to demand a variety of circuits; but the desires of both the LIC manufacturer and the user to standardize for production and logistics reasons makes the operational amplifier a logical choice for the basic active element building block for signal conditioners. With this approach the different functions can be realized by use of various feedback networks, and just two amplifiers at most need be considered by the semiconductor LIC manufacturer: (1) a low level front end op amp, (2) a simpler, high level signal processing amplifier. For the above reasons, the circuit requirements of signal conditioning in Figure 2 have been written in the format of op amp (operational amplifier)specifications.

It may be noted that the preamplifier has a great number of critical parameters because it interfaces with the external world--the transducers and input lines--and therefore must be prepared to handle a range of signal levels, bandwidths and, most important, large spurious common mode voltages. The values given in Figure 2 were estimated on the basis of the following assumptions: (1) permissible system error contributed by each block--±.05% FS for 5 v signals and ±.3% for 5 mv signals; (2) input voltage range--± 5 mv FS to ± 5 v FS; (3) input source resistance- - 5 kΩ maximum; (4) common mode voltage range permitting satisfactory operation--± 10 v; (5) maximum common mode range (permitting circuit survival)--± 20 v; (6) maximum bandwidth based on 2 kc maximum transient or vibration signals; (7) load impedance–1 MΩ minimum; (8) power–1 watt maximum for 100 preamps. It should be noted that the gain accuracy can be ±50% if its nominal value is 10^6 --i.e., gain stability is a function of the loop gain, decreasing inversely with the latter. Also, for brevity V and I offsets are given as totals, including initial offset, noise, and thermal drift.

The use of an op amp for low level instrumentation signals presents one unorthodox problem--difficulty of getting high input impedance with differential inputs. This is because of gain control feedback current. For single ended input, this problem can be avoided by use of a noninverting input and feedback to the inverting input. However, this sacrifices the common mode pickup bucking properties of the differential input. One answer is that many of the low level sources, e.g., thermocouples and photodiodes, do

not require high impedance input. Thus the requirements on input impedance in Figure 2 have been split into three cases, the first two of which can be satisfied by a low level op amp: (1) low level grounded input, (2) low level differential input from low (< 100Ω) source resistance, and (3) low level differential input from high source resistance.

Another circuit function, common to signal conditioners, is low power transducer supply regulators and references. It can be shown that general purpose op amps in the Fairchild μA709 class are very useful as current sources and DC voltage transformers using a zener or external voltage reference. This usage is not sufficiently standardized to specify for present purposes.

The processor requirement is relatively uncritical, since it handles full scale signal levels. This permits relaxation of the specs for offset, input impedance, gain, and common mode rejection ratio.

Multiplexing

Multiplexing has been divided into (1) time-division (TD) gates or switches for the TD systems, (2) VCO's for frequency division*, (3) TD common high level buffer amplifier, (4) TD common low level booster/buffer amplifier. Although Figure I shows a single common amplifier, these amplifiers are important because actual systems often employ as many as (N/8) amplifiers (where N is total channels) for buffering purposes.

Digital control is similar for all time division systems; therefore, it is important only in setting interface logic levels. Because MOS-FET's are good analog switches, and permit good logic packing densities, their logic levels--typically of the order 0 and -10 volts--tend to be preferable for the analog multiplexer. But the additional power supply levels they entail may be a system drawback. This problem and possible solutions are discussed later in the section on the Fairchild developmental 16 channel differential multiplexer.

Four principal parameters for the multiplexer are given in Figure 3. The assumptions leading to the values given are: (1) permissible Ron errors, ±.1% PAM, ±.025% PDM and PCM; (2) maximum system sampling rate, 100K samples/sec PAM, 1K samples/sec PDM, 50 to 100K samples/sec PCM; (3) permissible $I_{leakage}$ error, ±.02% high level, ±.5% low level; (4) common mode range the same as that for the signal conditioner preamp--±10 v--due to lead pickup (this assumes no buffer at the multiplexer input); (5) one layer of submultiplexer cascading to achieve capacitive and leakage isolation. The permissible accuracies are based on the higher overall accuracies achievable with PCM and PDM, over PAM--typically ±.1%, .5%, and 1.0% respectively.

---

* The popular, proportional FM/FM or the later constant bandwidth FM subcarriers are assumed. AM subcarriers not considered of sufficient interest.

The common high level buffer requirements are self evident, with the possible exception of the bandwidth, which should be about six times the sample rate for acceptable pulse-tail crosstalk. The common low level buffer requires input characteristics similar to the signal conditioner preamp, coupled with a wider bandwidth to accommodate the multiplexer sample rate. This demands much more power. About 150 to 300 mw was estimated, depending on the amplifier design.

The VCO requirements have been included (Figure 4) just for completeness, since they have a number of peculiar characteristics which militate against a high degree of standardized monolithic integration within the present state of low cost production technology. Sonle of these are: (1) frequency stability implying very stable RC products versus temperature in frequency determining networks; (2) linear frequency deviation over 7.5%, implying 0.5% linear variation of RC products within this tolerance; (3) a wide variety of center frequency and bandwidth. All of these features may be obtained by the use of IC op amps as the active elements in conjunction with passive selective feedback networks, and at most one voltage variable element. However, no translation of VCO requirements into op amp specifications has been attempted as yet.

Encoding and Decoding

The major linear circuit blocks within the encoding and decoding categories are: (1) D/A for PCM, (2) precision comparator for PCM and PDM, (3) sample-and-hold for PCM and PDM, (4) summing (buffer) amplifier for display D/A, and (5) the FM discriminators for FM/FM.

The salient parameters for the Digital-to-Analog Converter are speed, accuracy, logic level in, and analog level out. The vehicle-borne encoders commonly require speeds approaching 500 kbits/sec, and new systems may go higher. The local A/D's and the display readouts usually need much lower speeds--typically 2 kbits/sec to 20 kbits/sec. Overall PCM system accuracy of 8 to 10 bits ± 1/2 bit maximum, governed the D/A requirement. Logic level depends on whether MOS or bipolar digital circuits are used. Bipolar was assumed because it can more easily handle 1 Mbit/ sec. The more important requirements on the D/A buffer are the input offsets and the output current. These were specified in Figure 5 on the assumption that 8 bits ± 1/2 bit is sufficient accuracy for compatibility with most display subsystems and devices.

For the Precision Comparator, speed permitting A/D conversion at 1 μsec per bit, coupled with input offset low enough to permit encoding to .05% accuracy, are the basis for the PCM requirements of Figure 5. The PDM accuracy requirements depend on both the switching speed and the threshold accuracy; however, assuming .1% error from each source, and 1 msec FS for PDM, the PCM comparator is able to do the PDM encoder comparisons also.

For data frequencies over about 20 Hz, a Sample-and-Hold is needed in a 10 bit (1 Mbit/sec) PCM system 2/. The sampling aperture, or charging cycle of the sample-and-hold, was assumed to be 1 μsec, and the switching time uncertainty, 100 nsec, giving a time constant of less than .15 μsec. This determines the required output current of the sampleand-hold input amplifier, assuming a 200 pf storage capacitor, to be about 10 ma. The output amplifier requires an input impedance for these assumptions of 100 MΩ, and offset stability of ±2.5 mv, with both input and output amplifiers having unity gains precise to ±.05% (or their gain products).

The sample-and-hold for PAM and PDM display driving can use larger storage capacitors with the same in-out amplifiers as for the PCM encoder, because their accuracies are lower, and they have greater available charging time. However, their output current may require an additional buffer.

The input requirements on the D/A Summing Amplifier are similar to those for the processing amplifier in the signal conditioner. Its output requires greater current capacity to drive some displays without additional buffering.

FM Discriminators have standard FM/FM proportional and constant bandwidth specs, and can potentially use building blocks similar to those hypothesized for the subcarrier VCO's, i e., a nonlinear VCO phase-locked by a frequency discriminator composed of op amps and RC's. Thus far we have not attempted to postulate individual amplifier and VCO specs for such a scheme.

The New Family of Monolithic IC's for Telemetry Monolithic linear integrated circuits have been improving rapidly during the past two years, but still have required significant performance compromises which have prohibited their use in a number of important applications. Recent advances in MOS and bipolar semiconductor and thin film technologies in conjunction with new circuit techniques have reduced or eliminated several of the important deficiencies restricting LIC designers in the past, namely: (a) noise, (b) low gain transistors (with low input impedances), (c) low resistance values, (d) leaky capacitors. The new technologies are permitting development of a family of new circuits applicable to telemetry systems:

(1) Micropower High Impedance, Low Noise Operational Amplifier,
(2) Low Drift, High Impedance, Low Noise Instrumentation Operational Amplifier,
(3) Low Noise, High Impedance, High Slew Rate Operational Amplifier,
(4) Junction FET Input Operational Amplifier,
(5) 16 Channel Differential Multiplexer,
(6) 10 Bit D/A Reference and Current Switches,
(7) Precision Comparator.

Performance and design considerations on several of these circuits are being reported separately at ITC/USA '67[**]. It is our intention here to summarize the applicability of these various LIC's to the telemetry requirements described and tabulated in the preceding section.

Micropower Operational Amplifier

This amplifier is truly micropower, yet it compares with conventional instrumentation amplifiers. Its outstanding characteristics are: (1) 0.1 mw total power drain unloaded (max); (2) input impedance typically 5 MΩ, (3) over 100 db common mode rejection, (4) over 10 kHz bandwidth, (5) less than 10 μv noise. Additional information is given in Reference 3.

Comparing its performance with the signal conditioner amplifier requirements, it may be seen that it will certainly serve the signal filtering and processing function. Also, its CMR is close to the preamp requirement of 120 db CMR, and it has low noise. Because it uses adjustable thin film resistors, a later version will be adjusted to less than 0. I mv input offset.

In systems where large numbers of preamps are desirable, and power is at a premium, the front end performance of this amplifier should be acceptable with external resistance balancing of offset when necessary. One hundred of these amplifiers will take just 10 mw to 50 mw of power, depending on output drive requirements!

Instrumentation Operational Amplifier

This amplifier was designed expressly for low level instrumentation. However, the main performance advantage it has over the Micropower Amplifier is bandwidth and slewing rate, which permit it to perform the common multiplexer amplifier function (see Figure 1) in addition to the signal conditioner functions. With its offset adjusted to zero by an external resistor, it has drift performance of 1 μv/°C--close to that of chopper amplifiers. An additional and very important advantage of this amplifier is economic: it achieves high input impedance and low input bias and offset currents by virtue of using a new high beta, low noise, all diffused (high yield) process. Minimum beta of its NPN transistors is 500! A summary of its outstanding characteristics, which compare favorably in many respects with the best discrete component amplifiers, follows: (1) Input Offset Current, 10 na; (2) Input Impedance, 1 MΩ; (3) Common Mode Range with ±15 v supply, ±13 v; (4) Input Current Noise, .1 to .2 pa per root Hz; (5) Slewing Rate with Gain ≥ 100, 20 v/μsec; (6) Short Circuit Protection of both input and output; (7) Common Mode Rejection, 120 db; (8) Wideband Noise, 8 nv per root Hz.

[**] See References 3 through 7.

As a post-multiplexer common buffer amplifier, it can handle PAM pulse rates up to about 150 to 300K samples/sec, as its open loop unity gain crossover is 9 MHz. A more detailed description of the amplifier is given in Reference 4.

High Slew Rate Amplifier

For applications where high slew rate is more important than maximum CMR, a second amplifier is in development. It will slew at 20 v/μsec with unity gain, thus qualifying as the input member of a telemetry Sample-and-Hold. Its significant differences with the Instrumentation Amplifier are:

(1) Higher slewing rate and higher unity gain bandwidth,
(2) Input offset current null, as well as input offset voltage null, by means of external potentiometer.

In most other respects the amplifier characteristics are similar to those of the μA709. Noise, drift, and other input characteristics are not presently as good as the instrumentation amplifier.

Hi Z_{in} Operational Amplifier

The combination of a junction FET (J-FET) input with bipolar transistor following stages is necessary to combine very high input impedance with good output drive characteristics required by (1) the Sample-and-Hold output buffer, (2) some high impedance transducers, and (3) monolithic thin film (low C's) signal conditioning filters. However, such an amplifier has two major design problems: (1) J-FET's are generally more difficult to drift-stabilize, and (2) a monolithic process for simultaneously constructing high performance J-FET's and NPN's is difficult and expensive with present state-of-the-art. Studies and developments are in progress at Fairchild to solve these two problems, but at time of writing no data can be given. It is hoped that some comments on feasibility can be given at the time of presentation.

To satisfy the system requirements for the sample-and-hold, the Hi Z_{in} Amplifier will require 100 MΩ input impedance, .1 na leakage, less than 5 mv offset drift over full temperature range, and 20 to 30 v/μsec unity gain slewing rate. Similar offset requirements are posed by the signal conditioning preamp. The Hi Z_{in} Amplifier should be ideal for AC filtering, where DC stability is not required.

16 Channel Differential Multiplexer

This is the largest single-chip MOS multiplexer reported to date (110 x 110 mils). It has 16 pairs of DPDT switches, which are activated by a random access decoding matrix of MOS transistors on the chip, minimizing external connections. In addition, it incorporates some protection against spurious channel overvoltages. Its switching speed is just fast enough to meet the 50 to 100K samples/ sec requirement of Figure 3. It was designed primarily for high level signals, but can handle low level channels whose source impedances do not exceed 50 ohms. It is bilateral, and is, therefore, equally useful as a demultiplexer for PAM or PDM, or as a function generator. Its important characteristics are as follows(1) R_{on}, 400 ohms @ +5 v channel voltage to 1000 ohms @ -5 v channel voltage; (2) R_{on} channel-channel variation (ΔR_{on}), 5 to 15 ohms; (3) switching speed < 10 μsec; supply voltages, +10, -20, -35 (zero power). More detailed information on its characteristics is given in Reference 5.

The two most important characteristics, from the standpoint of system compatibility, are the variation of R_{on} with channel voltage, and the use of logic and supply voltages differing from those of most bipolar IC's. The R_{on} variation is not a problem if a high Z_{in} common amplifier is used, and its effect is reduced greatly if the signal range is restricted to 0 to +5 v. Unfortunately, this effect on Ron of channel voltage places a substantial limitation on common mode range. It is of the order ±2.5 v, depending on supply and logic tolerances and system error budget.

The question of logic and power supply compatibility hinges on whether bipolar or MOS logic is used for the system. Normally MOS logic is fast enough for telemetry. However, even with MOS logic in the system, the high negative voltages used in a P-channel multiplexer in order to achieve low switch resistance (R_{on}) and compact MOS-FET pullup resistors generally will require special supplies. In this respect it should be noted that many of the linear integrated circuit amplifiers are capable of operating with unbalanced supplies, so zener dropping diodes may be used to drive the LIC's from a +10 v, -20 v supply. The -35 v supply is for logic resistor gate bias and requires practically zero power and minimal filtering.

10 Bit D/A

This circuit is the furthest advanced of the new family, and offers a simple, economical approach to D/A and A/D design over typical remote telemetry temperature ranges. In conjunction with external, weighting resistors and existing IC summing amplifiers (D/A) or the High Slew Rate Amplifier (A/D), it is capable of completely meeting the system requirements outlined in Figure 5, over a 100°C temperature range, and will operate over the full -55°C to 125°C military range. The process by which it is built is compatible with the addition of a thin film resistor process, and weighting resistors will be added

when economics permit. An important advantage which this circuit enjoys, even while operating at 1 Mbit, is its practically complete freedom from external transients and pickup, because of the use of a built-in reference current mode switching and current summing. Also, because of its small size and low thermal coefficient of error, it can be used to encode to as high as 13 to 15 bits by placing it in a small circuit board oven.

The most important characteristics of this circuit are: (1) it contains a reference and ten current sources which can be weighted binarily or as desired by precision external resistors; (2) once set at $T_{nominal}$, the sources plus reference track within the initial setting to . 2% over 100°C; (3) switching speed < 1 μsec; (4) it can be driven by all common IC logic levels, except MOS. For the latter, a ± inverter is necessary, and such P-channel MOS/bipolar inverters will, no doubt, become common as MOS use progresses. Additional characteristics and application concepts are given in Reference 6.

Precision Comparator

The new high beta, low noise monolithic process makes it possible to achieve the high input impedance and low offset required for 10 bit telemetry A/D comparison; and the use of careful circuit design permits the necessary switching speed without gold doping (as is used in memory sense amplifiers). It is clear from the requirements, that a comparator satisfying the 1 Mbit A/D encoding application can inherently serve as a PDM (or a ramp A/D) comparator as well. Because it is built with a relatively non-critical, all diffused process, this comparator is expected ultimately to have an economic advantage over other solutions. Its salient characteristics over the full military temperature range are: (1) with offset voltage trimmed to zero by an external resistor, V_{offset} temperature coefficient < 5 μv/°C; (2) offset current, 25 na plus 1.6 na/°C; (3) Rin, > 200 kΩ ; (4) C_{in}, < 10 pf; (5) switching speed with 1 mv overdrive, 300 nsec.

A description of the circuit and more complete parameters are given in Reference 7.

Future LIC's for Telemetry The circuits described in the preceding section are those whose development is most advanced at the authors' firm. Other economical telemetry LIC's which can be expected from present development efforts, in years to come, are:

1. High Performance Differential-in/Differential-out Instrumentation and Light Servo Amplifiers for balanced loads.
2. Precision Film Resistor Arrays and Ladders for A/D's and D/A's.
3. Ultrastable Preamps by thermal control of the die, or use of monolithic chopping circuits.
4. Micropower versions of other Low-Frequency Telemetry Circuits.

5. Monolithic Active Filters for signal conditioners, and FM/FM VCO's and Discriminators.
6. IF Amplifier Blocks using both bipolar and MOS elements.

Conclusion Linear monolithic integrated circuits comparable in performance to present custom discrete circuits will soon become available to simplify the design and construction of the most popular telemetry systems, PCM/ FM/FM, PAM, and PDM. These can not only reduce the parts count and hardware costs of such systems, but can significantly reduce design time and effort because of their mutual compatibility with the majority of telemetry requirements. Gradually, as more LIC's reach production status, not only the most frequently used functions such as signal conditioning, multiplexing, and D/A conversion will be integrated, but all other remote, or vehicle-borne circuits will be integrated to capitalize on the inherent miniaturization, economy, and reliability of IC'S.

Initially, feasibility of the following linear monolithic integrated telemetry circuits is being demonstrated at Fairchild Semiconductor R & D Labs:

1. Micropower Operational Amplifier,
2. Low Level Instrumentation Operational Amplifier,
3. High Slew Rate Operational Amplifier,
4. Junction FET Input Operational Amplifier,
5. 16 Channel Differential Multiplexer,
6. 10 Bit D/A Reference and Current Switches,
7. Precision Comparator.

Acknowledgments

Credit is due the individual developers of the LIC's reported herein, without whom this paper would not be possible: Mr. D, J. Pilling, Dr. G. H. Wilson, Mr. D. J. Fullagar, Mr. K. R. Stafford, Mr. R. C. Barry, Mr. C. M. Botchek, Mr. R. T. Jenkins, and Mr. R. F. Rotunda.

References

1. D. P. Shulz and D. J. Dooley, "Integrating Space Telemetry Systems with Compatible Thin Films on Silicon," Electronics, June 26, 1967.
2. J. G. Hammond, W. F. Link, M. B. Rudin et al, Telemetry System Study, Contr. No. DA-36-039, USA Signal R&D Labs, Dec 18, 1959 (Aeronutronics).
3. D. J. Pilling and G. H. Wilson, "A Micropower Low Noise Integrated Operational Amplifier," ITC/USA '67.

4. D. Fullagar, “A Low Level, Low Noise Integrated Operational Amplifier,” ITC/USA ’67.
5. M. B. Rudin, C. M. Botchek, and R. F. Rotunda, “An Integrated Multi-Channel Differential Analog Multiplexer,” ITC/USA ’67.
6. M. B. Rudin and R. L. O’Day, “A High Speed 10 Bit D/A Integrated Circuit,” ITC/USA ’67.
7. K. R. Stafford, “A Precision Integrated Circuit Comparator for Analog-to-Digital Conversion,” ITC/USA ’67.
8. M. H. Nichols and L. L. Rauch, Radio Telemetry, (John Wiley & Sons, Inc., New York) 1956.

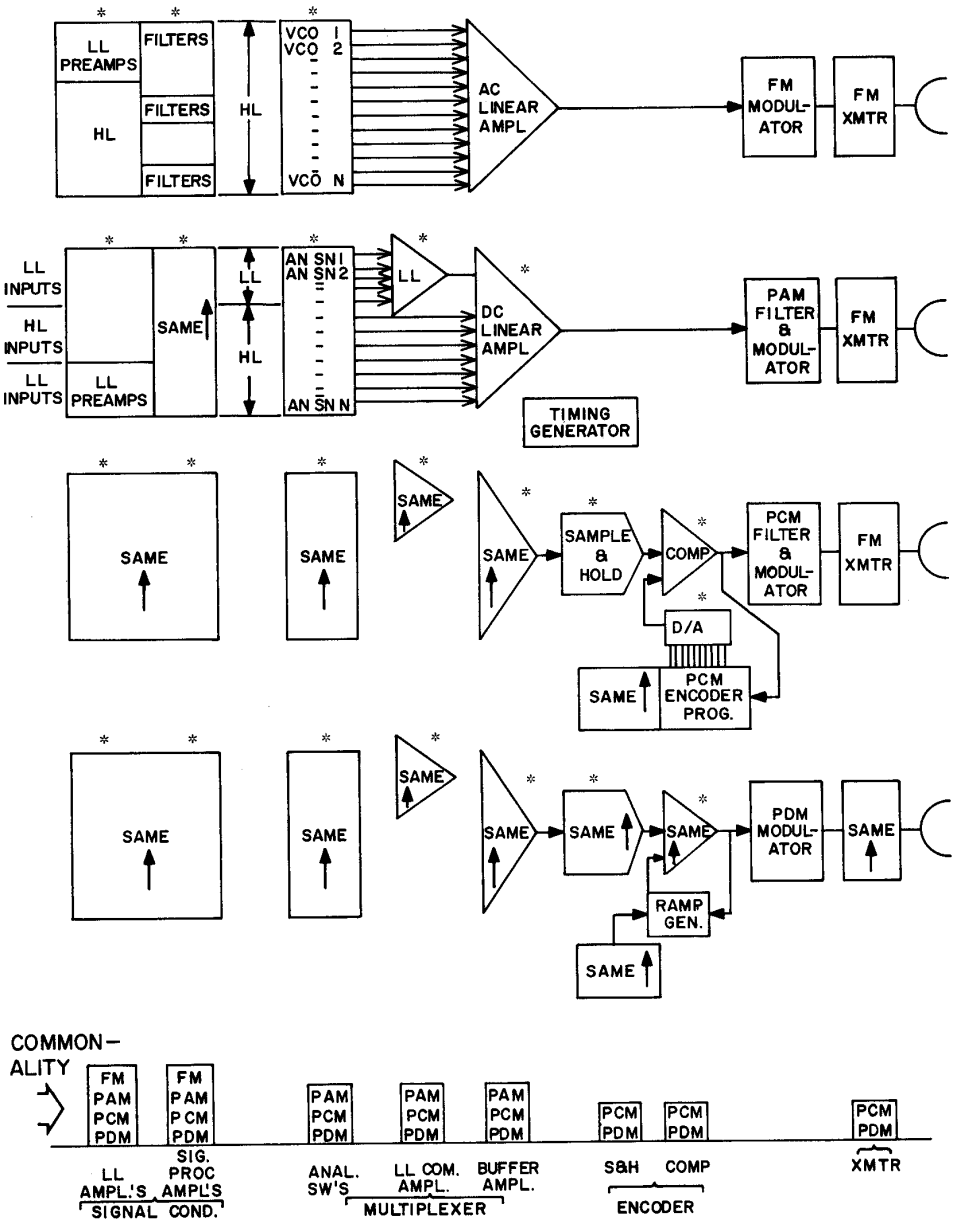

Figure 1A - Remote Analog Data Signal Acquisition Systems for FM/FM, PAM/FM, PCM/FM and PDM/FM Telemetry

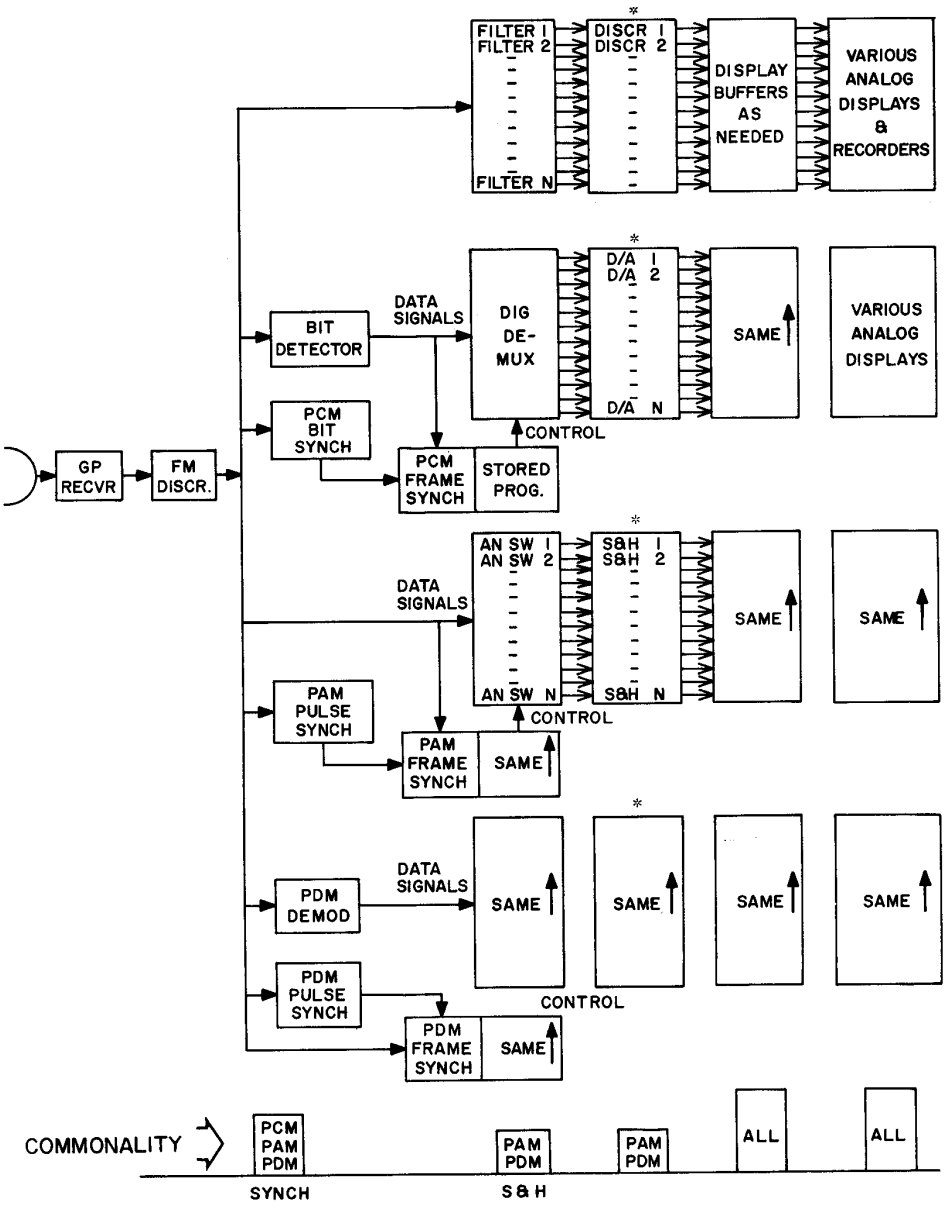

Figure 1B - Telemetry Receiving Station Illustrating Commonality of Circuit Functions for FM, PCM, PAM, and PDM

Preamplifier Op Amplifier		Signal Processor Amplifier	
Total Voltage Offset	$\leq 50\ \mu v$	Total Offset Voltage	≤ 5 mv
Total Current Offset	≤ 50 na	Total Offset Current	$\leq 50\ \mu a$
Input Impedance	*	Input Impedance	$\geq 100\ k\Omega$
Common Mode Ratio	≥ 120 db	Common Mode Rejection Ratio	≥ 66 db
Common Mode Range	$\geq \pm 10$ v	Common Mode Range	$\geq \pm 2.5$ v
Power Supply Rejection Ratio	≥ 100 db	Power Supply Rejection Ratio	$\geq \pm 70$ db
Gain	$\geq 10^5 \pm 10\%$	Gain	$\geq 10^5 \pm 10\%$
Bandwidth	$\geq$ 0-10 kHz	Bandwidth	$\geq$ 0-10 kHz
Output Voltage	$\geq 0 - \pm 5$ v	Output Voltage	$\geq 0 - \pm 5$ v
Output Impedance	$\leq 0.1\ k\Omega$	Output Impedance	$\leq 0.1\ k\Omega$
Power Supply Voltages	$\geq$ CMR	Power Supply Voltages	$\geq$ CMR
Power Consumption	≤ 10 mw	Power Consumption	≤ 10 mw

* Case I: LL Ground Input $\geq 1\ \text{Meg}\Omega$

Case II: LL Differential Input

Low R_S ($R_S < 100\ \Omega$), or $I_{source} \geq 1\ \text{Meg}\Omega$

Case III: LL Differential Input

High R_S ($R_S > 100\ \Omega$)

Int. Feedback Point is required $\geq 500\ R_S = 2.5\ \text{Meg}\Omega$ max.

Figure 2 - Signal Conditioning Circuit Requirements

Analog Switches and Decoders

Channel R_{on} Variation	$\leq \pm 500\ \Omega$ (PCM); $\pm 3\ k\Omega$ (PAM); $\pm 1\ k\Omega$ (PDM)
Switching Time	$\leq 10\ \mu$sec (PCM and PAM); 1000 μsec (PDM)
Crosstalk or Leakage Current	$\leq 1\ \mu$a (High Level PCM); 50 na (LL PCM, PAM, PDM)
Signal Range	$\leq \pm 5$ v
Common Mode Rejection	$\leq \pm 10$ v
Protection vs. Spurious Channel Overvoltage	± 20 v (survival)

Common Amplifiers

Input Impedance	≥ 1 MegΩ
Bandwidth	≥ 500 kHz
Gain	≥ 1000 (LL); unity (HL)
V_{out}	0 to $\pm$ 5 v
Z_{out}	$\leq 0.1\ k\Omega$

Figure 3 - Time Division Multiplexing Circuit Requirements

Proportional BW VCO's

Frequencies	0.4 kc to 70 kc $\pm$ .075 %
Frequency Deviations	$\pm$ 7.5% max.
V_{input}	0 to $\pm$ 5 v max.
Z_{in}	500 kΩ min.
$I_{leakage}$	5 μa max.
Linearity	0.5%
Amplitude Modulation	1 db max.

Constant BW VCO's

Frequencies	16 kc to 198 kc $\pm$ .15%
Frequency Deviations	$\pm$ 2 kc, $\pm$ 4 kc, $\pm$ 8 kc

(Other specifications are similar to PBW VCO's)

Figure 4 - Frequency Division Multiplexing Circuit Requirements

Digital-to-Analog Converter for PCM A/D

Accuracy	10 bits ± 1/2 bit Linearity
	8 bits ± 1/2 bit Full Scale Accuracy
	10 bits ± 1/2 bit Resolution
	above performance over ±50° C temp. range
Speed	0 to 1 Megabit/sec
External Reference Option	±10% of full scale (for ratio conversion to eliminate transducer supply variations)
Input Logic Levels	CCSL Compatible (DTL, TTL): 0 to 2.5 v min. range
Analog Output Levels	Voltage: ± 5 v @ < 1Ω source resistance
	Current: ± 2 to 5 ma @ > 1 MegΩ source resistance
Power Supply Voltages	≤ ± Comparator and Op Amp Levels

Precision Comparator for PCM and PDM

Speed (switching time)	300 nsec @ 1 mv overdrive
Total Voltage Offset	≤ 1 to 2 mv (voltage source D/A)
Total Current Offset	≤ 1 μa (current source D/A)
Input Impedance	Resistance > 100 kΩ (voltage source D/A)
	Capacitance < 10 pf (voltage source D/A)
Common Mode Rejection	60 db (central encoder)
	90 db (remote encoder)
Common Mode Range	± 10 v (remote encoder)
Output Logic Levels	CCSL compatible 0 to 2.5 v min. range @ 5 ma
Power Supply Voltages	≥ ± 10 v
Power Consumption	< 150 mw switchable on use for remote encoder

Figure 5 - Encoding and Decoding Circuit Requirements - Pt. 1

Sample-and-Holds

Input Impedance	$\geq$ 100 kΩ (nom.)
Switching Time	$\leq$ 1 μsec
Aperture	$\leq$ 0.1 μsec
Hold Time (Droop < .05%)	$\geq$ 10 μsec

Display D/A Buffer Amplifier

Slewing Rate	.1 v/μsec
Output Current	$\geq$ 5 to 10 ma
Input Voltage Offset	$\leq$ 5 mv
Input Current Offset	$\leq$ 2 μa

FM Discriminators

Frequencies, Deviations, Linearity	Same as PBW and CBW VCO's given previously.
Input Level	$\geq$ 10 mv
Output Level	$\geq \pm$ 1 v
AM Limiting	60 db
Distortion	< 1%
Linearity	.2%
Stability	.5%
Temperature	0 to 50°C

Figure 5 - Encoding and Decoding Circuit Requirements - Pt. 2