

CONCEPTUAL DESIGN OF A PCM DIGITAL RECORDER FOR ON-BOARD APPLICATIONS

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ABSTRACT

On reviewing current PCM on-board data acquisition systems design is not very uncommon to find lots of useful signals being generated together with the PCM stream, such as bit clocks, word clocks, minor and major frame pulses. The purpose of this paper is to demonstrate a conceptual design of a digital recording device that takes advantage of these signals to collect data directly into a computer compatible disk file. Such device can eliminate the need of further PCM signal processing after the test and speed up the conversion process of pure digital sampling values into floating point numbers.

KEYWORDS

PCM Data Acquisition Systems, Decommuration, Digital Recorders.

INTRODUCTION

The process of collecting data on-board of a test aircraft normally involves the installation of numerous analog and digital input devices, a data acquisition system and a recording device. The most popular design of a test data acquisition system is the one that produces a PCM encoded serial signal. Consequently, a very common design of test data recording device is one that takes a PCM signal input and stores it on a magnetic tape media.

To reconstruct original samples encoded in the PCM stream the signal restored from tape needs to be synchronized and decommutated, that is, the serialization process done by the on-board data acquisition system needs to be "undone" before each raw digital sample value is mathematically processed into a floating point number.

Current on-board data acquisition systems generate lots of useful signals, such as bit and word clocks, minor and major frame pulses, together with the PCM stream. The usual PCM signal acquisition devices -- Bit Synchronizers and Decommutter -- produce the same type of signals as result of the synchronization and decommutation process.

These additional signals are in general sufficient for driving the acquisition of a complete majorframe on a digital logic circuitry. Once it can be acquired and stored in some kind of volatile memory, a computer interface can provide access to majorframe data over an I/O bus for further manipulation. In a computer, majorframe data can be sequentially transferred and recorded into a hard-disk file

Conceptually, such a setup can eliminate the need of magnetic tape recorders, bit synchronizers and decommutators for getting PCM data into a computer environment.

Data stored in a computer hard-disk file has many advantages over data stored on magnetic tape media: a) it can be accessed simultaneously by multiple computer programs executing locally or remotely over a network; b) it can be accessed randomly; c) manipulation through a computer program is extremely fast; d) it can be easily transferred to a more permanent optical media such as CD-R or DVD-R, and survive very long storage periods.

The next paragraphs will describe a conceptual device that interfaces directly to a hypothetical PCM on-board data acquisition system and records PCM data words directly into a computer disk file.

HARDWARE COMPONENTS

The device called here simply Digital Recorder has three main hardware modules: a Signal Conditioner Module, a Word Sequencer Module and a Main Computer Module.

These three main components connect to each other and to a particular PCM Data Acquisition System as shown in Figure 1.

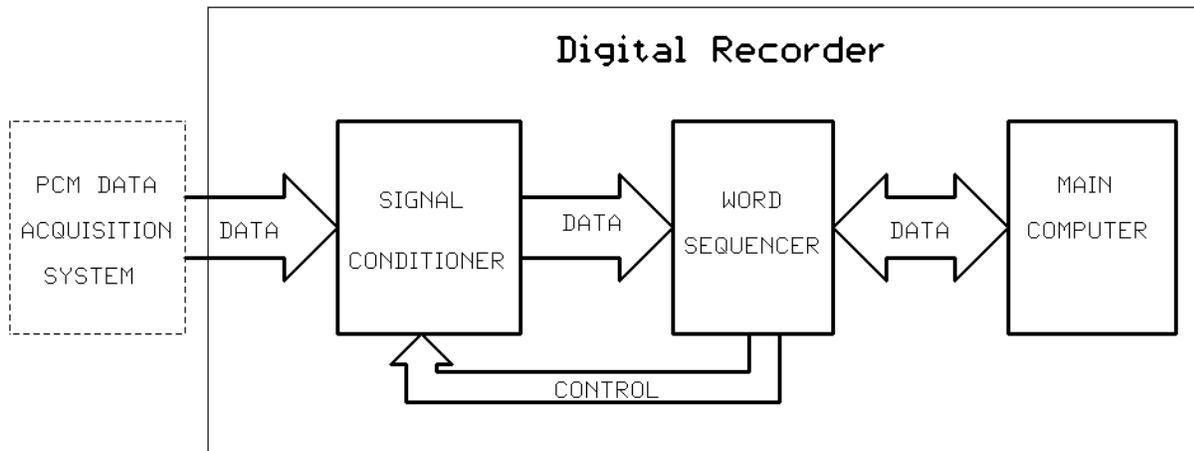


Figure 1 - Digital Recorder Hardware Modules

Signal Conditioner Module

The Signal Conditioner Module (SCM) interfaces directly to a particular PCM data acquisition system converting its available output signals – serial data and clock, word clock, frame strobes, end-of-cycle pulses, etc – into four “standard” output signals: a Bit Clock, a First-Bit Strobe, a Minorframe Strobe and a Majorframe Strobe. In addition, 16 lines of parallel data are produced as part of the input signal processing. The timing diagram for these output signals is shown in Figure 2:

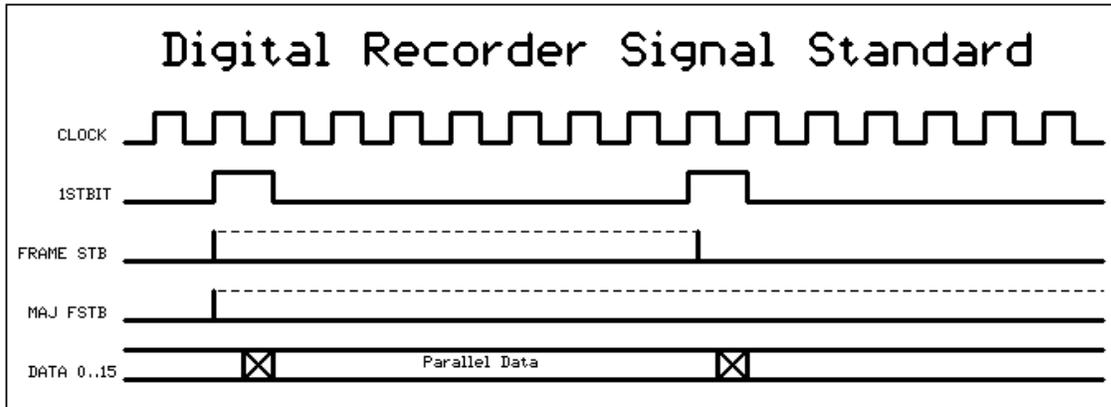


Figure 2 - Timing Diagram for Signal Conditioner Module Output

The Bit Clock is repeated from the original clock signal. The First-Bit Strobe is true for a complete clock cycle (or 2 data bits) starting at the first bit of each PCM word. The Minorframe Strobe is true for the length of a PCM word starting at the beginning of each minorframe. The Majorframe Strobe is true for the length of a minorframe starting at the beginning of each majorframe. The 16 lines of parallel data are available right after each First-Bit Strobe until the next one.

A sample conversion scenario is shown in Figure 3 for a PCM Data Acquisition System that provides a frame synchronization pulse with the length of one data bit with the first bit of the first word for every minorframe, and an end-of-cycle strobe with the length of one word at the end of each majorframe.

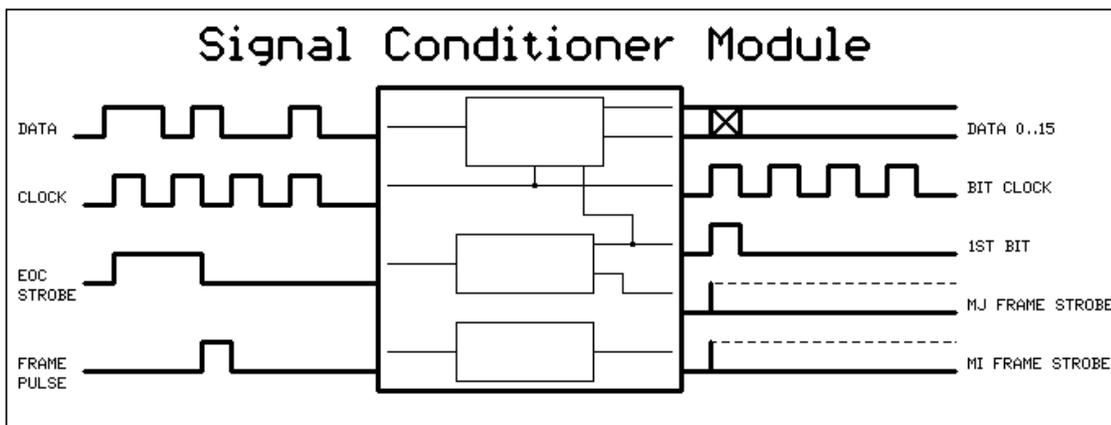


Figure 3 - Sample signal conversion by the Signal Conditioner Module

The purpose of having a SCM is to provide a unique signal interface to the Word Sequencer Module. Typically, each different PCM Data Acquisition System requires a matching SCM.

Word Sequencer Module

The Word Sequencer Module (WSM) interfaces to the SCM through a number of data and clock signals.

Using the First-Bit, Minorframe and Majorframe Strokes the WSM updates three internal registers: Bits/Word, Words/Frame and Frames/Majorframe. The Bits/Word stores the result of counting clock cycles between two consecutive First-Bit Strokes: it must equal the word length in bits of the acquired PCM signal. Similarly, the Words/Frame stores the result of counting First-Bit Strokes between two consecutive Minorframe Strokes -- it must equal the number of words in a minorframe -- and the Frames/Majorframe stores the result of counting Minorframe Strokes between two consecutive Majorframe Strokes -- it must equal the number of minorframes in a majorframe. The WSM uses internal control logic to calculate memory addresses for each data word posted in the 16 data lines coming from the SCM. Each word is stored sequentially in a dual-ported memory right after the First-Bit Strobe. The memory is split in two pages and each page is made available after a majorframe acquisition cycle signaled by the Majorframe Strobe.

Two other internal registers provide status and control over the WSM. The Control Register and the Status Register contents are shown in Figure 4.

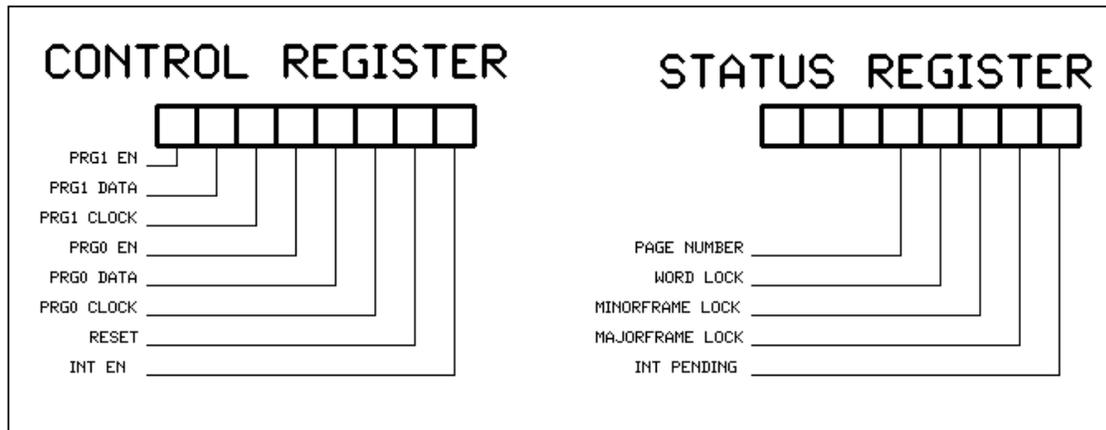


Figure 4 - Word Sequencer Module Control and Status Registers

In the Status Register, the Interrupt Pending bit is set after each majorframe acquisition cycle and cleared by reading the Control Register. If the Interrupt Enable Bit is set in the Control Register, a hardware interrupt is generated. Three other bits, Word Lock, Minorframe Lock and Majorframe Lock reflect the state of the incoming signals generated by the Signal Conditioner Module, mimicking those produced by a standard PCM Decommutator. The Page Number bit signals what page is available for reading.

In the Control Register, the Interrupt Enable Bit is set to cause hardware interrupts after each majorframe acquisition cycle. The Reset Bit is used to bring the WSM to a known initial state. Two sets of three registers allow for field programming integrated circuits in the module.

A Clock Rate Register stores the result of counting Bit Clock ticks within 1-second time intervals. This equals the bit rate of the incoming PCM signal.

The WSM also produces a "freeze pulse" at the beginning of each Majorframe Strobe. This can be used for reading from an external IRIG Timing Module, if time-tagging each acquired majorframe is desired.

Figure 5 shows a functional block diagram for the Word Sequencer Module.

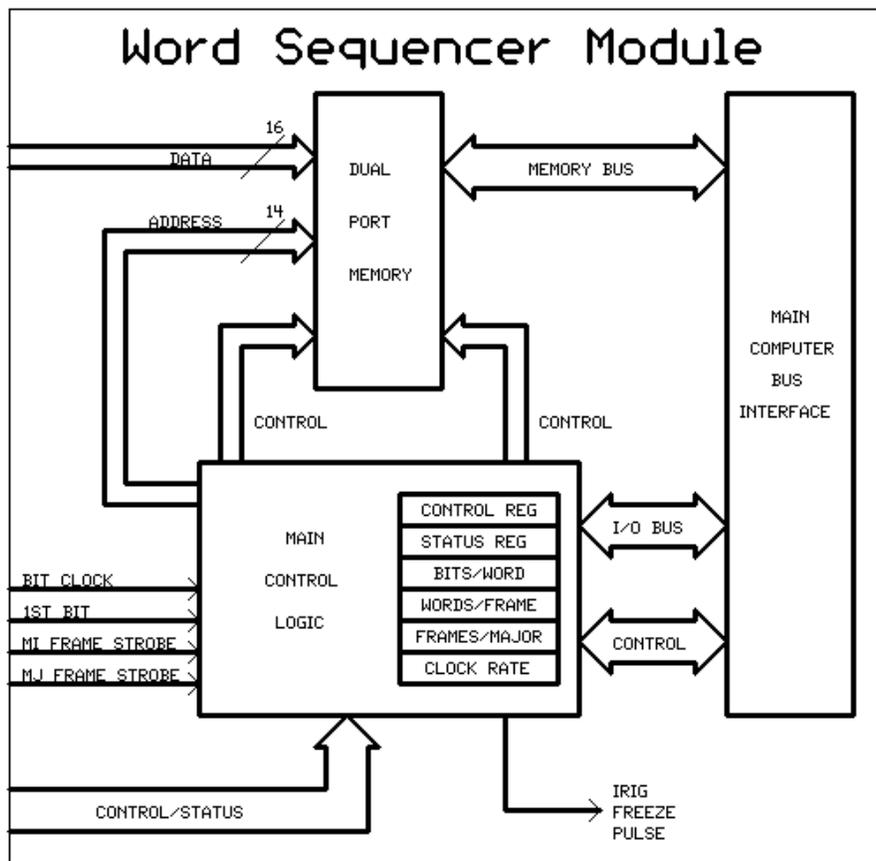


Figure 5 - Word Sequencer Module block diagram

Main Computer Module

The Main Computer Module (MCM) controls the acquisition process by reading and writing Word Sequencer Module internal registers.

It starts the operation by resetting WSM and reading the Majorframe Lock bit in the Status Register to verify its state. During this initial phase it is necessary to know the number of PCM words in a majorframe for dimensioning internal data structures used for recording data to a disk file. This can be calculated by reading and multiplying the values in Words/Frame and Frames/Majorframe registers. Once this is done, the Interrupt Enable bit can be set to start the acquisition process.

The Control Program loaded in the Main Computer memory reacts to each hardware interrupt, copies the contents of the available WSM memory page to its internal data structures and once after a specified number of interrupts writes them to a disk file.

User control over the acquisition and recording process is exercised through a function keyboard and a small LCD display. It is also possible to remotely control the unit by sending commands to the MCM serial communication port. The Control Program polls the serial port expecting reserved "escape" character sequences and executes commands as if they were entered through the keyboard.

The acquisition process ends when the Interrupt Enable bit is cleared. The Control Program, no longer interrupted by the WSM, finishes writing all remaining data to disk and closes the file.

IMPLEMENTATION CONSIDERATIONS

The Digital Recorder concept can be implemented in a compact form factor such as the one described by the PC/104 Consortium [1]. PC/104 modules are 3.6 x 3.8 x 0.6 inches in size and can be "stacked" on top of each other using a standard parallel connector, actually a 16-bit ISA bus. Each PC/104 module can be installed in a small metal frame, just big enough to hold the connectors needed for interfacing with other external devices.

Of the hardware modules needed for the conceptual Digital Recorder, only two are particular to this application: the Signal Conditioner and the Word Sequencer. The Main Computer can be assembled using available PC/104 CPU modules and accessories. The integrated circuits needed for implementing SCM and WSM functions can probably fit in one PC/104 module, so one would expect a very compact design for the resulting device.

Figure 6 shows a block diagram of all the hardware components. Figures 7 and 8 illustrate a possible mechanical design using the PC/104 format. The proposed unit has a power supply, a CPU card (the MCM), a PCMCIA adapter card, an IRIG-Time decoder card, an application specific card (performing SCM and WSM functions), a small LCD display and a function keyboard.

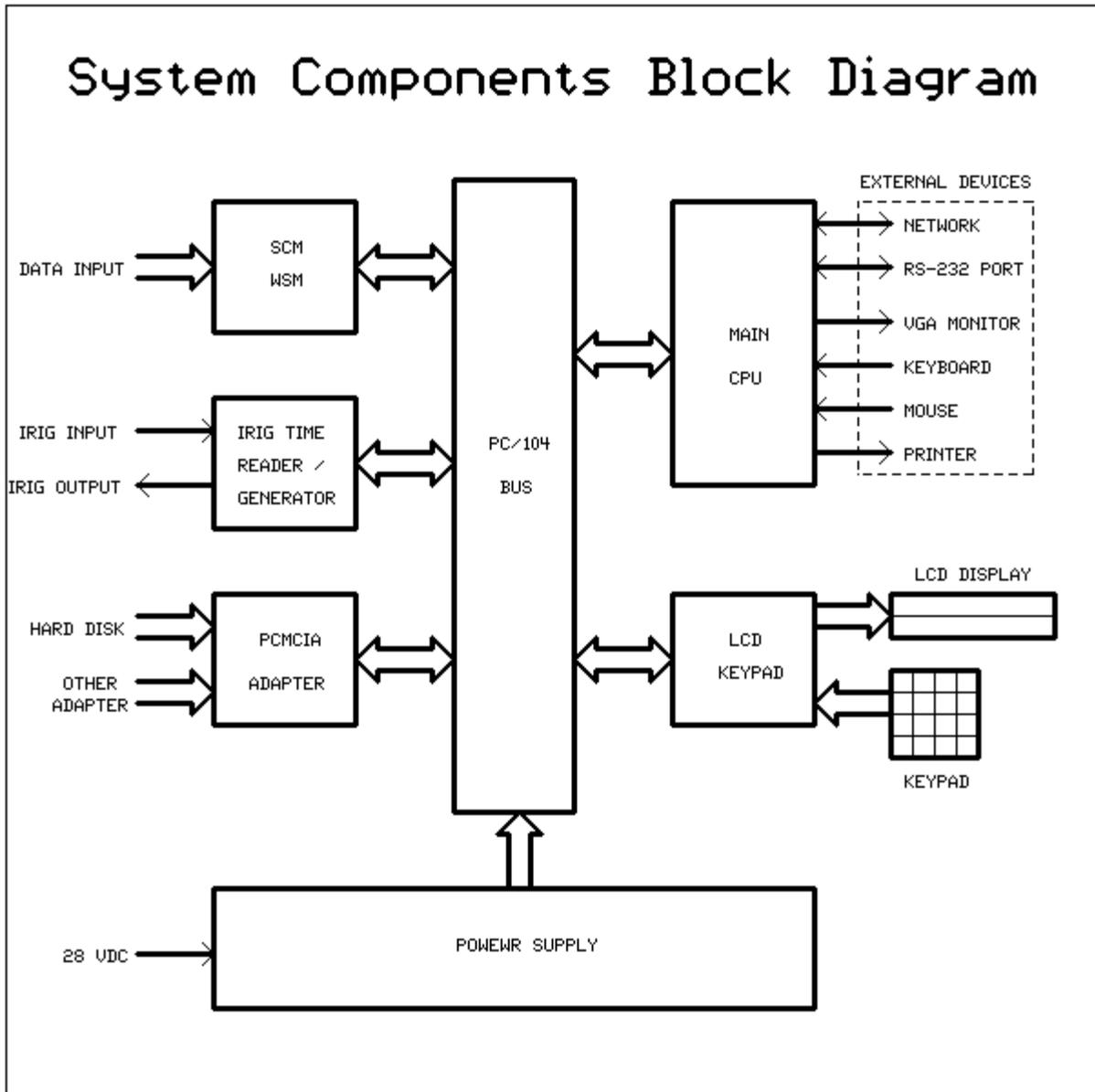


Figure 6 – Hardware components for the Digital Recorder

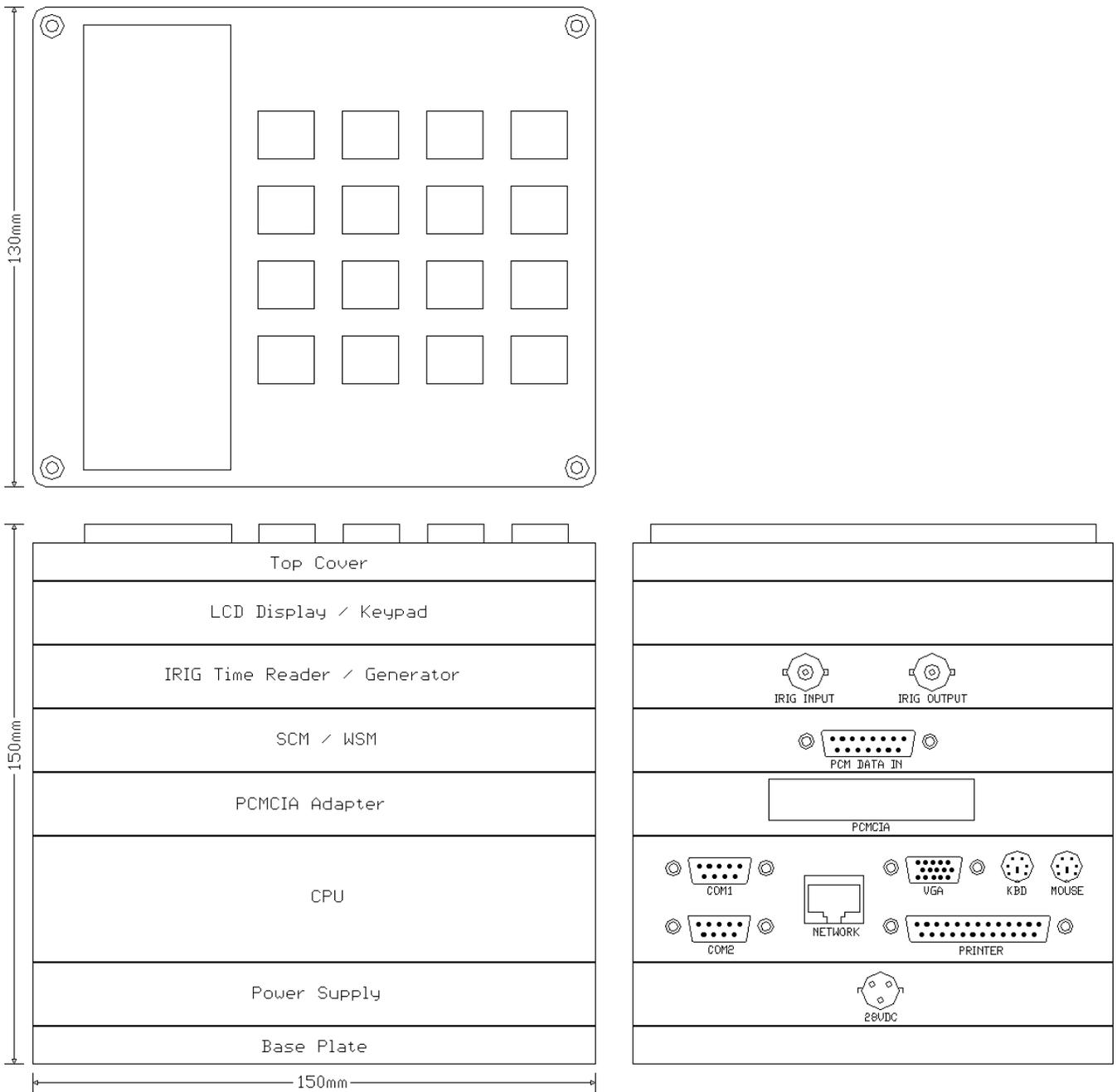


Figure 7 – Prospective mechanical design for the Digital Recorder

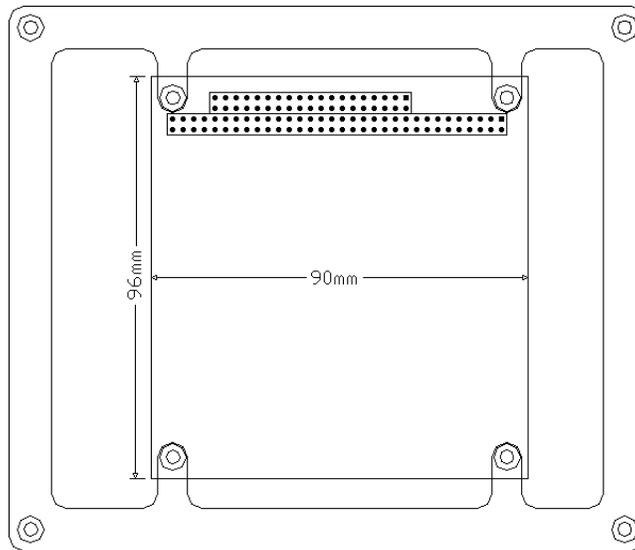


Figure 8 – Typical PC/104 board on metal frame

CONCLUSION

Today's application specific integrated circuit technology leads to more and more software driven components. It is possible to change, add and extend functions of a PC card significantly by reprogramming certain chips in the field, while single-board computers with the size of a wallet with clocks with 233 Megahertz can host applications developed in desktop computer. All this allows us to dream of an unprecedented flexibility when it comes to bridge the gap between specialized hardware and a desktop computer.

On-board PCM data acquisition systems are a breed of specialized hardware that has seldom found replacement throughout the years. Although there are glimpses of new technology being developed [2], much of the basic characteristics have not changed significantly in 10 years. Getting PCM data in a Ground Station computer has always required specialized hardware as well, making the transcription of an analog-to-digital conversion of an aircraft transducer output into a computer environment a very expensive task.

While PCM is required (mostly) for telemetering measurement data collected for a test object to a remotely located site, other alternatives are certainly possible for recording data in a computer installed next to the acquisition hardware. One of these is certainly a device such as described in this paper.

To have all the necessary transducer data available in an environment that is completely dominated by software is in general what a test engineer wants. A device that incorporates a minimum of specialized hardware in an industry-standard computer platform is probably the shortest path between a digitized aircraft transducer output and the engineer's own desktop computer.

REFERENCES

- [1] *The PC/104 Consortium*, P.O. Box 4303 Mountain View, CA 94040
- [2] Alex Karolys and Bruce Swanson, *Pressure Belt – A Smart Sensor Network System for Flight Test*, SFTE 30th Annual International Symposium, August 1999.