PERFORMANCE CHARACTERISTICS AND SPECIFICATION OF PCM BIT SYNCHRONIZER/SIGNAL CONDITIONERS

B. PEAVEY
NASA-Goddard Space Flight Center
Greenbelt, Md

Summary The PCM BR Synchronizer/Signal Conditioner, hereafter called "synchronizer," plays a vital role in telemetry data recovery, and is perhaps the most important and complex component of telemetry data processing systems (DPS). The synchronizer, being the "front end" of the system, makes an irrevocable decision as to the binary value of each data bit, and provides the fundamental timing signal (clock) for the entire DPS. Thus, the performance characteristics of the synchronizer substantially determine the system's capabilities, and it may be said that the system is as good (or bad) as the synchronizer.

This paper presents and discusses test data obtained on synchronizers available to date, and used at Goddard Space Flight Center (GSFC) and its satellite tracking and data acquisition network (STADAN) stations. Performance characteristics such as bit synchronization (bit sync), bit sync acquisition, tracking, bit error rate, and intersymbol interference have been measured with respect to split-phase (SP) and NRZ-L input signals between 500 bps and 300 Kbps, perturbed by "white" Gaussian noise plus jitter. The effect of tape recording and band limiting of these signals on synchronizer performance is also discussed. It is shown that bit error rate alone does not "tell the whole story" about synchronizers, particularly when operating with low (less than 7 dB) SNR's plus jitter.

The test data indicate that there is no single synchronizer excelling in all respects. For example, a synchronizer which operates well down to SNR of -3 dB has inferior acquisition, and slippage characteristics when jitter is added to noise. Generally, the performance threshold for random jitter (defined later) is at SNR greater than 10 dB. Some synchronizers seem to perform better with SP than NRZ-L signals, and vice versa.

Finally, discussed and suggested are definitions of performance parameters which would uniformly and unambiguously describe and specify synchronizers. A lack of precisely defined and measurable performance parameters and characteristics has caused misinterpretation and misunderstanding of specifications presented by both vendor and customer.

Introduction PCM telemetry has been in use for almost 10 years. During this time PCM synchronizers have gone through several design cycles, each time having achieved an improvement in performance. How well, or how poorly, have these synchronizers performed with respect to the purpose for which they were designed? How capable are the "state-of-the-art" synchronizers, and how can they be characterized? These are the basic questions to be considered.

Almost every synchronizer model available to date has been tested to obtain the data presented in this paper. It can be stated that all of them perform well at SNR greater than 15 dB (defined later) plus some jitter, base line variation, and frequency offset, for random SP or NRZ-L data. Therefore, we are not concerned about performance characteristics at high SNR's, rather, at SNR's less than 7 dB at which recovery of data is still possible even though the bit error rate is greater than 1×10^{-3}. In fact, in some cases data having error rates up to 20% (SNR of -4 dB) can be made useful. Coded telemetry data can be error-corrected to effect a gain of about 7 dB [5], which means that a -4 dB SNR signal can be recovered with the equivalent error rate of a 3 dB SNR signal, producing an effective error rate reduction of 7:1!

Clearly, the ability of the synchronizer to maintain bit synchronization is of utmost importance to frame synchronization and, therefore, to decommutation of telemetry data. It has been found that even relatively little jitter, well within the tracking range of the phase-lock-loop, produces bit slippage (loss of bit sync) at SNR less than 10 dB. The effect of this on data recovery is appreciated when one considers data frames of, say, 1000 bits, and realizes that each time bit slippage occurs at least 2 frames of data are lost (of course, it is possible to recover one of these at the expense of an inordinate amount of computer time, hardly worthwhile in the author's opinion). Consequently, test data on synchronization characteristics, including bit sync acquisition time, and tracking, have been obtained for simulated signal conditions, as well as actual telemetry data.

This paper begins with the definition and discussion of performance parameters and characteristics on which test data has been obtained. This is followed by the presentation and discussion of the test data. The next section describes the methods and instrumentation employed. Lastly, a possible way of unambiguously specifying synchronizers is suggested. The conclusion inevitably completes the paper.

Performance Parameters The parameters (also referred to as signal conditions) affecting the performance of synchronizers are:

1. Signal-to-noise Ratio (SNR)
2. Signal jitter
3. Signal amplitude
4. Signal wave form

5. Signal base line and DC offset
6. Signal pattern (data contents, i.e., distribution of the 1’s and 0’s)
7. Signal code, i.e., SP, NRZ-L, etc.

In this paper, these parameters are defined as follows:

1. SNR - this is the ratio of rms signal to rms noise referred to the signal base band (also referred to as signal frequency or data bit rate), and is measured in dB. This definition is equivalent to “signal energy per bit per noise power density” (ST/N_o).

2. Signal jitter - is defined as the frequency deviation, Δf, from the nominal signal frequency at a given rate, f_m (modulating frequency) or a known spectral distribution as shown in Figures 1 and 2. Of course, Δf may vary from a positive to a negative value in a sinusoidal or any other specified manner. Both Δf and f_m are given in % of signal frequency.

This definition is chosen because Δf can be easily simulated by modulating the test frequency source VCO at any desired f_m, or over any random range of f_m’s (as described later), and measured accurately and directly by means of an appropriate counter or spectrum analyzer. Since, in our experience, the predominant jitter source has been the spacecraft tape recorder, the produced jitter (wow and flutter in this case) occurs in the form of Δf at discrete and approximately sinusoidal f_m’s. Obviously, since frequency and phase are related (the former being the derivative of the latter), it is possible to convert frequency into phase measurements, and vice versa. However, the difficulty arises in making accurate measurements of phase deviation and the rate at which it occurs. It turns out that the phaselock-loop is sensitive not only to Δf but also to f_m.

3. Signal Amplitude - this is the amplitude range over which the input signal is expected to vary, and is to be accommodated by the input amplifier and AGC.

4. Signal Wave Form - this describes the extent to which the input signal is prefiltered.

5. Signal Base Line - this is defined as the variation of the signal center line (1/2 of peak-to-peak signal amplitude, normally at ground). If this center line does not vary, and is above or below ground, then, it is referred to as DC offset.

6. Signal Pattern - is defined as the distribution of bit values in the data stream. It may also be described by “transition density,” which means the number of transitions from one binary value to the other (“1” to “0” or vice versa) over a given period of time. For example, a transition density of 1/10 means that in 10 consecutive bits there is only one change from binary “1” to binary “0” (or vice versa). It should be noted that for a SP

signal consisting of all 1’s or 0’s, the transition density according to this definition is zero. In other words, this definition distinguishes between signal (voltage) and data transitions.

7. Signal Code - is defined as shown in Figure 4. Inverting the voltage polarities will simply complement the code.

Performance Characteristics Performance characteristics are functions of performance parameters. The distinction between parameters and characteristics is made in order not to lose sight of what is presented to and what is expected from the synchronizer. In its simplest form, Figure 5 shows the basic constituents of the synchronizer, viz., the signal detector/conditioner and the phase-lock-loop (PLL)/bit synchronizer. The detection of data is characterized by the bit error rate (β), and intersymbol interference (I), whereas the clock (or bit synchronization) is characterized by phase shift, bit rate tracking, bit slippage, and bit sync acquisition, all of which affect the recovery of telemetry data, particularly at low SNR’s. Though the data and clock are certainly interdependent, the characteristics of both must be known in order to determine the overall performance of the DPS. Thus, the definitions of performance characteristics considered in this paper are as follows:

1. Clock Phase-Shift - this phase-shift (θ) (also called clock jitter) is defined with respect to the reference frequency which is the data bit rate. The measurement thereof indicates the number of times θ exceeded a prescribed limit in a given sample size. For example, “$\theta > |\pi/2| = 1 \text{ X } 10^{-3}$ means that θ, on the average, exceeded + or - $\pi/2$ once every 1000 cycles (bits).

2. Bit Slippage - is defined with respect to the reference bit rate as an increase or decrease in the clock frequency, or $\theta \geq \pi$. This constitutes loss of bit sync, of course. Bit slippage, s, is measured as the average number of times it occurs over a given period of time. Thus, “$s = 5 \times 10^{-6}$ ” means that, on the average, the clock (PLL) slips 5 times in 10^{6} bits. It is observed that for SP signals loss of phase ambiguity resolution also constitutes bit slippage.

3. Bit Rate Tracking - this is defined as the range of Δf over which the clock is to follow the variable (jittering) reference bit rate both in frequency and within a tolerable θ. Although it may seem redundant because of its similarity to bit slippage, it is included, however, as a performance characteristic for higher SNR’s at which slippage is not expected to occur.

4. Bit Sync Acquisition (BSA) - this is defined as the time (usually in bit periods) required by the PLL to establish and maintain the data bit rate and phase from the

moment the signal has been applied to the synchronizer. The measurement is made with respect to the reference frequency, and the allowed phase-shift, $\Delta\theta$, as shown in Figure 3. For example, bit sync acquisition (BSA) of, say, 1000 bits means that the PLL took 1000 bit periods to acquire (pull in) bit sync and remain in lock for a definite period of time.

5. Intersymbol Interference - by this is meant the sensitivity of the data detector to data bit patterns and band limiting. Any given pattern equally affected by noise, or other disturbance, is expected to be detected with the same number of errors in every bit position by an ideal detector.

6. Bit Error Rate (β) - this is self explanatory. It is measured with respect to the reference data, making a bit-for-bit comparison, and is compared with the optimum for given SNR's. The optimum error rate, P_e, is given by

$$P_e = 1 - \int_{-\infty}^{S/\sigma/\sqrt{2}} \frac{1}{\sqrt{2\pi}} e^{-t^2/2}\, dt$$

where S = signal in volts rms
σ = noise in volts rms (white Gaussian)

and the detector is assumed to be a <u>matched filter</u>. The optimum curve of P_e vs. SNR is shown in Figure 6.

Performance Of Synchronizers The performance data presented herein was obtained on synchronizers employing basically full bit <u>integrate and reset</u> (I&R) or filter and sample (F&S) detectors, and second order PLL's (consisting essentially of a VCO, phase detector, and low pass filter). In all cases, the I&R detector proved to be as good as or from 1 dB to 3 dB better than the F&S with regard to the overall performance.

1. Bit Error Rate vs. SNR: The range of β' s due to various synchronizers represented by curves 1,2,3, and 4, is shown in Figure 6. It is interesting to note that synchronizers designed within the past 2 years (3rd generation, as it were) performed between curves 1 and 2. However, some of these began to slip (approximately at a rate of 2×10^{-6}) at SNR of 5 dB, while others maintained bit sync down to SNR of -3 dB. This performance held for both SP and NRZ-L codes. The signal frequency was stable, and the data was random.

2. Bit Sync Acquisition vs. SNR: Generally, BSA for SNR greater than 7 dB was measured to be less than 1000 bits. This was true for PLL in narrow bandwidth mode so as to produce minimum β. However, at the expense of β, it was possible to reduce the

BSA by an order of magnitude by increasing the PLL bandwidth. A considerable difference in performance was observed for SNR less than dB. Here, by necessity, the PLL had to be in the narrow bandwidth mode, and the BSA increased up to 3000 bits. Some synchronizers which maintained bit sync down to -1 dB of SNR could not acquire even within 10^4 bits, while others acquired within 2000 bits. For SNR of -3 dB, it took, on the average, 3000 bits (certainly not by design!).

3. Bit Slippage vs. SNR + Jitter: For random jitter, as shown in Figure 2, at Δf of ±1.5% and f_m randomly distributed up to 3%, a minimum SNR of 7 dB (magic number?) was required for the “best” synchronizer to produce an average slippage rate, s, of 1.6 x 10^{-5}. The degradation of β due to this amount of jitter was 2 dB (i.e., without jitter $\beta = 2 \times 10^{-3}$, while with jitter $\beta = 1 \times 10^{-2}$). The same synchronizer, for SNR of 10 dB, had s of 3×10^{-6} (and $\beta = 1 \times 10^{-3}$) , and for SNR of 15 dB, had s less than 1×10^{8} (and $\beta < 1 \times 10^{-5}$). The other synchronizers did considerably (1 to 2 orders of magnitude) worse. The BSA was not affected appreciably either way. In this test, it was observed that some synchronizers favored SP while others performed somewhat better with NRZ-L data.

In the following 2 tests, the signal frequency was modulated with (a) Δf of ±. 5% and (b) Δf of ±1.5%, both at sinusoidal f_m’s, as shown in Figures 7 and 8, respectively. In Figure 8, s_1 and s_2, with corresponding, β_1 and β_2, apply to 2 representative synchronizers tested under the same conditions. In Figure 7, s_2 and s_3 correspond to the same synchronizer but for different SNR’s, while s_1 corresponds to another synchronizer (same as s_2 in Figure 7). All synchronizers tested fall into one of these 2 performance characteristics. Although the intent here is not to discuss the reasons for these differences, it is relevant to state that the designs of the corresponding PLL’s are different.

Referring to Figure 8, it is evident that the effect of f_m on the slippage rate is significant. Note that over a certain range of f_m, slippage increased sharply. Slippage above 1×10^{-3} was not actually measured, therefore the dotted portions of these curves are questionable. However, it was observed that even in these regions the PLL’s did not slip (i.e., maintained bit sync) once in a while. For smaller A f (up to ±0.5%) slippage decreased considerably with both types of PLL’s, however, as shown in Figure 7, one type remained fairly constant, while the other produced maximum slippage of 3×10^{-5} over a narrow range of f_m, outside which slippage diminished by an order of magnitude.

For higher SNR’s up to 15 dB the curves maintained roughly the same shapes. It is interesting to note that even at SNR of 15 dB and Δf up to ±1.5%, slippage up to 4 X 10^{-5} did occur within the same sensitive range of f_m as at the lower SNR’s. As before, the applied data was random, and the performance held equally for SP and NRZ-L, as well as for different bit rates.

4. Bit Error Rate vs. Band Limiting: This test was made to determine the effect on β by limiting the signal and noise bandwidth, as is the case in actual operation with tape recorders and demodulators. By band limiting the signal and noise with a low-pass filter (SKL, Model 302, 36 dB/octave) the following data were obtained:

(a) For SP code, band limiting at twice the bit rate produced a degradation in β of 0.5 dB to 1.5 dB with various synchronizers.

(b) For NRZ-L code, the same results were obtained for band limiting at bit rate, and a degradation of 1 dB to 2 dB was observed for band limiting at 1/2 bit rate.

Similar results were obtained when the signal and noise were recorded at tape speeds producing approximately the same band limiting effect. It is worth noting that for a small penalty in performance it is possible to save magnetic tape by recording at higher densities.

5. Tracking: In discussing this data, a distinction is made between static and dynamic tracking. When the signal bit rate is off by a fixed amount from the expected, i.e., Δf at zero f_m, tracking will be considered as static. Otherwise, when f_m is not zero, tracking will be dynamic.

Most synchronizers performed well within their respective tracking ranges for static Δf. Some exhibited negligible degradation in β, and s, for Δf up to 40% (not measured for Δf > 40%), but required a minimum SNR of 7 dB, and more than 10^4 bits to acquire bit sync. Some required higher SNRI's (up to 10 dB) as the Δf increased (up to 10%) and the PLL bandwidth was extended correspondingly, but the BSA was not affected. Other synchronizers tracked statically up to Δf of 3% at SNR greater than 1 dB, with attendant slippage within the range of 1×10^{-5} to 1×10^{-7} at SNR's less than 5 dB, and negligible ($< 1 \times 10^{-7}$) slippage for SNR > 5 dB.

Dynamic tracking was not generally accomplished without slippage, as mentioned previously, except at SNR greater than 15 dB. At Δf less than .1% and all f_m, or Δf up to 3% and f_m less than .01% tracking was performed without appreciable degradation in β, s, and BSA for SNR's greater than 1 dB.

6. Performance vs. Base Line Variation: This perturbation in addition to noise and jitter, does, as expected, degrade the overall performance considerably. Variations of less than 20% of signal amplitude at frequencies less than 0.1% of bit rate were tolerated by most synchronizers for SNR greater than 7 dB. However, when added to jitter, both s and β increased considerably beyond the acceptable level of performance.

7. Performance vs. Transition Density: As one would expect, synchronizers are more sensitive to low transition densities (TD) of NRZ-L than SP data. With NRZ-L data having an average TD of 1/20 the BSA increased by a factor of 2 or 3, and tracking became more critical. However, for SNR greater than 15 dB (based on random data), TD of 1/32, and stable bit rate, it was still possible to acquire and maintain bit sync. In case of SP, the performance was slightly better, but the ambiguity resolution problem kept cropping up. Once in sync, however, the synchronizers were able to maintain it for more than 10^7 bits.

8. Intersymbol Interference: Although tests on this characteristic have not been completed, it is worthwhile to report on the preliminary findings as follows:

(a) there is a measurable difference of bit errors vs. bit pattern in various synchronizers,
(b) some synchronizers are sensitive equally to both strings of 1's and 0's, while others are sensitive more to one string than the other (a string in this case consists of no more than 6 consecutive 1's or 0's),
(c) the ratio of the largest to the smallest number of errors in given bit positions of a data pattern varies among synchronizers from 2:1 to 5:1 (the ideal ratio would be 1, of course).

These results were obtained for SP data with noise being the only error causing agent. Tests including NRZ-L data, and perturbations in addition to noise are yet to be performed.

Synchronizer Test Facility The synchronizer test facility is shown in Figure 9. Equipment not commercially identified or listed herein is "home made."

1. Signal Source: Both NRZ-L and SP data were generated by the Bendix SPS-2000 stored program simulator and the random (as random as a noise diode can produce) signal generator. Except where noted, the signal was "square" and balanced about ground.

2. Perturbation Source: "White" Gaussian noise was obtained from an Elgenco 610A noise generator. Jitter was produced by modulating the bit rate source VCO with a Wavetek Model 111 signal generator, which was also used to provide base line variation.

3. Test Equipment: The test equipment consisted of the Data Analyzer and Test Instrumentation subsystems. The Data Analyzer (DA) was capable of frame synchronization, frame sync shift measurement, frame sync bit error rate measurement, and detection of deterministic data patterns up to 32 bits. Various timing and gating signals for the requisite measurements were also provided by the DA. The Test Instrumentation (TI) consisted of a bit comparator, phase comparator, ratio counter,

sample size control, bit delay (continuous and discrete up to 11 bits) error strobe control, linear wide band adders, low pass filters up to 1 MHz, HP 3400A true rms meter, HP 5532A counters, and appropriate interfaces to a printer and digital recorder.

4. Tape Recorders: Two analog tape recorders, Ampex FR600 and CEC VR2600 were used.

5. Auxiliary Equipment: A phase modulator and RF signal generator, built for GSFC by Dynatronics, RF receiver built for GSFC by General Dynamics, and an Electrac 215 phase lock demodulator were used to verify some of the simulated tests.

Measurement Methods The following is a description of the basic approach taken to obtain the data presented in this paper.

1. Signal and Noise Measurement: Both signal and noise were measured at the <u>input</u> to the synchronizer. The signal was always "square" and "random," while the noise was band limited (lowpass filtered) to 5 times bit rate up to 200 Kbps, and less above 200 Kbps. This meant that the actual noise power applied had to be No + 7 dB (assuming that a 36 dB/octave roll-off was sharp enough), where, in general, N = No + 10 log (NBW/BR) + 10 log (ENBW/NBW). The signal was also measured in dB with the same rms meter. It was observed that the rms voltage of a "square wave" and that of a "random square" signal, both balanced about ground, was practically the same. Therefore, no correction factor was necessary to account for the difference in wave form, particularly at bit rates greater than 100 Hz. When NRZ-L low transition data was tested, the signal measurements were actually made with "random" data, and then the data format was changed by program from "random" to low transition density.

2. Signal Jitter (Af at fm) Measurement: The amount of jitter introduced to the signal was produced by modulating the source frequency VCO of the signal simulator. The amplitude of the modulating frequency, f_m, was adjusted until the signal bit rate deviated by $\pm\Delta f$, which was measured by a frequency counter (at very low f_m) , and verified by a spectrum analyzer. Once Δf was established, fm was increased to the desired value, while continuously monitoring its constant amplitude on the scope, in order to ensure the same Δf for the entire range of single f_m's.

The "random" distribution of f_m was derived by modulating the source VCO with "random" noise, which was band limited to the desired cutoff frequency by the low pass filter. The noise amplitude was adjusted until Af as observed on the spectrum analyzer reached the desired range (See Figure 2).

3. Bit Slippage Measurement: This measurement, perhaps the most difficult from an accuracy point of view, was made in 2 ways (a) by employing the DA where loss of frame sync was produced solely due to slippage, and (b) by using the TI to determine clock phase shift and clock ratio with respect to the reference frequency. In the first case, it was established beforehand that by allowing the frame sync (actually any periodically occurring pattern of 32 bits) to have between 30% and 40% bit errors in the lock mode, the loss of frame sync was then due exclusively to bit slippage for SNR greater than -3 dB and sample sizes up to 10^7 bits (larger samples were not used). The frame length was selected judiciously to be 256 bits so as to make the measurements accurate to approximately within 500 bits. This means that if " $s = 1 \times 10^{-4}$ " it may actually have been 1/9,500 or 1/10,500. Actually, for SNR greater than 7 dB, the accuracy was within 256 bits, because the frame synchronizer took, on the average, 1 frame to correctly acquire frame lock with 5% to 10% allowed bit errors. The measurement consisted of observing the frequency of frame sync losses over a given period of time (bits). By proper application of control signals, it was possible to discount the time during which the PLL was not in lock.

The second method was used for verification during preliminary tests, which were to correlate the "frame sync loss" observations with both the θ equal to or greater than π and clock ratio measurements. Bit slippage was exhibited by the clock not being equal to the reference frequency (or the ratio $\neq 1$), or θ being equal to or greater than π. Having established the validity of the first method, the second method was then used alone to obtain the final data.

4. Bit Sync Acquisition Measurement: This measurement was made in accordance with the definition given previously. The TI determined the number of bits the PLL required to pull-in within 90° of the reference frequency. This was verified by the DA, which counted the total number of bits taken to acquire frame sync from the time the signal had been applied to the synchronizer. Subtracting the average number of frames (1 or 2 depending on SNR and allowed bit errors) required to establish frame lock from the total number of bits counted gave the BSA.

5. Bit Error Rate Measurement: A bit-for-bit comparison was made between the reference and detected data, and the number of disagreements was counted over a given period of time (bits).

6. Intersymbol Interference Measurement: The DA examined the recurring data pattern (up to 32 bits) and each erroneous bit position was recorded on the digital recorder. This information was processed on a computer, which also totalized the number of errors in each bit position.

Specification Of Synchronizers In order to minimize the problem of misinterpretation of synchronizer specifications it is suggested that the definitions of performance parameters and characteristics described in this paper be adopted. It should be recognized that quoting of numbers and/or referring to circuit features, e.g., "difference integral," "phase jitter 20%," etc., without precisely defining them, is simply unacceptable.

To properly specify synchronizers, 4 major aspects must be considered. They are:

1. Signal conditions, i.e., the kind of signals which the synchronizer shall operate with, and for which the required performance is valid;

2. Operational features, i.e., setup, controls, indicators, power requirements, etc.;

3. Performance characteristics, i.e., bit error rate, bit slippage, bit sync acquisition, etc. These characteristics must be stated clearly for specific signal conditions and, preferably, should be accompanied by test data when proposing certain models.

4. Mechanical features and environmental conditions.

Overspecification should be avoided. It is questionable indeed, if there has been an application in PCM telemetry of 1 bit per second signal bit rate, or a need for an overall operational requirement from 1 bps to 1 Mbps. Moreover, it is doubtful whether the user or manufacturer has actually tested the equipment at these extremes under the various signal conditions. Yet, when one reads the specifications it appears to him that this has been done. Therefore, it is recommended that the user accurately describe the input signal of interest, the required response to it, and how both are to be measured. The manufacturer, in advertising his equipment, should state explicitly the test conditions under which the performance data was obtained, and describe the measurement methods used.

Conclusion Test data obtained on PCM synchronizers indicates that SP and NRZ-L signals having stable bit rates and random data can be detected within 1 dB of the optimum for SNR's greater than -3 dB (ST/No). Bit synchronization is shown to be adversely affected by the modulating frequencies, f_m, as well as by Δf. Therefore, when considering jitter perturbations it is not sufficient to know the peak-topeak, or rms phase deviation, but also the manner in which it deviates, i.e., the specific signal characteristic (Δf, f_m) which produces this phase deviation. When jitter is added to the signal in addition to noise, the PLL begins to slip (skip cycles, lose lock) even at relatively high (greater than 10 dB) SNR's. This bit slippage results in loss of frame sync which decreases data recovery. Synchronizers tested and found to have less bit slippage actually recovered more real telemetry data than those which exhibited higher slippage rates, even though the bit error rates were comparable.

The synchronization aspect of synchronizers can be tackled by employing a relatively simple frame synchronizer, 2 counters, a signal simulator, and perturbation generator.

A measurable set of parameters and characteristics defining synchronizer performance has been described, and used to test synchronizers. These definitions are suggested as a possible means of specifying PCM Bit Synchronizer/Signal Conditioners.

Acknowledgment The author wishes to thank Mr. William M. Watt of GSFC, for having implemented the Data Analyzer and for having written the computer program.

References

1. Nichols and Rauch, “Telemetry” ESD-TR-66-464, USAF.

2. M. Schwartz, “Information, Transmission, Modulation, and Noise,” McGraw-Hill, New York, N. Y.

3. A. J. Viterbi, “Principles Of Coherent Communication,” McGraw-Hill, New York, N. Y.

4. Strong and Saliga, “Comparison of Phase-Coherent and Non-Phase-Coherent Coded Communications,” NASA TN D-3079.

5. W. P. Barnes, “A Simulation of Convolutional Encoding With Sequential Decoding,” GSFC, X-563-68-65 (to be published).

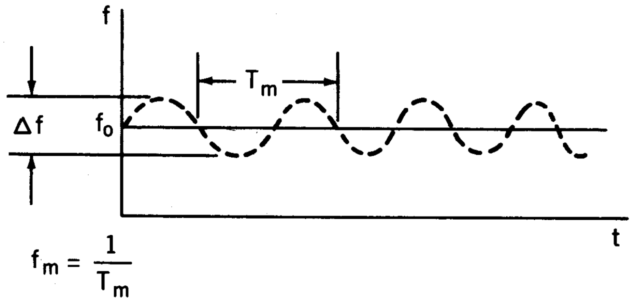

Fig. 1 - Sinusoidal Jitter.

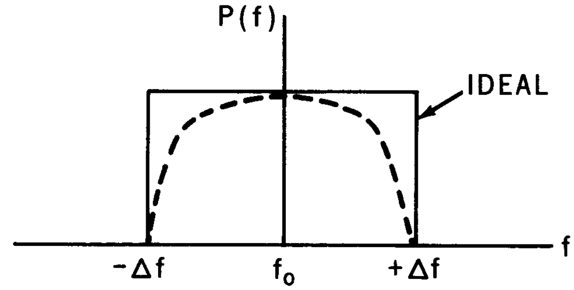

Fig. 2 - Random Jitter.

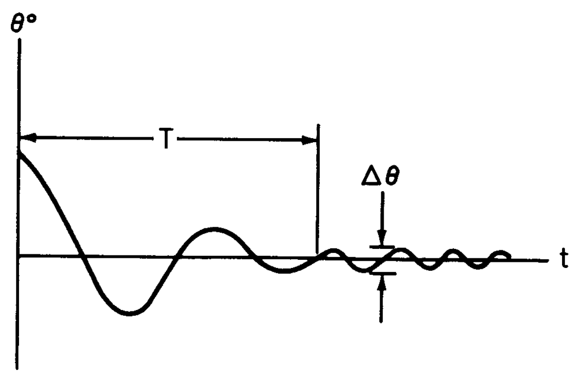

Fig. 3 - Bit Sync Acquisition.

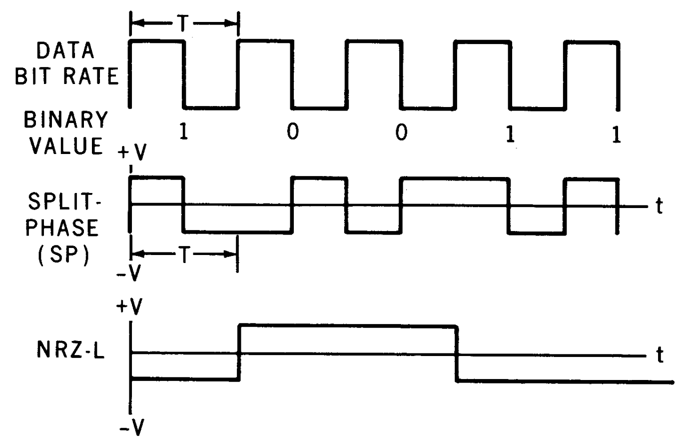

Fig. 4 - Telemetry Data Codes.

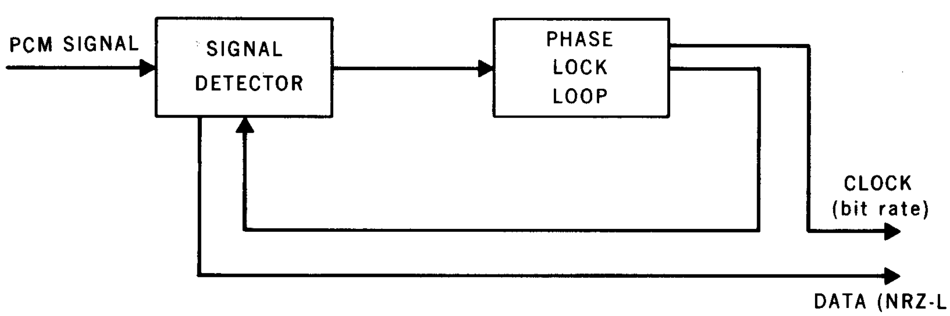

Fig. 5 - Bit Synchronizer/Signal Conditioner.

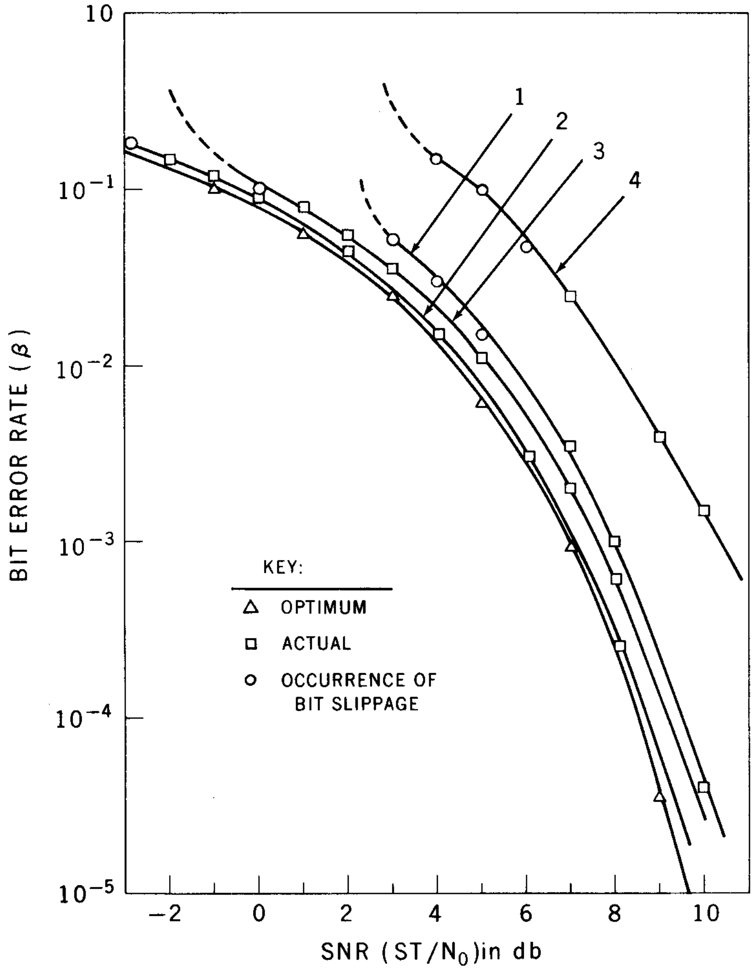

Fig. 6 - Bit Error Rate vs. SNR.

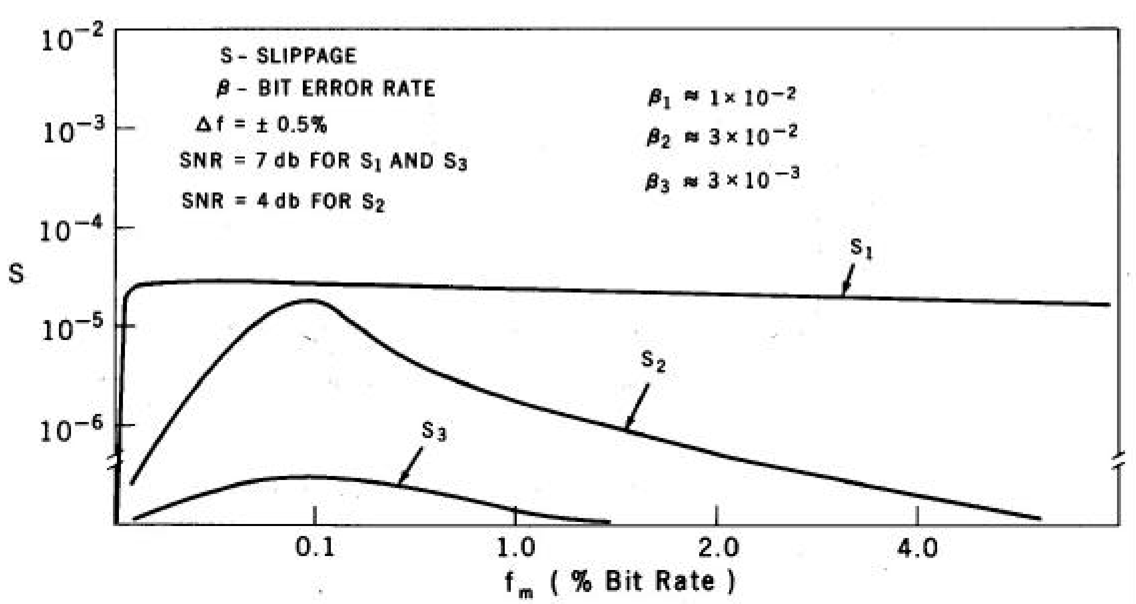

Fig. 7 - Bit Slippage vs. f_m For $\Delta f = \pm 0.5\%$

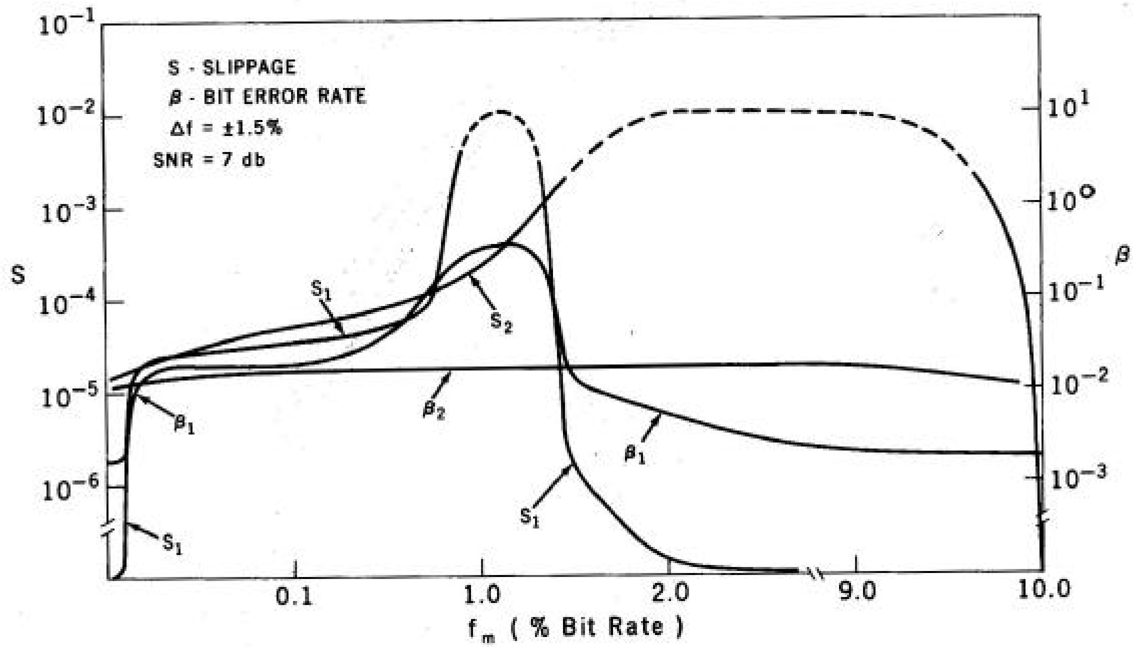

Fig. 7 - Bit Slippage vs. f_m For $\Delta f = \pm 1.5\%$

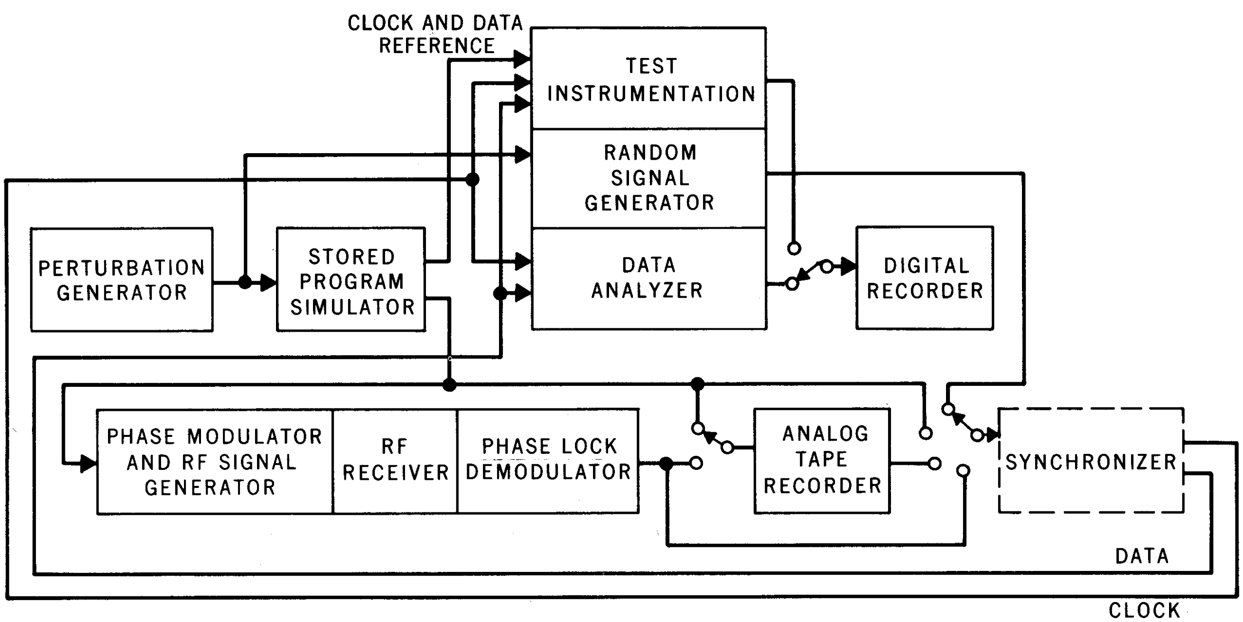

Fig. 9 - PCM BSSC Test Facility.