SYNTHESIS OF HIGH DATA RATE COHERENT TELEMETRY SYSTEMS

L. N. MA
M. S. STONE
D. P. SULLIVAN
Communication Laboratory
TRW Systems Group

Summary For high data rate telemetry (above 100 Mbits/sec) multiphase modulation effectively trades transmitter power to alleviate the RF bandwidth requirements. This paper presents a unified method of synthesizing and analyzing multiphase systems. In particular, the design of multiphase modulators and three types of coherent demodulators are discussed in detail.

Included is a description of 400 Mbits/sec quadriphase system fabricated by TRW which employs direct modulation and demodulation of an 8.5 GHz carrier and a transversal filter to effect matched data filtering. This system operates within 2.5 db of theoretical performance of coherent quadriphase.

Introduction At high data rates, bandwidth is more of a constraint than transmitter power. Therefore, telemetry system performance can no longer be improved by the well known coding techniques that trade bandwidth for signal power. In this situation one must attempt to improve system accuracy by trading signal power for bandwidth. Multiphase modulation systems provide a means of attaining such a tradeoff. As is well known, coherent biphase (PCM/PM) yields almost the lowest probability of error among all multiphase systems. It can be shown that quadriphase yields the same probability of error per bit as biphase but requires one-half the bandwidth of biphase. Higher order phase systems, while requiring less bandwidth for a given data rate, yield increasingly higher error probability for the same transmitter power.

In this paper, methods are given that allow one to synthesize multiphase systems. A description of the methods of modulation is presented. Three ways of demodulation are discussed. They are the multiplier loop, analog I-Q loop, and data estimation I-Q loop. Of these methods the data estimation I-Q loop is preferred.

TRW has fabricated a 400 Mbits/sec quadriphase system which consists of a quadriphase modulator, data estimation I-Q loop, and matched filter data detectors. The performance of this system was measured and found to operate within 2.5 db of the theoretical optimum.

Synthesis of Multiphase Systems A digital N-phase modulated signal without regard to filtering may be represented as

$$S(t) = V \sin(\omega_c t + \theta + \varphi_s(t)) \tag{1}$$

where

V	=	amplitude scale factor
θ	=	arbitrary carrier phase
$\omega_c/2\pi$	=	carrier frequency
$\varphi_s(t)$	=	phase modulation; $\varphi_s(t)$ takes on one of N discrete values in each baud time

For a quadriphase signal, (1) becomes

$$S(t) = V \sin\left(\omega_c t + \theta + \frac{\pi}{4} F_4(t)\right) \tag{2}$$

where $F_4(t)$ is a four-level pulse train which takes on the values ±3, ±1. Equation (2) may be alternatively expressed as

$$S(t) = \frac{V}{\sqrt{2}} \{A(t) \sin(\omega_c t + \theta) + B(t) \cos(\omega_c t + \theta)\} \tag{3}$$

where A(t) and B(t) are independent rectangular pulse trains which take on the values ±1. From the above it can be seen that a quadriphase modulator can be constructed as shown in Figure 1.

For octaphase the representation is

$$S(t) = V \sin\left(\omega_c t + \theta + \frac{\pi}{8} F_8(t)\right) \tag{4}$$

where $F_8(t)$ takes on the values ±7, ±5, ±3, and ±1. A realization of an octaphase modulation can be obtained by noting that (4) can be rewritten as

$$S(t) = \frac{V}{\sqrt{2}} \left\{A(t) \cos\left(\omega_c t + \theta + \frac{\pi}{8} C(t)\right) + B(t) \sin\left(\omega_c t + \theta + \frac{\pi}{8} C(t)\right)\right\} \tag{5}$$

where A(t), B(t), and C(t) are independent rectangular pulse trains which take on the values ±1. Another form of (5) is

$$S(t) = \frac{V}{\sqrt{2}} \cos\left(\frac{\pi}{8}\right) [A(t) \cos(\omega_c t + \theta) + B(t) \sin(\omega_c t + \theta)] \tag{6}$$

$$+ \frac{V}{\sqrt{2}} \sin\left(\frac{\pi}{8}\right) [B(t)\, C(t) \cos(\omega_c t + \theta) - A(t)\, C(t) \sin(\omega_c t + \theta)]$$

The equation above shows that octaphase can be viewed as the sum of two dependent quadriphase signals of unequal level. Further manipulation yields

$$S(t) = \frac{V}{\sqrt{2}} \sqrt{1 - \frac{1}{\sqrt{2}}} \left\{ A(t) \cos(\omega_c t + \theta) + B(t) \sin(\omega_c t + \theta) \right. \qquad (7)$$

$$\left. + D(t) \cos\left(\omega_c t + \theta + \frac{\pi}{4}\right) + G(t) \sin\left(\omega_c t + \theta + \frac{\pi}{4}\right) \right\}$$

where

$$D(t) = \frac{1}{2} \{A(t) - B(t) + C(t) [A(t) + B(t)]\}$$

$$G(t) = \frac{1}{2} \{A(t) + B(t) + C(t) [B(t) - A(t)]\}$$

This last equation shows that an octaphase modulator may be constructed by summing the outputs of two dependent equal level quadriphase modulators as shown in Figure 1. The procedure outlined above may be easily generalized to design of multiphase modulators.

Coherent detection of an N-phase signal entails obtaining a carrier reference and demodulating the data. Assuming for the moment that such a reference exists, one may describe the detection process vectorially.

The received signal can be represented as a vector of the form

$$\overline{X} = V \overline{S} + \overline{N} \qquad (4)$$

where

$$\overline{S} = \begin{pmatrix} \cos \varphi_s \\ \sin \varphi_s \end{pmatrix}$$

$\overline{N}$ = two dimensional noise vector

The demodulator is thus a device that operates on this vector so as to determine which signal was sent with the smallest probability of error. It can be shown that if each signal has equal probability of being transmitted and is perturbed by white gaussian noise, then the receiver should select the signal point closest to the received point.[1] Geometrically, this means that the plane should be divided into disjoint areas or decision regions. An N-phase demodulator will have N regions, each encompassing $2\pi/N$ radians.

An N-phase demodulator requires N/2 phase detectors and associated equipment as illustrated in Figure 2. By placing the phase detector references orthogonal to the boundaries of the decision regions, the output of each phase detector and integrate and dump circuit combination, which is obtained by comparing the output to a threshold, represents a specific region of the plane. Then by performing logic operations on these outputs, the decision regions are realized.

In order to accomplish coherent detection, it is necessary to provide a carrier reference at the receiver. The alternative to transmitting a residual reference is to construct a suitable reference from the received data modulated signal. For an N-phase PCM/PM signal (disregarding the effect of link filtering on the data signal), this can be accomplished by multiplying by N, filtering, and then dividing by N. This removes the data and provides a reference which has a $\log_2 N$ bit ambiguity. A tracking loop is desired for the filtering operation to provide a narrow filter after the multiplication and to track the time variations of the carrier phase. One wants to limit the bandwidth of the noise before the nonlinear device but would still like to preserve the phase transitions in the signal. Thus, the predetection and/or post-modulation filtering operation becomes a tradeoff between preserving the signal waveshape and limiting the noise power. A basic multiplier loop to provide a reference for N-phase is shown in Figure 3. In this mechanization, the VCO output is multiplied by N to provide the phase detector reference for carrier demodulation of the signal. This is equivalent to the use of a divider in performance. The multiplier is simpler to construct and operate and only affects the frequency at which the VCO operates.

The error signal developed by the N-fold multiplier loop is essentially sin [$N\epsilon(t)$], where $\epsilon(t)$ is the difference between the input carrier phase (excluding data transitions) and the VCO phase. An alternative mechanization of this loop, referred to as the in-phase/ quadrature (I-Q) loop, can be generated by simply expanding sin [$N\epsilon(t)$] as follows:

$$\sin[N\epsilon(t)] = 2^{N-1} \prod_{m=1}^{N} \sin\left[\epsilon(t) + \frac{m-1}{N}\pi\right] \qquad (9)$$

The generalized I-Q loop of (9) and Figure 4 simply consists of N-phase detectors separated in carrier phase by π/N, the outputs of which are multiplied together to provide an error signal to drive the VCO. The only essential difference between the multiplier loop and the I-Q loop is that the I-Q loop allows filtering of the data at the outputs of the various phase detectors before the final multiplication derives the error signal. The equivalent filtering for the multiplier loop must be done in the IF filters before the multiplier. This limits the flexibility somewhat. Given the outputs of any two of the N-phase detectors of Figure 4, the output of any other can be generated by a linear combination of these two. Therefore, the I-Q loop can be implemented by two phase detectors, summers, and the product device which multiplies all of its inputs.

Inherent in the operation of the phase tracking loops discussed to this point is that noisy signals are multiplied together. This problem is largely overcome by the use of the so-called data estimation I-Q loop. This type of loop may be realized by passing the output of the phase detectors through lowpass filters and operating on the resultants in a linear manner. In the absence of noise, these outputs, $L_i(t)$, when the phase error is equal to ϵ are

$$L_i(t) = V \cos\left(\varphi_s(t) - \varphi_R{}^i - \epsilon\right) \quad i = 1, 2, \ldots, N/2 \tag{10}$$

$$= V\left[\cos\left(\varphi_s(t) - \varphi_R{}^i\right)\cos\epsilon + \sin\left(\varphi_s(t) - \varphi_R{}^i\right)\sin\epsilon\right]$$

where $\varphi_R{}^i$ = phase of the i^{th} reference. By proper operations on these outputs, the $\cos(\varphi_s(t) - \varphi_R{}^i)$ and $\sin(\varphi_s(t) - \varphi_R{}^i)$ terms can be estimated, thus making it possible to solve the above N/2 equations for the VCO control signal $\sin\epsilon$ as shown in Figure 5. Errors in estimating these data will cause the control signal to be incorrect for time intervals equal to the bit time interval. However, the smoothing of the loop filter will prevent small numbers of errors from affecting the loop appreciably.

For quadriphase, using (3), equation (10) becomes

$$L_1(t) = V\,[A(t)\cos\epsilon - B(t)\sin\epsilon] \tag{11}$$
$$L_2(t) = V\,[A(t)\cos\epsilon + B(t)\sin\epsilon]$$

At high signal-to-noise ratio, A(t) and B(t) may be estimated by passing $L_1(t)$ and $L_2(t)$ through limiters. Using these estimates, designated $\hat{A}(t)$ and $\hat{B}(t)$ respectively, the VCO control signal can be obtained by multiplying $\hat{A}(t)$ by $L_2(t)$ and $\hat{B}(t)$ by $L_1(t)$ and adding the result, i.e.,

$$V_c = V\left\{\left[A(t)\,\hat{A}(t) + B(t)\,\hat{B}(t)\right]\sin\epsilon + \left[A(t)\,\hat{B}(t) - \hat{A}(t)\,B(t)\right]\cos\epsilon\right\} \tag{12}$$

At high signal-to-noise ratio $\hat{A}(t) \cong A(t)$ and $\hat{B}(t) \cong B(t)$, thus leading to the desired result

$$V_c = 2V\sin\epsilon \tag{13}$$

This loop is shown in Figure 6. Note that by breaking the lead as shown in the figure, the loop may be used for biphase.

Performance of Multiphase Systems This section is devoted to a review of some of the analytical information on multiphase systems that is available in the literature. To begin with, the probability of error is given by

$$P_E = 1 - \frac{1}{\pi} e^{-\lambda^2/2} \int_0^{\infty} dr\, r \exp\left(-\frac{1}{2} r^2\right) \int_0^{\pi/N} e^{\lambda r \cos\varphi} d\varphi \tag{14}$$

where

λ^2 = S/N_oR ($2 \log_2 N$)

S/N_o = signal power-to-noise spectral density ratio

R = data rate

For N = 2, equation (14) becomes

$$P_E = 1 - \frac{1}{\sqrt{2\pi}} \int_{-\lambda}^{\infty} \exp\left(-\frac{1}{2}\beta^2\right) d\beta \tag{15}$$

For N = 4, equation (14) becomes

$$P_E = 1 - \left[\frac{1}{\sqrt{2\pi}} \int_{-\lambda/\sqrt{2}}^{\infty} \exp\left(-\frac{1}{2}\beta^2\right) d\beta\right]^2 \tag{16}$$

Note that on a per symbol basis the performance of biphase exceeds that of quadriphase, but when the two systems are operated at the same data rate their performance is equivalent on a per bit basis.

For larger values of N, (14) must be evaluated by computer. Arthurs and Dym[1] have obtained upper and lower bounds for error probability by geometrical arguments which lead to

$$\frac{1}{\sqrt{2\pi}} \int_{\lambda \sin \pi/N}^{\infty} e^{-x^2/2} dx < P_e < \frac{2}{\sqrt{2\pi}} \int_{\lambda \sin \pi/N}^{\infty} e^{-x^2/2} dx, \quad N > 2 \tag{17}$$

Figure 7 presents the theoretical and measured quadriphase bit error rate versus S/N_oR.

Curves can also be found in Cahn[2] that illustrate the tradeoff between signal power and bandwidth for given error rates.

400 Mbits/sec Quadriphase System In order to verify that a high data multiphase modulation system could be synthesized, TRW undertook a task of building a 400 Mbits/sec quadriphase system. This system consists of a quadriphase modulator, quadriphase demodulator, and matched filter data detectors. Additionally, a set of test equipments which consists of a 31 bit pseudo-random (PRN) code generator, code correlation detector, and bit error comparator, were built to measure system performance. The design and performance of these equipments are discussed in the following sections.

Quadriphase Modulator The quadriphase modulation is performed directly onto a 8.5 GHz carrier. Using the same configuration as shown in Figure 1, the quadriphase modulator consists of two biphase modulators whose carriers are 90° out of phase. Figure 8 presents the completed 8.5 GHz quadriphase modulator. The performance of the modulator is tabulated in Table 1.

Table 1. X-Band Quadriphase Modulator Performance

Center frequency	8.5 GHz
Insertion loss	9.6 db
Maximum RF input	23 dbm
Residual carrier	-54 db

Quadriphase Demodulator The quadriphase demodulator, as shown in Figure 6, is of the data estimation I-Q loop variety and is operated at 8.5 GHz. The complete unit is shown in Figure 9 and its performance characteristics are tabulated in Table 2.

Table 2. X-Band Quadriphase Demodulator Performance

Center frequency	8.5 GHz
RF input frequency stability	≤ 500 kHz peak-to-peak
RF input power	10 dbm
VCO stability	$\leq \pm 6 \times 10^{-5}$
Loop characteristics	
Type	second order
Noise bandwidth, two-sided	600 kHz
Loop gain	10^8
Data output response	lower 3 db ≤ 500 kHz
	upper 3 db ≤ 6 00 MHz

Detection System The detection portion of the system consists of a bit synchronizer and a matched filter. The bit synchronizer generates a local clock by differentiating the received PCM waveform, then frequency doubling the output and filtering with a phase-locked loop.

As shown in Figure 10, the matched data-filter employs a transversal filter[4]. The filter operates as a stair-step approximation to an integrate and dump circuit.

The output of the transversal filter is sampled at the end of each bit period through a bilateral switch. The sampling pulse used to drive the switch is derived from the bit synchronizer output. To reconstruct the data, the sampled output is used to drive a decision-and-hold circuit. Figure 11 depicts the noise corrupted input to the data filter and the resultant reconstructed output.

Bit Error Rate Measurement The configuration for measuring the bit error rate is shown in Figure 12. The setup utilized a 31 bit PRN code as a data source and a delay line correlator for comparing only one selected bit per code cycle. As shown in Figure 13, this goal is achieved by selecting one of 31 bits by setting the variable delay corresponding to the time delay of the selected bit. The delayed output (inverted if necessary for proper polarity) is applied along with the correlation output to the two-input “AND” gate. Since code phasing is known precisely at the time of correlation, the signal at the delayed output, i.e., binary “ 1” or binary “0” is also known. If the proper polarity is used at the “AND” gate and no error occurs at the selected bit position, no output will be seen. However, if a bit error occurs at this position in the code, the amplifier output will go positive and trigger the AND gate since the correlation pulse is simultaneously present. Figure 14 shows the bit error output voltage waveform in relation to the correlation waveform when the error amplifier input connection is set to generate zero error and 10076 error condition. The results of a typical test are shown in Figure 7.

Conclusion This paper has presented an analysis of communication systems utilizing multiphase modulation and demodulation. Methods have been derived to generate and coherently detect multiphase signals. The carrier references for the appropriate phase detectors were deduced from considerations of the decision regions for optimal detection.

A unified method was presented for synthesizing cohe-rent demodulators of the multiplier/divider, multiplier loop, analog I-Q loop, and data estimation I-Q loop varieties. This allows a straightforward extension of biphase systems to higher order phase systems.

An X-band 400 Mbits/sec quadriphase system which was built by TRW Systems verifies the analysis and synthesis procedure.

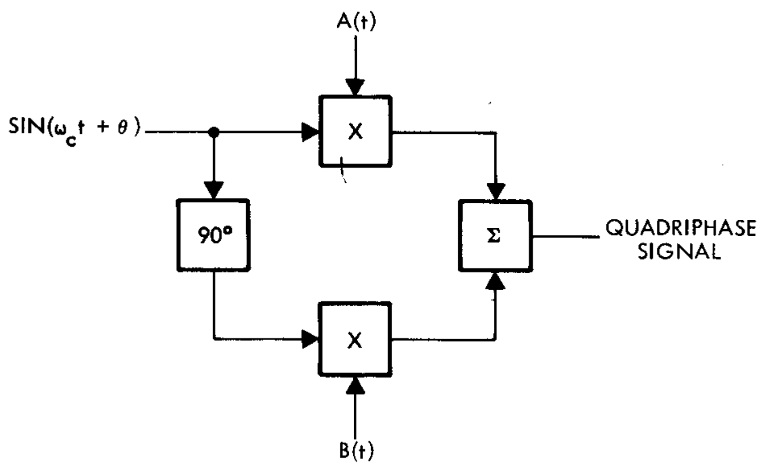
References

1. Arthurs and Dym, “On the Optimum Detection of Digital Signals in the Presence of White Gaussian Noise -- A Geometrical Interpretation and a Study of Three Basic Data Transmission Systems,” IRE Trans. on Comm. Systems, vol. CS-10, no. 4, December 1962.

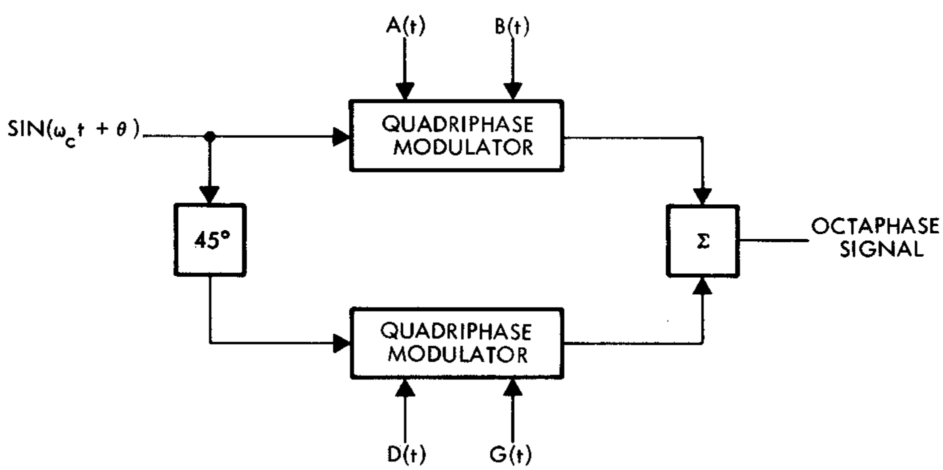
2. C. R. Cahn, "Performance of Digital Phase-Modulation Communication Systems," IRE Trans. on Comm. Systems, vol. CS-7, May 1959.

3. R. V. Garver, "Broadband Binary 180° Diode Phase Modulators," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-13, no. 1, pp. 32-38, January 1965.

4. H. E. Kallmann, "Transversal Filters," Proc. IRE, vol. 28, pp. 302-310, July 1940.



QUADRIPHASE MODULATOR



OCTAPHASE MODULATOR

Figure 1. Generation of Quadriphase and Octaphase

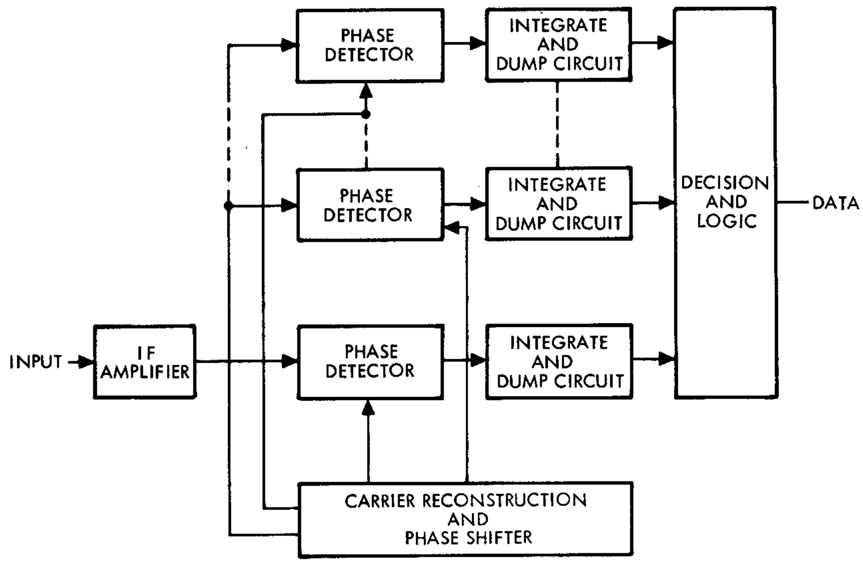


Figure 2. N-Phase Demodulator

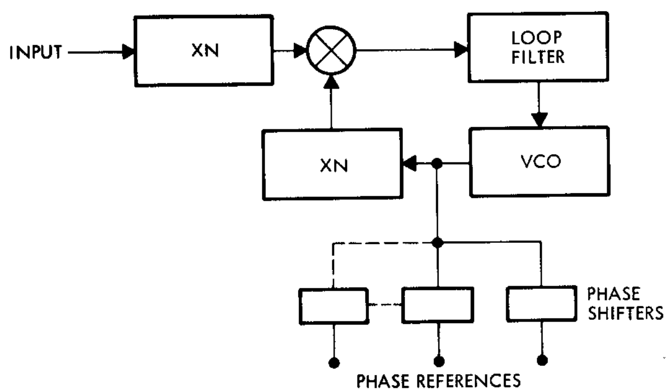


Figure 3. Multiplier Loop for the Generation of the Phase References for N-Phase

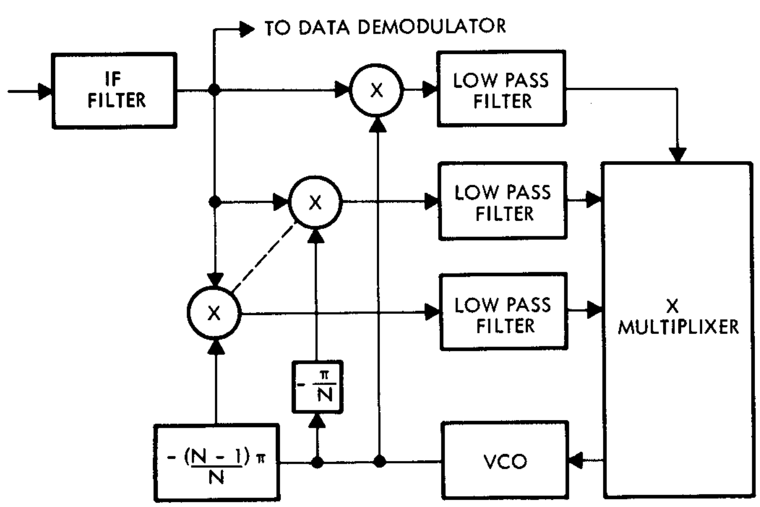


Figure 4. Generalized I-Q Loop for N-Phase

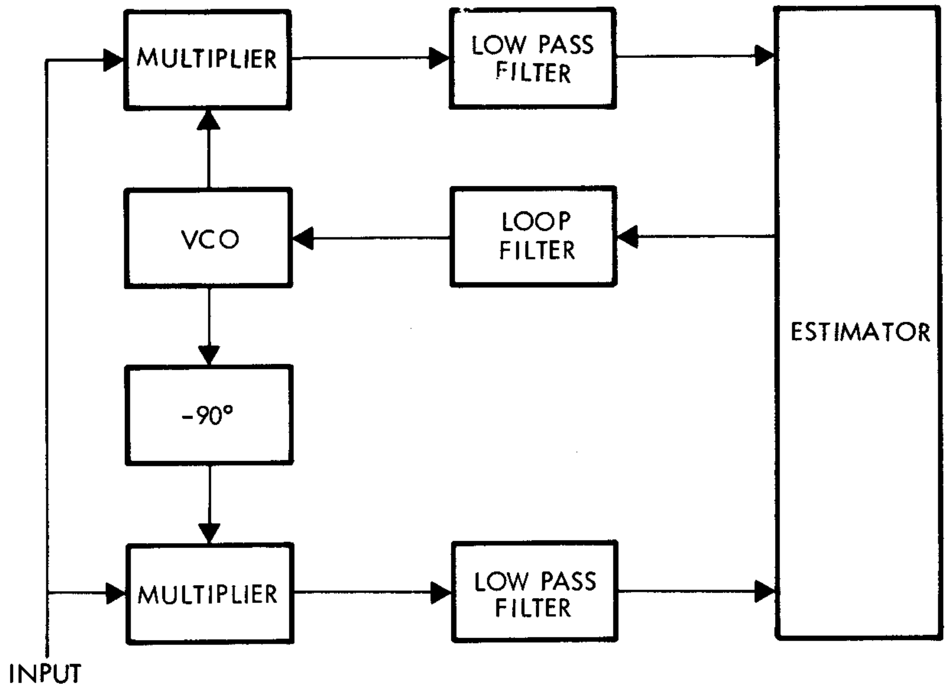


Figure 5. Multiphase Data Estimation I-Q Loop

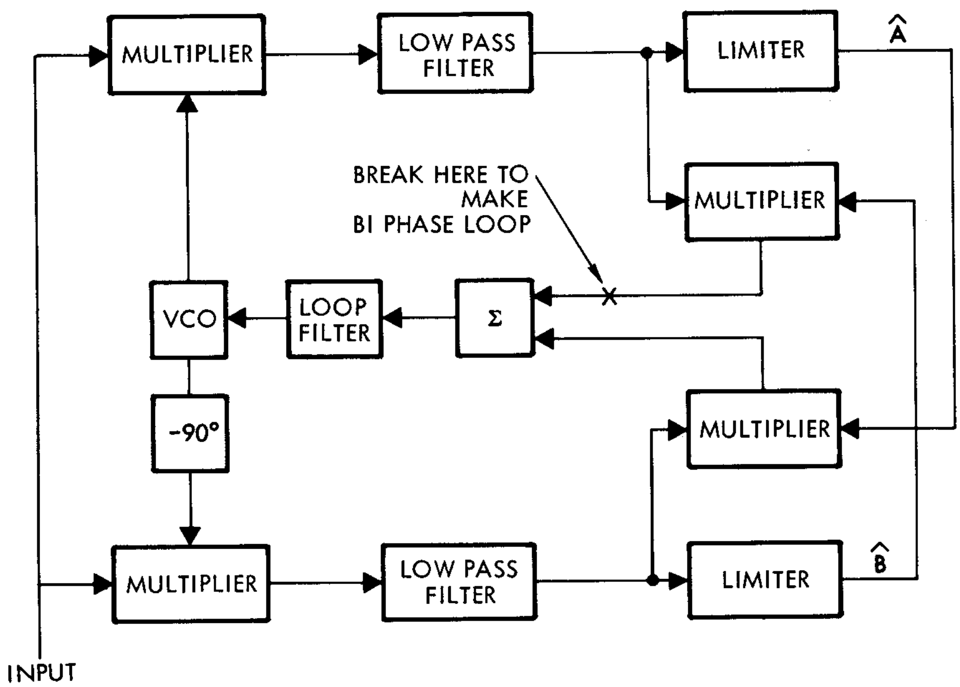


Figure 6. Quadriphase Data Estimation I-Q Loop

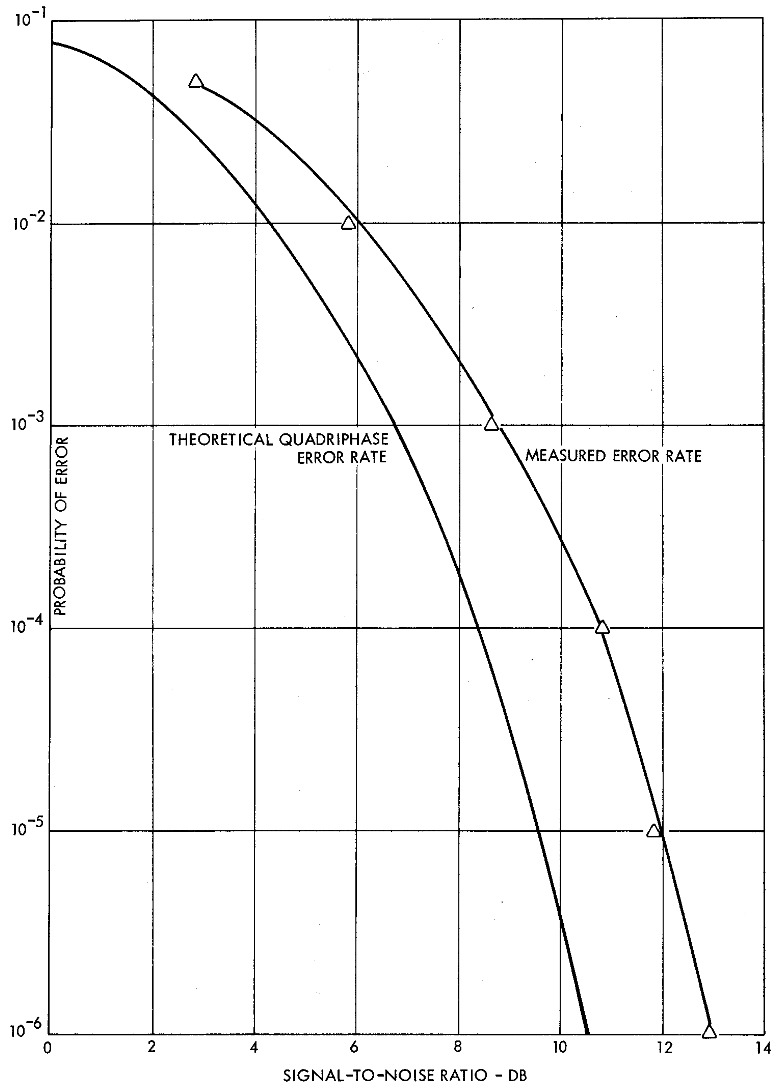


Figure 7. Quadriphase Error Rate

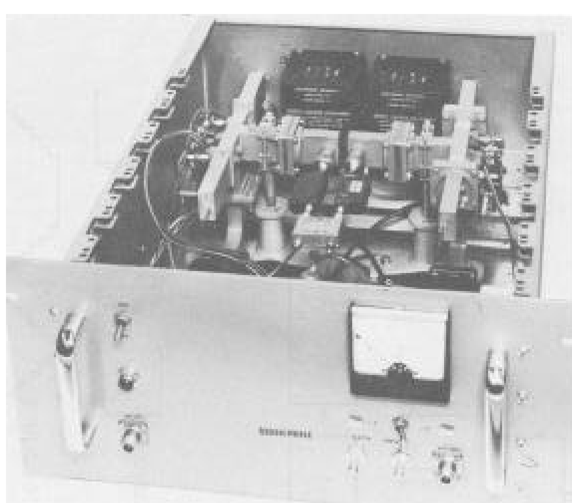


Figure 8. 8.5 Ghz Quadriphase Modulator

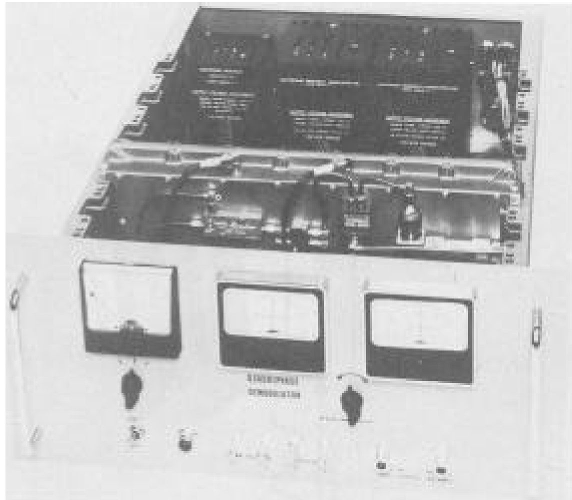


Figure 9. X-Band Quadriphase Demodulator

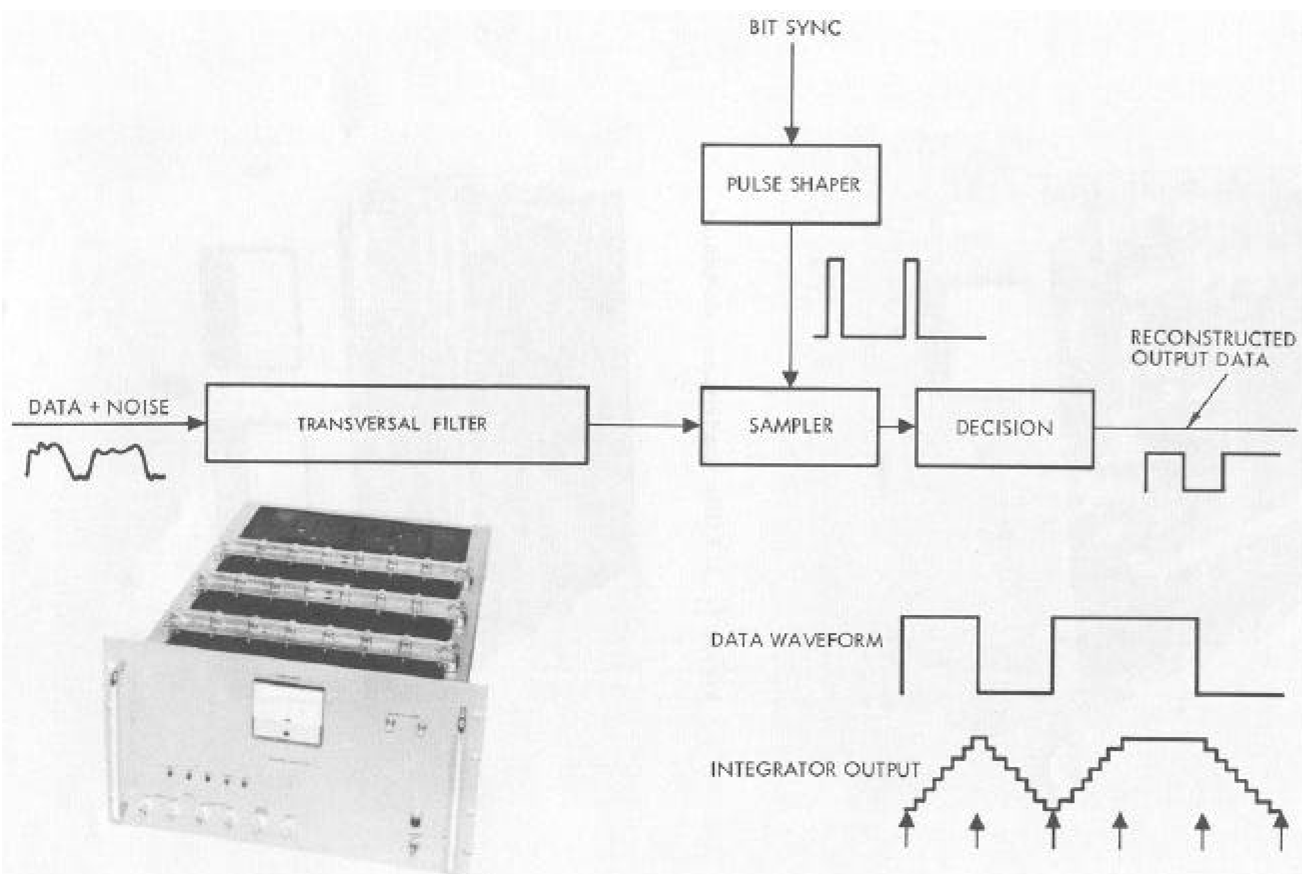


Figure 10. Matched Data Filter

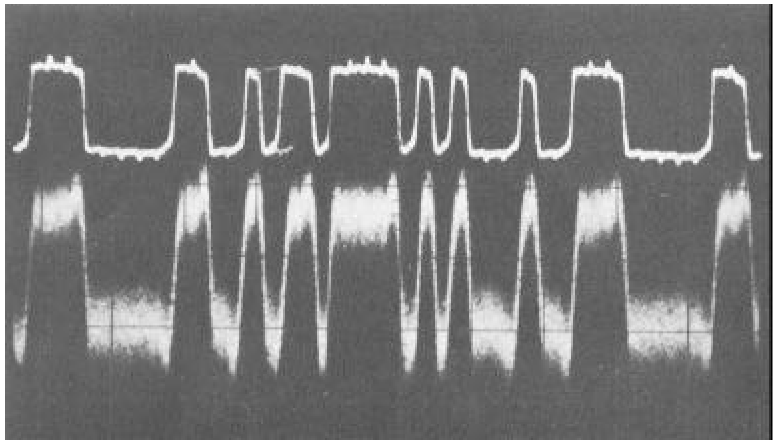


Figure 11. Matched Data Filter Waveforms

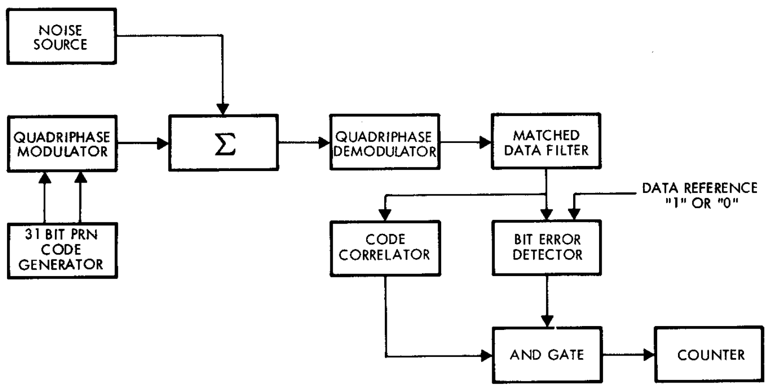


Figure 12. Bit Error Rate Measurement Configuration

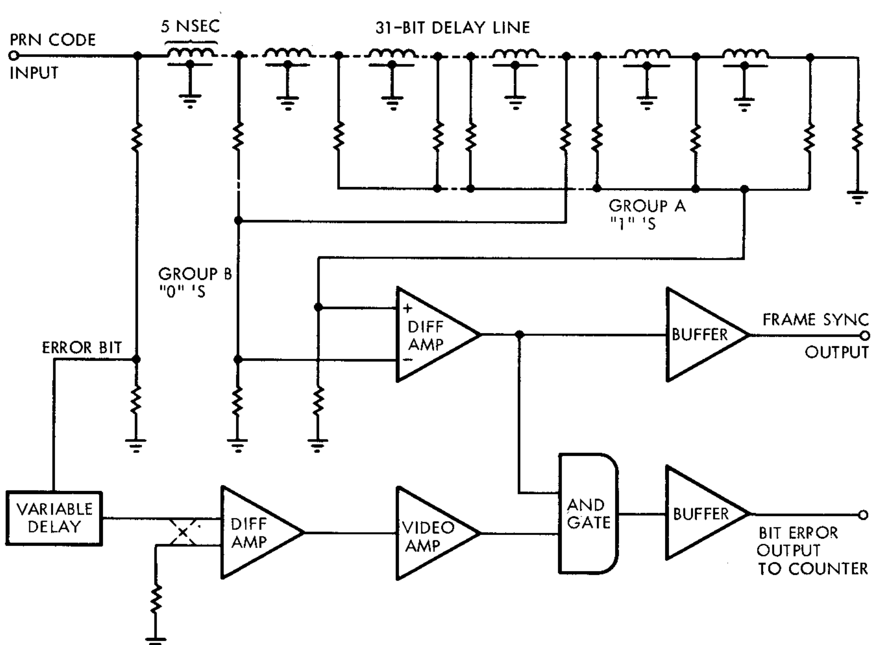
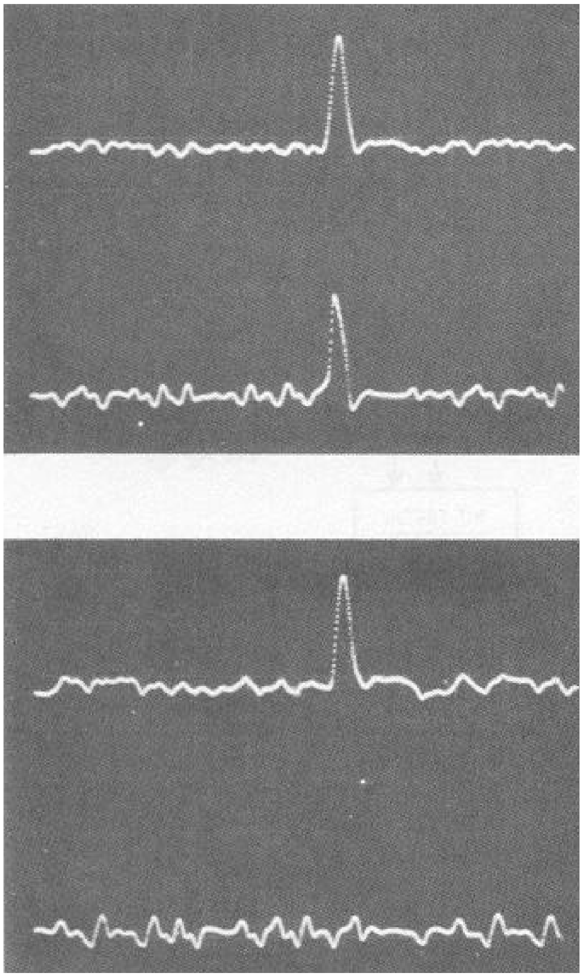


Figure 13. Frame Sync and Bit Error Detector



(a) Frame Sync Output
0.5 v/cm vertically
20 nsec/cm horizontally

No. 31 Bit Error Output (100% errors)
0.2 v/cm vertically
20 nsec/cm horizontally

(b) Frame Sync Output
0.5 v/cm vertically
20 nsec/cm horizontally

No. 31 Bit Error Output (no errors)

0.2 v/cm vertically
20 nsec/cm horizontally

Figure 14. Error Detection Waveform