A COMPLEMENTARY MOS SPACECRAFT DATA HANDLING SYSTEM

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Summary An on-board data handling system for a 1970 earth orbiting spacecraft has been designed and is currently being fabricated using medium scale integration, complementary MOS arrays. This arrangement which interfaces with the spacecraft's cosmic ray experiment will essentially be an engineering experiment. The organization can be divided into several distinct parts: a 512 word by 16 bit memory, a logarithmic data compressor, 5 rate counter/ registers, an address switcher, and a control logic block. The system contains random access 64 bit memory arrays, 8-bit preset counters, and 8-bit parallel load shift registers. The smallest of these arrays contains over 200 active devices. The rest of the scheme is composed of multi-input nand and nor arrays, D type flip-flops, and 7 stage binary ripple counters. Without these MSI arrays the part count would have exceeded 1000, and would require more than one watt of power compared to the complementary arrangement which requires less than 80 milliwatts.

Introduction Complementary MOS has long been recognized as the ideal logic for spacecraft applications because of its low power dissipation, high noise immunity, excellent temperature characteristics, wide operating supply range and reasonable switching speed. However, it has been only recently that logic blocks of sufficient complexity and variety have become available incorporating complementary MOS technology to realistically consider designing spacecraft data systems. Therefore, a small spacecraft scheduled for launch in late 1970 will carry into earth orbit what in all likelihood will be the first complementary MOS data system. This system (Figure 1) which interfaces with the spacecraft's cosmic ray experiment will essentially be an engineering experiment.

Data Handling System

Memory Addressing Logic Whenever the experiment detects a cosmic ray particle, an 8-bit word is presented to the memory addressing logic. The 8-bit word is equivalent to the particle energy value which represents one of 256 energy levels. Thus, a word

signifying that energy level is read from memory into a counter, incremented by one, and placed back into memory at the same address. Each word of memory is actually a software binary counter, counting the number of particles of a given energy level for a fixed period of time. The experiment's ability to detect events is limited to a maximum of one every 100 microseconds. Therefore, the data system will not be accessed at a rate greater than 10 kilohertz.

Rate Counters Associated with the experiment are five 16-bit rate counters. Four of these counters represent gross energy levels, and the fifth counter is used to monitor the experiment's system parameters. Whenever an 8-bit word is presented to the memory address logic, by the experiment, one of these five counters is incremented by one. Periodically 22 words of memory are logarithmically compressed from 16 to 8 bits, and are sent along with data from the five rate counters and an 8-bit address to the spacecraft encoder. This address is monitored so that the value of the first energy level sent from memory will be known.

Each of the five rate counters shown in Figure 1 is composed of two 8-bit binary counter arrays (200 active devices) in cascade and two 8-bit parallel shift register arrays (200 active devices) in cascade with the counter outputs connected to the register parallel inputs. The input rate for any of these counters will be significantly less than 10 kilohertz. Periodically the contents of each counter is transferred to its adjacent register and each counter is reset.

Each register shifts the data at a 400 bit per second rate to the spacecraft encoder. The worse case power dissipation of these five rate counters (10 counter arrays, 10 register arrays) using a +12 volt supply is less than 400 microwatts. (P channel logic for the same application would require more than 10 milliwatts.)

Memory Organization The 8 kilobit memory (Figure 2) organized as 512 words of 16 bits uses IZ8 memory arrays containing 64 bits (400 active devices) of random access NDRO memory. The decoding is X-Y select, and current sensing is the method of read-out using complementary bipolar emitter followers. The address logic is activated by the presence of the read command. The presence or absence of current is then sensed and respectively a one or zero is read out on each of 16 data lines. Without the read command the memory, decoder, and sense amplifiers (a total of 170 arrays) dissipate 0.8 milliwatts, the majority of which is due to bipolar leakage current. The memory can access 500 thousand words a second dissipating 1.6 watts. At worse case the memory in the data system will be accessed at a 20 kilohertz rate and due to the complementary circuitry will dissipate only 64 milliwatts without resorting to power switching.

The memory is divided into two halves of 256 words each. The memory has the ability to be time-shared by both the experiment and the spacecraft encoder. This is performed by

means of a ninth memory address bit that indicates which half of memory is in operation. A priority must be established, and, because the cosmic ray experiment accesses memory more often, it receives the highest priority. The ninth bit flip-flop will always point to the half of memory that the experiment is using. When the spacecraft encoder needs a word from memory, the experiment is inhibited, and the ninth bit is changed to point to the other half of memory. As soon as this word has been fetched, the inhibit is lifted, and the ninth bit is reset to point to the experiment's address again.

Data from the memory is either loaded into a 16 bit binary counter to be incremented by one or is loaded into a 16-bit register to be shifted to the logarithmic compressor. The counter and register arrays previously mentioned are used for these functions and will dissipate no more than 80 microwatts. If all 256 words have been read out of memory, the ninth bit is switched so that both the experiment and the spacecraft encoder can continue to use opposite halves of memory. Prior to this, at the time of read out, zeros are substituted into the memory so that no erroneous count will be left in memory for the experiment to misuse.

Logarithmic Data Compressor The logarithmic data compressor,[1] as a subsystem (Figure 3) dissipates only 40 microwatts because of its low duty cycle. It must compress 22 words from memory every second and shift the compressed data to the spacecraft encoder at a 400 bit-per- second rate. A 16 bit word is compressed to 8 bits; bits 1 through 4 indicate an exponent and bits 5 to 8 indicate the 2nd, 3rd, 4th, and 5th MSB of the original word. A word fetched from memory is loaded into a 16 bit parallel load shift register and is shifted into a 5 bit shift register. The word is shifted until a I enters the most significant stage of the 5 bit register. This enacts the control to stop shifting the rest of the word into the 5 bit register. However, the remaining shift pulses are counted by a 4 bit counter. The 2nd, 3rd, 4th, and 5th MSB's of the word plus a 4 bit binary representation of the exponent is loaded into an 8 bit parallel load shift register which is then sent to the spacecraft encoder. The most significant bit is not sent since it is known to be a one.

Part Count The total part count of the system is 265 arrays; 178 of these are MSI arrays, namely 64-bit memory arrays[2] (Figure 4A), 8-bit preset binary counters[3] (Figure 4B), and 8-bit parallel load shift registers (Figure 4C). The remaining arrays consist of multi-input nand and nor arrays, D type flip-flops and 7 stage binary ripple counters.

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[1] Schaefer, D. H., "Logarithmic Compression of Binary Numbers," Proceedings of the IRE, Vol. 49, No. 7, July, 1961.

[2] Work on the 64-bit memory array is being performed by RCA.

[3] Work on the 8-bit counters and shift registers is being performed by Solid State Scientific Corporation.

Without the MSI arrays the part count would have exceeded 1000. A system built with either P channel and bipolar technology, even assuming a core memory, would require more than one watt compared to the complementary system which requires less than 80 milliwatts.

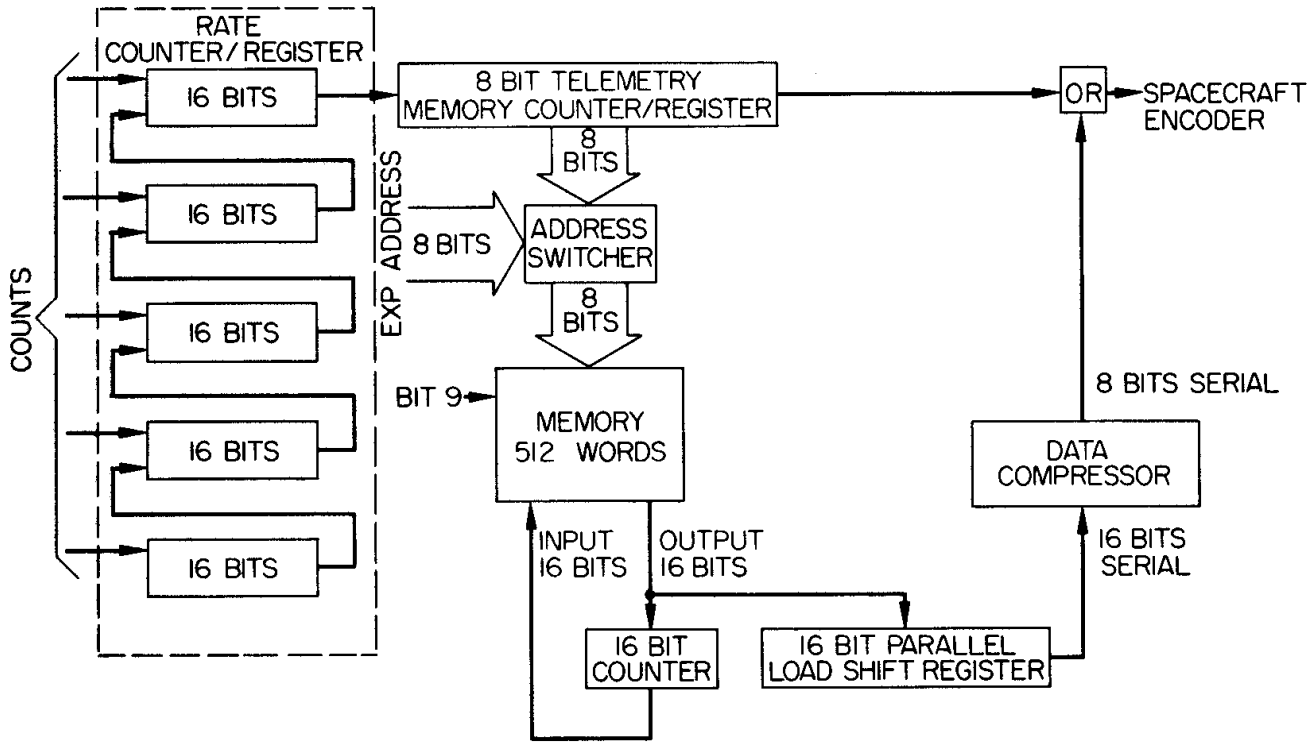

Fig. 1 - Spacecraft Data Handling System.

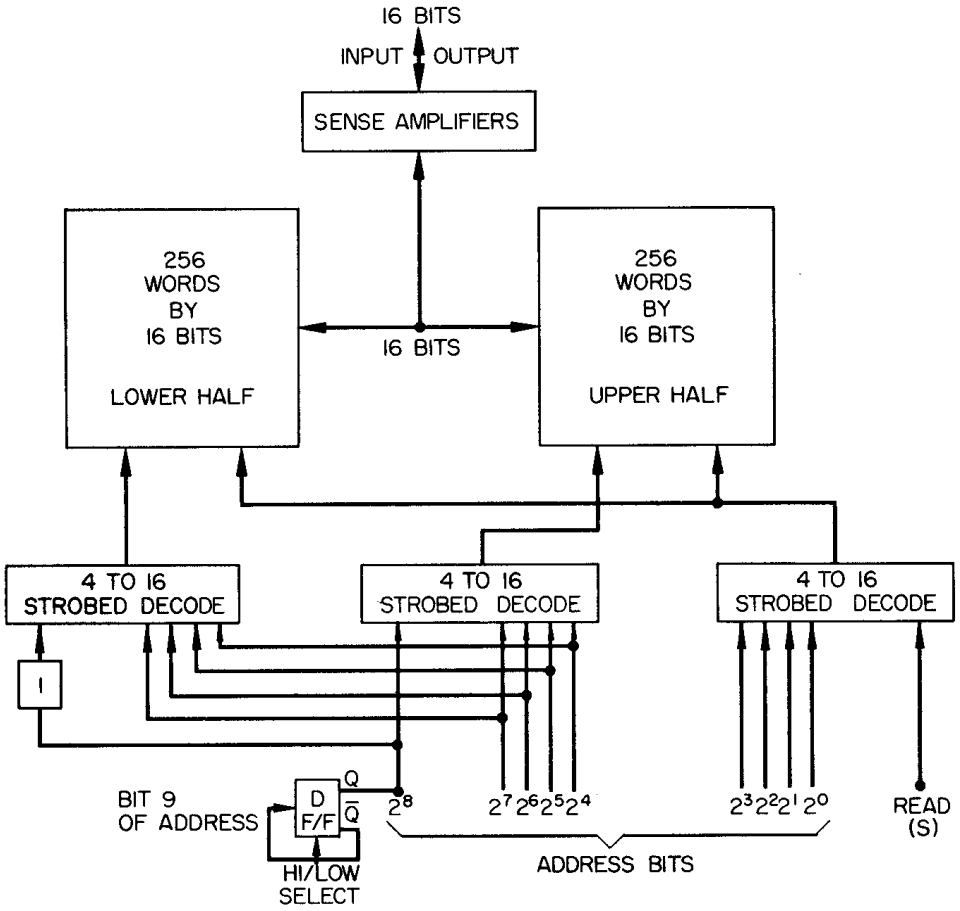

Fig. 2 - Memory Organization.

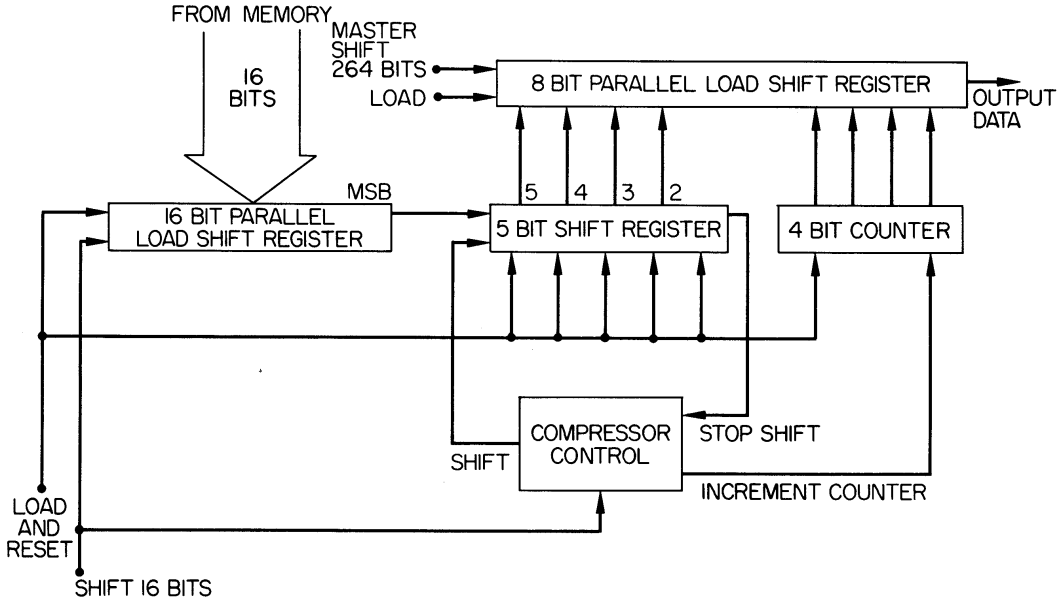

Fig. 3 - Data Compressor.

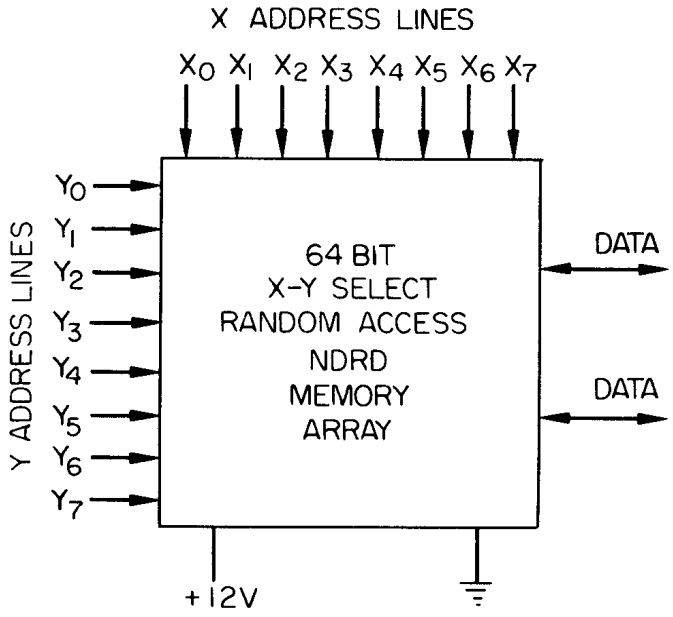

Fig. 4a - 64 Bit Memory Array.

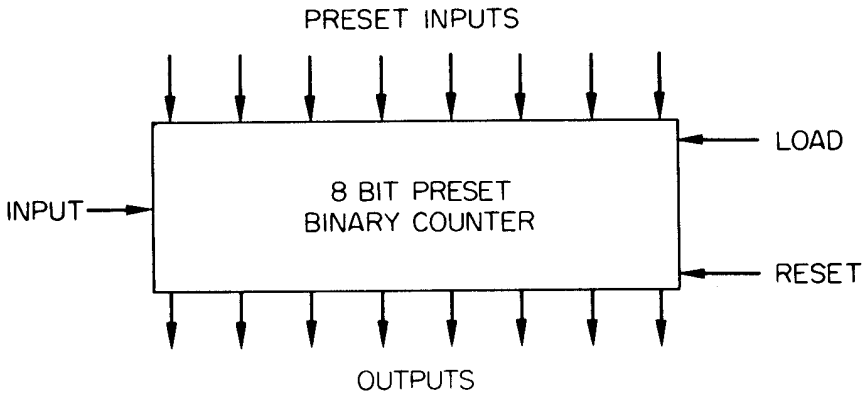

Fig. 4b - 8 Bit Preset Binary Counter.

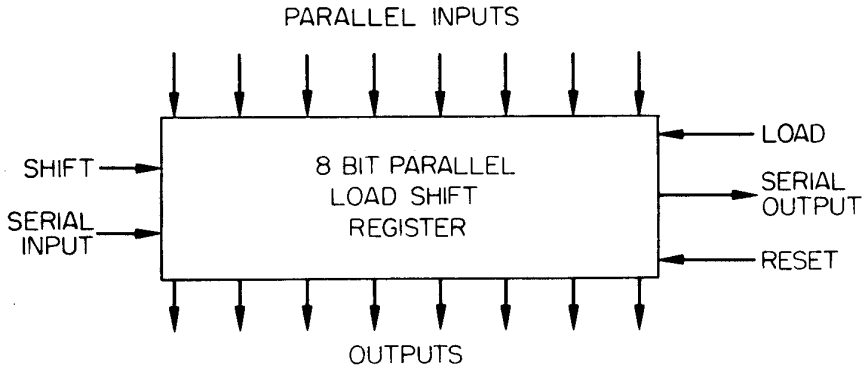

Fig. 4c - 8 Bit Parallel Load Shift Register.