A FLEXIBLE FORMAT ADAPTIVE TELEMETRY ENCODER

RICHARD S. COOPERMAN
COMSAT Laboratories
Communications Satellite Corporation
Washington, D. C. 20006

Summary The Communications Satellite Corporation is developing the systems design and implementation techniques for a flexible format adaptive telemetry encoder. The encoder design includes wired program options to tailor system capability to mission requirements. on-board data source controlled interrupt of the normal telemetry format for transmission of preprocessed or block accumulated information automatically adapts the telemetry channel to variable data rate sources. Ground command control format modifications provide increased data rate or continuous burst readout of selected data inputs. Distributed commutation is also available for the remote collection of analog and digital data. Extensive use is made of monolithic MSI MOS devices and custom hybrid bi-polar logic arrays in the instrumentation of the encoder.

Introduction The performance capability of the INTELSAT series of communications satellites has advanced significantly since the development of Early Bird. This improvement in communications performance has required an increase both in satellite size and complexity. With this growth has come the need for greater parameter readout accuracy, greater parameter information bandwidth and a greater total number of satellite performance parameters to be monitored. Up to the present time all INTELSAT satellites have employed PAM/FM/FM telemeters to obtain housekeeping data. With the more complex INTELSAT IV satellite series presently under development, a changeover to a PCM telemetry system will take place. In order to more efficiently fulfill the telemetry requirements of future satellites, COMSAT has initiated the in-house design of a flexible format adaptive PCM telemetry encoder capable of being easily tailored to fit the instrumentation requirements of future satellites. The encoder system design and implementation provide the capability of being tailored for an operational satellite or an experimental satellite. All major telemetry system parameters such as bit rate, word length, frame/sub-frame length, number of channels, digital/analog input grouping may be changed simply by exercising hardware wiring options. The capability of handling blocks of serial digital data under either command or remote demand priority interrupt control is provided. Provision is also made for command control super-commutation of a selected sub-frame.

The extreme long-term reliability requirements of COMSAT satellites will be met through system redundancy and extensive use of high reliability screened MSI circuits and hybrid multichip arrays. The system wiring will be minimized through the use of ultra-low power logic elements packaged in multichip array hybrids and standard MSI analog integrated circuits. Whole registers, counters, A/D converters, eight channel commutators, etc., will be contained in a single hybrid or monolithic circuit. Interconnections between circuits will be accomplished by high reliability multilayer printed circuit boards. Also, extensive satellite harness wiring for remote sensors will be eliminated by the use of distributed analog/digital signal commutation.

System Performance The telemetry encoder (Figure 1) is designed to handle the needs of both large and small operational communications satellites and the requirements of advanced experimental satellites. The capability of handling auxiliary experimental data collection unit information onboard an operational satellite is also provided. The system design and modular instrumentation is such that the encoder may be simply configured to satellite system requirements through the use of minor wiring options. The performance envelope within which the system capabilities may be set and the performance parameters selected for a developmental model are set forth in Table I.

Table I
SYSTEM PERFORMANCE PARAMETERS

	Developmental Model	Maximum
Bit Rate (BPS)	1024	10,240
Word Length (Bits)	8	10
Words per Sub-frame (Words)	24	32
Sub-frames per Frame (Sub-frame)	8	32
Sub-frame Sync (Words)	1	1
Frame Sync (Words)	2	2
Sub-frame Identification (Wordsl	1	1
Channels - Digital	32	256
Analog	160	786
Interrupt Inputs	4	8
Command Data Inputs	4	8

The telemetry encoder operation, once the performance parameters are established and wired in, is subject to modification by remote data collection units or by command control. Signals at the data interrupt inputs override the normal fixed data format and allow processing of the interrupting data source on a pre-established priority basis. The data interrupt blocks are pre-wired to be handled as serial bursts of up to twenty words,

in four word units. Command control of the telemeter overrides individual or all interrupt inputs, as well as causing dwell and repeat of a particular sub-frame. Ground command control also has the capability of burst readout of selected data accumulators via the telemetry link.

Input Data Commutator The input data commutator is the telemetry encoder interface for all input signals handled in the pre-wired fixed format. This unit accepts information from individual sensors, distributed remote sub-multiplexers and digital data registers. The input signals are sequentially addressed and transmitted through a two tiered MOS commutator prior to being processed in the telemetry encoder. The commutator handles low level analog, high level analog and bi-level digital signals.

Since the commutator configuration in a large capacity telemeter has a major impact upon spacecraft instrumentation, much effort has gone into developing an efficient design. A review of present communication satellite designs has shown that a significant portion of the structural weight is taken up by harness cabling arrays and that a major contributor to the harness is telemetry sensor wiring. The problems and weight penalties of routing large numbers of cables for telemetry sensors are all too familiar to anyone involved in satellite subsystem design. The availability of high-reliability MSI and hybrid array commutator elements now allows the telemetry engineer to distribute or decentralize his commutator interface strategically about the satellite. This is accomplished by physically transferring groups of commutator switches in the first tier of the two tiered commutator from the telemetry subsystem box to other locations in the satellite. A complete thirty-two channel remotely located commutator (Figure 2) is instrumented with four MSI analog switch ICs, one multichip hybrid logic array IC for control and one analog IC as an output buffer. The counter and logic contained in the multichip array can be programmed for fewer than 32 channels, in increments of eight, through simple external wiring changes. Thus the thirty-two harness wires required by a thirty-two channel centralized commutator have been reduced to just four wires through the use of a remotely located sub-multiplexer. The sub-multiplexer address counter operates under the direct control of the main telemetry unit word clock and master sub-frame reset signals. The sub-multiplexer PAM output signal is handled at the main telemetry unit as a second tier input signal and its information is processed along with the other telemetry signals.

The two tiered commutator is addressed as an RxCxS three dimensional matrix. The row and column digital data select one switch in each first tier array, while the sub-frame data makes the final selection of a single channel. A two tiered commutator was chosen as a best compromise between leakage current offsets and ON resistance effects. The three dimensional addressing coupled with the built-in decoder/driver within the eight channel MOS ICs makes for extremely efficient logic design. It should also be noted that the MOS switch IC control signal logic levels are compatible with those normally found in

low power digital integrated circuits, and that no complex switch driver circuits are required.

Fixed Format Digital Data Information from fixed data rate sources and normal housekeeping status data is processed in a conventional manner during each telemetry frame, The selected format to meet mission data requirements is established through fixed hard wired options. As with the commutator design, the circuitry to collect and transfer the fixed format digital data is designed for minimum impact on spacecraft harness wiring.

The digital housekeeping data such as mode or relay status indicator bits and other fixed data rate digital information generally are collected at remotely located distributed storage registers and serially transferred to the telemetry encoder as digital TM words. Some housekeeping data are collected in parallel at the telemetry encoder itself, if the source is located close by or if insufficient data volume exists to warrant the use of remotely located storage registers. Each storage register is addressed by the telemetry encoder via two wires and serially outputs its data once per frame. The register contents are then cleared and prepared to accept new status data.

Where sufficient digital data volume exists in a localized area or sub-system the storage register will be remotely located so as to more efficiently collect the data. An entire 10 bit status register, along with its address and control logic, is completely contained in a single MSI multichip hybrid logic array. Remotely located digital storage registers located with a distributed commutator unit require only three control signals for the first register and one more signal for each additional register. Each separately located digital storage register requires only four signal connections to the telemetry unit. The control signals consist of register address and bit clock information. Provision is made for selection of up to 8, in blocks of 2, fixed digital words per sub-frame.

Variable Rate Digital Data The telemetry encoder has the capability of adapting its processing program to accept bursts of preprocessed data or information from variable rate sources. This data could be from a scientific instrument compiling statistics over a long period of time, or one which gathers its information in burst-like blocks of data. The efficient handling of non-conventional data inputs is best accomplished by making the telemetry format variable. This is achieved in two ways: first, by automatically adapting the data format to information source requirements through a priority interrupt capability; second, by varying the data format through ground command control delegation of the telemetry encoder for block data readouts.

The priority interrupt capability is instrumented in the telemetry encoder by the inclusion of logic circuitry to recognize, store and priority-rank interrupt control signals from remotely located sub-systems. The interrupt storage register contents are examined for a

stored signal at the end of each telemetry sub-frame and acted upon, in pre-wired priority order, in the next sub-frame. A telemetry sub-frame with interrupt data in it consists of the normal fixed digital words, including the synchronization word and an identification word tagging the interrupt data input, and from four to twentyeight words as the output of the interrupting data source. Each interrupt source is allocated a pre-wired four to twentyeight word block in four-word increments. Words in the subframe not required by the interrupt source contain the normal fixed format telemetry data. At the completion of the sub-frame an interrupt-complete signal is generated to terminate the interrupt operation. A maximum of up to eight interrupt input channels are provided, as well as ground command override capability for each interrupt channel.

Burst transmission of large blocks of preprocessed data from a remote sub-system can be accomplished via ground command control. This mode is suitable for data sources where the accumulation rates are not compatible with the standard telemetry format, yet not of sufficient importance or urgency to warrant an interrupt channel. Ground commanded data readouts are initiated at the start of the next telemetry sub-frame after receipt of a command execute. The capability of command selection of up to eight data inputs is provided. The ground command controlled data readout will almost completely delegate the telemetry encoder output to the selected data source. The only exception made is the inclusion of the normal fixed format digital words in the data stream. Priority data handling operations are suspended for the duration of the commanded data readout, and normal system operation is resumed only upon receipt of a command controlled data readout terminate command from the ground control station.

Analog to Digital Converter The PAM analog signal output of the commutator is converted into a digital word by a 10 bit analog-to-digital converter employing the successive approximation technique. Recent advances in 140S integrated circuit technology have made it possible to reliably integrate the digital logic and analog switch portions of a 10 bit binary A/D converter on a single monolithic chip. The external circuitry required to complete the A/D converter consists of a precision passive resistive ladder network a differential comparator, and a few logic level converters.

The telemetry encoder A/D converter is instrumented around a Fairchild type 3751 MOS-LSI A/D converter circuit. This unit contains on one chip the timing register, holding register, control logic, synchronization logic and analog switches necessary to perform a 10 bit successive approximation binary conversion. The ladder network is a precision standard R - 2R binary weighted hybrid network which converts the reference voltage and MOS switch status into a proportional analog voltage. The differential comparator receives the analog input and ladder output signals, and determines whether the ladder voltage exceeds the analog input. The comparator output signal is level converted and used to control the A/D conversion.

In system operation the A/D converter analog input signal is the PAM data from the commutator, with a conversion initiated at each channel step of the commutator. The A/D conversion clock rate is 100 kHz so that a complete conversion is made in 100 μsec. Since the anticipated channel rate is 100/sec the aperture is then one-hundredth of the channel dwell time. The A/D converter data output is provided serially during the conversion and is merged in the output buffer with the other encoder data signals.

Channel Address Logic The channel address logic provides all the signals required to sequentially address the fixed format data channels. Operating upon the word clock and control unit mode information, the address counters provide first and second tier commutator address signals. The row and column counter provides first tier address and a clock signal for the sub-frame counter, while the sub-frame counter provides the second tier address, and the frame complete signals.

The word clock is counted down in a five bit variable modulo counter to provide row and column address for 16, 24 or 32 channels per sub-frame. Selection of the number of channels per sub-frame is accomplished through simple wiring options external to the counter hybrid IC. Distributed commutator elements will each contain a row and column counter unit, with central control achieved through common clock and reset signals from the main counter. The five bit variable modulo sub-frame counter is incremented by the carry or sub-frame complete signal from the row and column counter. As before, simple wiring options external to the counter hybrid IC are used to determine the number of sub-frames per frame. A maximum capability of 32 subframes per frame is provided for in the counter.

The address data from the word and sub-frame counters are continuously applied to the commutator switch decoders. The two tier switch array is organized in row and column sub-frame blocks in the first tier and by sub-frame in the second tier. Thus the word counter row-and-column address selects one switch in each first tier sub-frame array for connection to the second tier. The sub-frame counter address then completes the selection of a single channel by enabling only one second tier switch.

Word and sub-frame counter data also is made to address the standard digital housekeeping data storage registers, synchronization words and data identification words. The first four to eight words of each sub-frame are dedicated to digital data by hard wired logic options. The first two channels of each sub-frame are reserved for synchronization and data identification words. The rest of the digital data channels are used for handling spacecraft data.

Clock Generator The clock generator provides a stable central time reference for all telemetry encoder operations. The basic reference element is a temperature compensated crystal oscillator operating at 1.024 MHz. The oscillator squarewave output is digitally

divided in a series of binary counters and linear shift-register dividers to provide all clock signals required within the telemetry encoder.

The 1.024 MHz oscillator signal is divided down to provide a two-phase bit clock, word clock, A/D converter clock and telemetry subcarrier. Division is performed either with synchronous counters for binary division or with linear shift-registers for non-binary division. The use of linear shift-registers for non-binary division allows the designer to employ standard building block shift-registers and add only a feedback logic circuit.

The word clock is generated by dividing down the bit clock in a four bit linear shift-register divider by the number of bits per word. The shift-register feedback logic is configured so that the pattern generated is also the optimum synchronization word for the selected word length. Thus this register performs as both a divider and aynchronization word generator. The feedback logic is designed so that simple logic inputs select between a division ratio of 8, 9 or 10 to 1, and also provides the proper length synchronization code word.

Conclusions The system design and implementation techniques described in this paper show that a flexible adaptive telemetry encoder is feasible. Implementation with modular units allows for maximum system flexibility by not requiring significant design effort to reconfigure the system. The inclusion of data controlled adaptive format capability greatly improves data handling efficiency with a minor increase in system complexity. The use of hybrid arrays and complex monolithic circuits increases system reliability and reduces the number of interconnections.

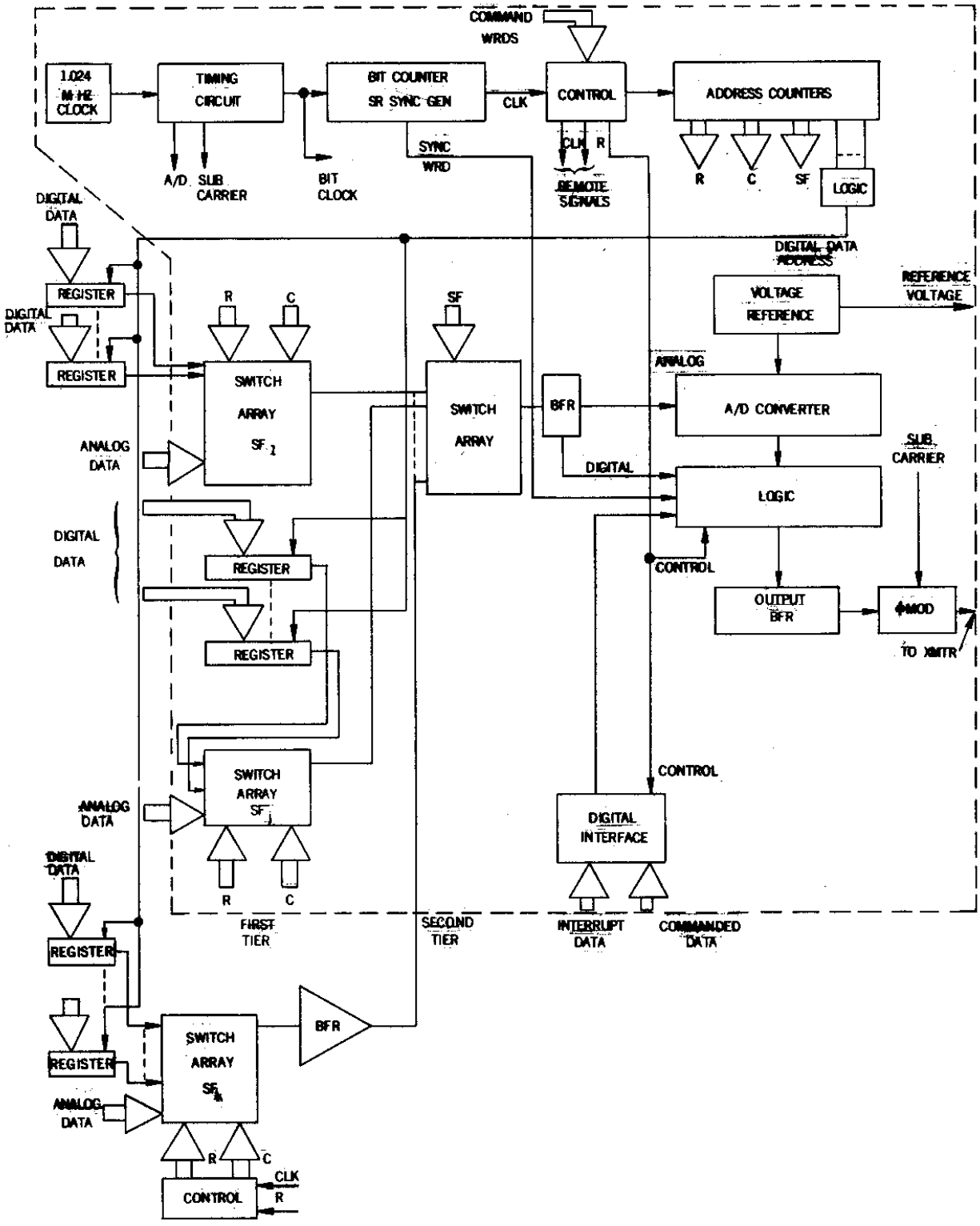

FIGURE 1 TELEMETRY ENCODER SYSTEM BLOCK DIAGRAM

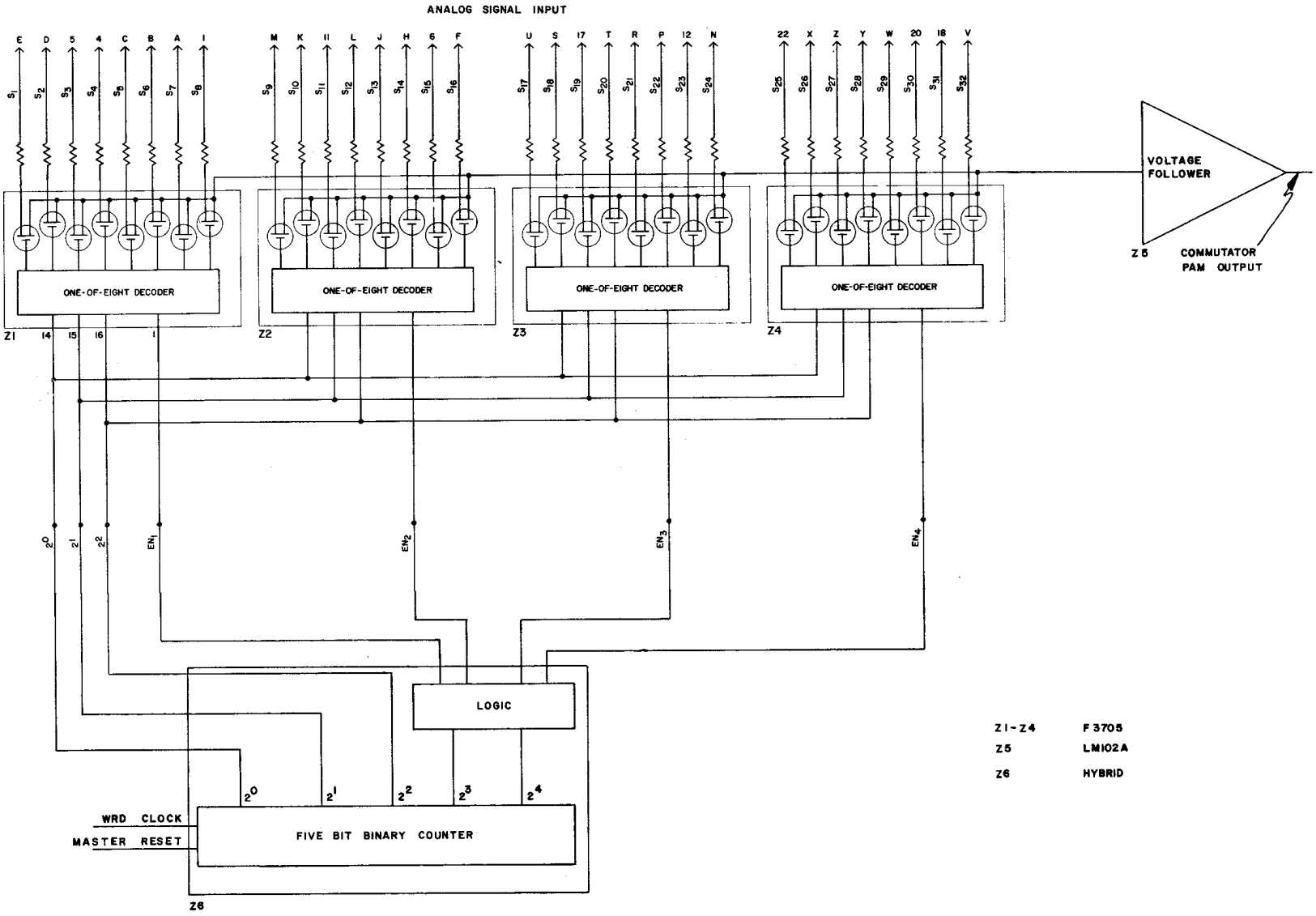

FIGURE 2. THIRTY-TWO CHANNEL REMOTE COMMUTATOR