DIGITAL RECEIVER PERFORMANCE

Robert C. Troublefield
NAWCWD, China Lake, CA

ABSTRACT

Bit errors often occur in a wireless communications link when impairments alter the transmitted signal. It is advantageous to be able to predict how well a system will tolerate transmission problems. This paper details laboratory performance measurements and comparisons in terms of evaluating configurations of a digital receiver for Feher patented Quadrature Phase Shift Keying (FQPSK-B) demodulation. The transmitted signal is subjected to calibrated levels of impairments while the receiver performance is monitored in real-time.

KEYWORDS

Feher patented Quadrature Phase Shift Keying (FQPSK-B) [3], bit error rate (BER) vs. signal energy per bit to noise power spectral density (E_b/N_0), flat fading, multipath fading, critical notch depth, adjacent channel interference (ACI), acquisition time, fade recovery time

INTRODUCTION

The wireless channel is the transmission medium that introduces effects such as attenuation, interference, noise, and distortion. Random noise, flat fading, multipath fading, and adjacent channel interference are dominant sources of distortion in the aeronautical telemetry channel. A fading channel is indicated by the transmission characteristics varying with time. Time variations in the channel structure arise due to random changes in the propagation characteristics of the medium. In contrast, adjacent channel interference (ACI) is the result of unwanted signals from other frequency bands spilling over into the channel of interest. The end results are periods of high bit error rates and periods of low bit error rates at the receiver.

This paper will provide insights to the performance levels of a digital receiver when demodulating FQPSK-B in the laboratory. Bit error performance, multipath fading, adjacent channel interference, as well as acquisition time and fade recovery time will be measured and compared to the Advanced Range Telemetry (ARTM) performance specifications on FQPSK-B demodulators [2].

DIGITAL RECEIVER DESCRIPTION

A completely digital receiver has been assembled and tested for performance measurements as shown in Figure 1. The receiving system consists of three printed circuit boards. Two boards are commercial-off-the-shelf items from Intersil, formerly Harris Semiconductor. The third board is an in-house designed interface card.

The Intersil HI5703 is a single board evaluation card to test a high performance analog-to-digital converter (ADC) [9]. The board contains the ADC, clock driver circuitry, analog input drive circuitry, voltage reference generator, and buffered data outputs. The ADC is a monolithic flash, 10-bit output, 40 megahertz (MHz) sample rate, and 250 MHz bandwidth device.

The Intersil HSP50110/210 is a single board evaluation kit for phase shift keying (PSK) communication systems [6]. It is designed as a drop in prototype for PSK demodulators in digitized intermediate frequency (IF) applications. The board contains three main programmable components consisting of a digital quadrature tuner (DQT), a digital Costas loop (DCL), and a digital filtering section. The quadrature tuner provides carrier local oscillator generation and mixing, low-pass filtering, and baseband re-sampling [7]. The digital Costas loop provides for carrier tracking and symbol synchronization [8]. Finally, the finite impulse response (FIR) serial digital filters provide for matched filtering of the baseband data.

The custom receiver interface board contains a programmable logic device (PLD), a phase-lock-loop (PLL), and a dual digital-to-analog converter (DAC) with filtering. The programmable logic device contains circuitry for symbol-to-bit conversion, differential decoding, and selectable derandomization.

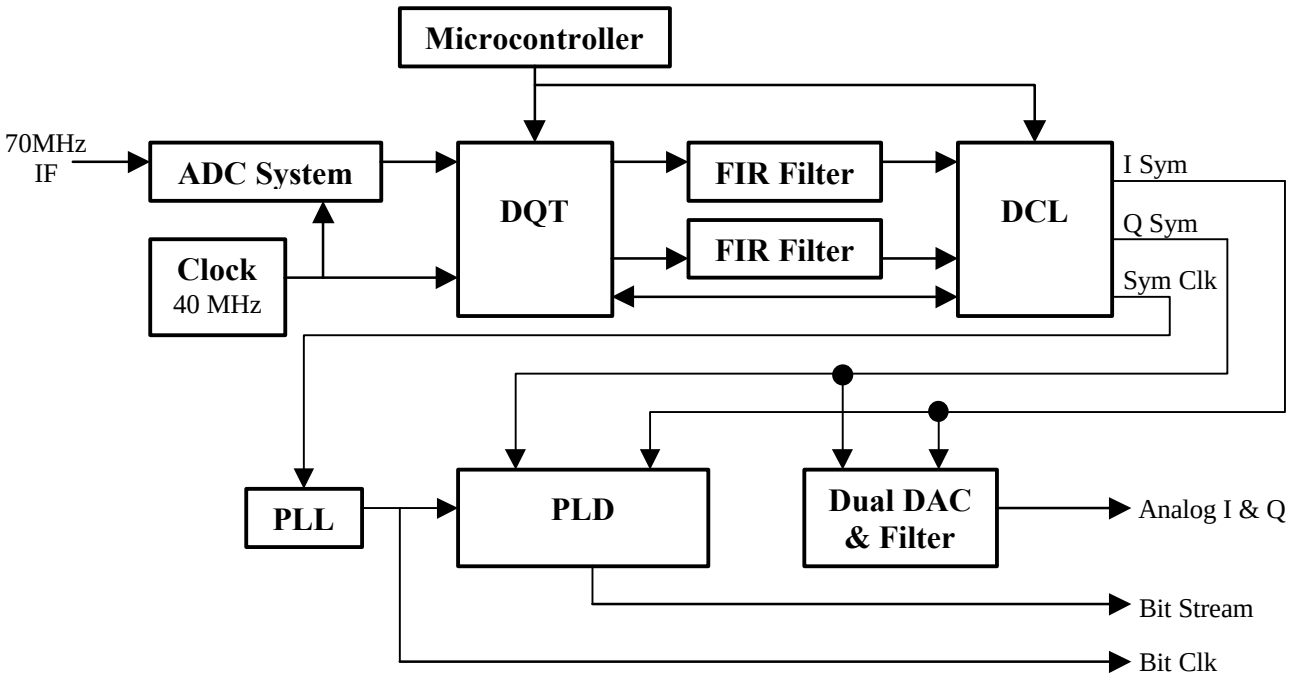

Figure 1. Digital receiver system.

The phase-lock-loop provides for bit clock generation from the symbol clock out of the Costas loop. The dual DAC outputs in-phase (I) and quadrature (Q) symbols. This interface board addition allows end-to-end testing, debug, and optimization of the digital receiving system.

DIGITAL RECEIVER OPERATION

The DQT and DCL register values are shown in the Appendix. Specific items that were altered for performance tests are discussed below.

This receiver is operating on hard-decision, single symbol detection. Soft-decision 3-bit outputs are available from the slicer for other applications. Demodulation mode is set to Offset Quadrature Phase Shift Keying (OQPSK).

Table 1 shows carrier loop bandwidths and symbol loop bandwidths selected for tracking mode, expressed in percentage of symbol rate. The acquisition mode loop bandwidths are set to 3 times the corresponding tracking mode loop bandwidth. The carrier tracking range is set at 100 kilohertz (KHz) to satisfy the performance specification [2]. Any narrower carrier loop bandwidths would not track the full range of carrier frequency offset limits.

	Carrier Loop Bandwidth	**Symbol Loop Bandwidth**
Narrow	0.08%	0.1%
Medium	0.5%	0.2%
Wide	1.0%	0.3%

Table 1. Loop bandwidth parameters.

The symbol tracking loop locks independently and under most circumstances will lock before the carrier tracking loop. The symbol tracking loop detector generates a sampling error based upon a measure of how far the mid-symbol sample is from the symbol transition midpoint, see Figure 2 [8]. The programmable carrier lock circuit detection is based upon an automatic search, verify, and lock state transition. The function of the lock detector is to monitor the baseband symbols and to decide whether the carrier tracking loop is locked to the input signal. Based on the in-lock or out-of-lock decision, either the acquisition or tracking parameters are selected for the loops. A phase error, θ_E, is generated for each symbol, see Figure 3 [8]. The lock detector monitors the outputs of the phase error accumulator to determine the search, verify, or lock state, see Figure 4 [8]. The accumulation process averages or integrates the phase error to reduce variance. The integration time can be programmed up to 1025 symbol periods. The carrier loop is in the lock state if the integration counter finishes before the phase error accumulator overflows. The verify state cycles through a programmable number of in-lock conditions before transitioning to lock. The initial search state is where the carrier frequency uncertainty is swept while acquisition parameters are active. The acquisition sweep rate parameter is the amount the carrier lag accumulator is incremented or decremented to produce a frequency correction value each time the loop filter runs. The false lock detection is not utilized since it is designed to operate on square wave data, not shaped waveforms such as FQPSK-B.

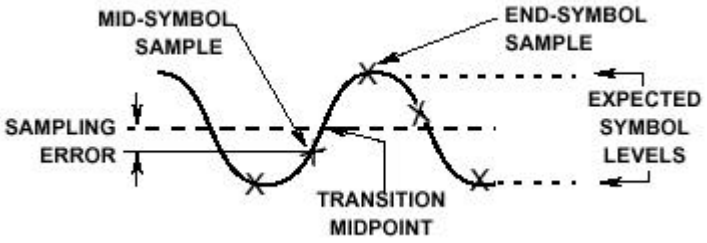

Figure 2. Symbol error detector.

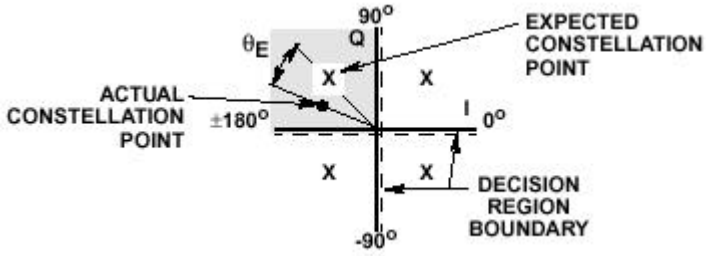

Figure 3. Carrier phase error detector.

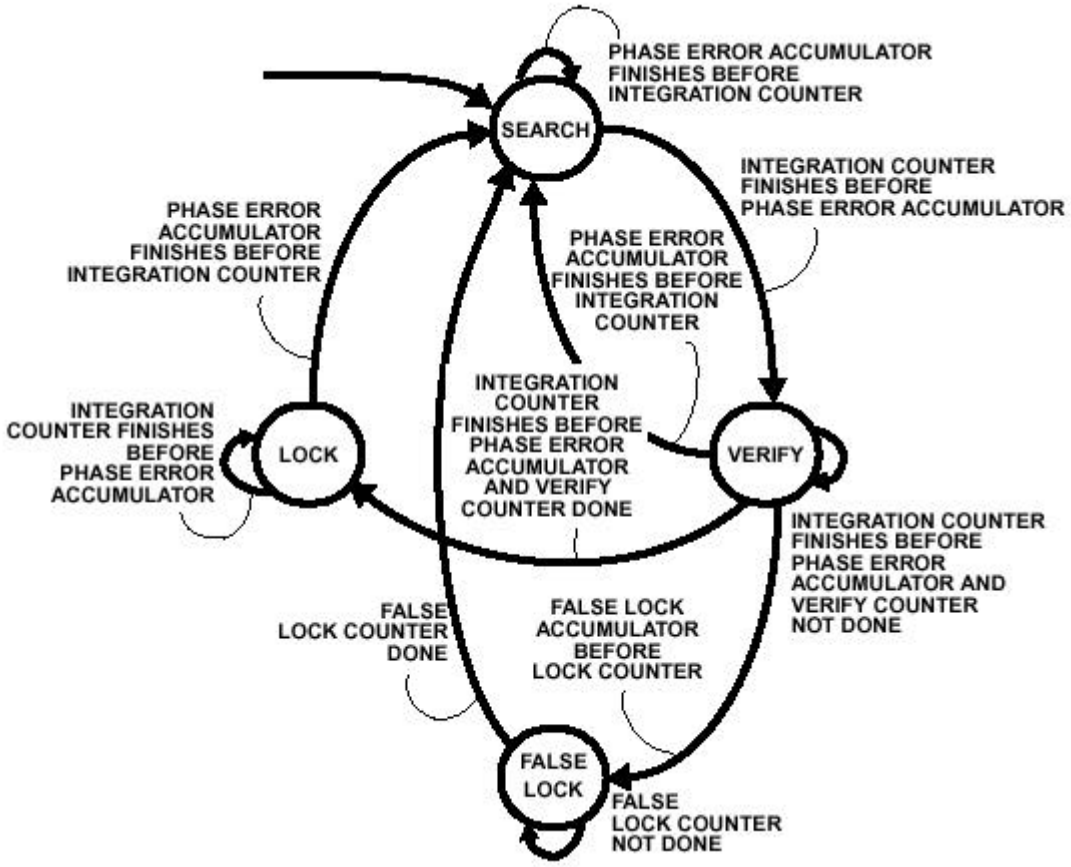

Figure 4. Acquisition/tracking state diagram.

Example for search to verify: If the acquisition threshold is 20 degrees and the acquisition integration time is 8 symbols, then verify is obtained if the magnitude of the phase error accumulated for 8 symbols is under 20 degrees. If the acquisition sweep rate is 2 KHz and the carrier tracking loop limit is 100 KHz, then 2000 is added/subtracted to the carrier accumulator to produce a frequency correction value over a 100,000 range.

Example for verify to lock: If the track threshold is 22 degrees and the track integration time is 32 symbols, then lock is obtained if the magnitude of the phase error accumulated for 32 symbols is under 22 degrees. Lock is maintained under the same criteria.

Wide loop bandwidths improve acquisition time but loss of synchronization occurs sooner as E_b/N_0 decreases. A narrow loop bandwidth's longer acquisition time can be somewhat compensated for with a smaller symbol integration count. However, small symbol integration counts negatively influence E_b/N_0 and multipath fade tests. Higher symbol integration counts yielded lower E_b/N_0 synchronization and deeper multipath fade tolerance. The track symbol integration count greatly influenced the acquisition time performance measurement, where the acquisition symbol integration count was not as significant. The acquisition symbol count is set to 8 and the track symbol count is set to 28 for narrow carrier track loops and to 32 for wide carrier track loops in the following performance tests. The thresholds are set to 22.5 degrees or less for this quadrature application.

The flat fade and acquisition time testing is affected by the carrier tracking mode. Three tracking modes offer a trade-off between delay around the loop and how well the signal is kept centered in the filtering. The DCL only mode provides for a lower bit error rate (BER) and faster acquisition times.

The number of serial bits sent for carrier offset frequency (COF) and symbol offset frequency (SOF) control loops is programmable from 8 to 32 bits and affects fade and acquisition performance tests. A 16-bit COF word will allow a 1 KHz frequency correction and a 16-bit SOF word will allow a 500 Hz frequency correction in the respective loops. 16-bit words are a minimum and allow for faster updates and less delay around the loops.

No external radio frequency (RF) automatic gain control (AGC) is employed in this system. Baseband AGC internal to the integrated circuits is inherent to the various closed loop designs.

The carrier tracking acquisition sweep rate was set by selecting the optimum value during the flat fade, low E_b/N_0 operation.

The DQT provides five selectable FIR low pass filters for operating on the down-converted channel. The third-order cascade-integrator-comb filter with compensation provides the highest out-of-band attenuation. Compensation flattens the frequency response of the filter and greatly improves the flat fade tests. The ACI test requires this type of filter for effective operation.

The DCL provides two selectable matched filters, a root-raised cosine (RRC) filter and an integrate and dump (I&D) filter. The two were tested and did not meet bit error performance requirements. Subsequently, the internal DCL matched filtering was bypassed, and the FIR filters, external to the DCL, were utilized. These serial FIR filters have been programmed with RRC filter coefficients. Several filter alphas and filter lengths were tested and found to meet or exceed the bit error performance

requirement. The serial processing rate of the FIR filters limit the data throughput of the demodulator to 2.5 Mega bits per second (Mbps).

BIT ERROR PERFORMANCE

Bit error rate (BER) vs. signal energy per bit to noise power spectral density (E_b/N_0) is measured and plotted for bit error performance. The channel has a flat fading condition and is characterized as non-frequency selective. Attenuation of the signal occurs across the entire pass-band in an Additive White Gaussian Noise (AWGN) environment. The AWGN channel is characterized as memory-less, in which the probability of errors is independent from one symbol to the next.

Figure 5 is the test setup for performing bit error performance. The reference transmitter generates the FQPSK-B baseband analog I and Q symbols at programmable data rates [1]. The data content is an 11-bit pseudo-random binary sequence (PRBS). A RF mixer combines the symbols and the composite spectrum is sent to the digital receiver via the HP3708A, which is in the "E_b/N_0 mode". BER is measured on the bit error rate analyzer at the corresponding E_b/N_0 values. The FQPSK-B constellation diagram is monitored on an oscilloscope with symbol outputs from the digital receiver. BER vs E_b/N_0 was measured at 1.0 Mbps and at 2.5 Mbps with the carrier tracking and symbol tracking loops set to narrow (N) and then to wide (W) for each test. See Table 2 for results and comparison to FQPSK-B specification limit [2].

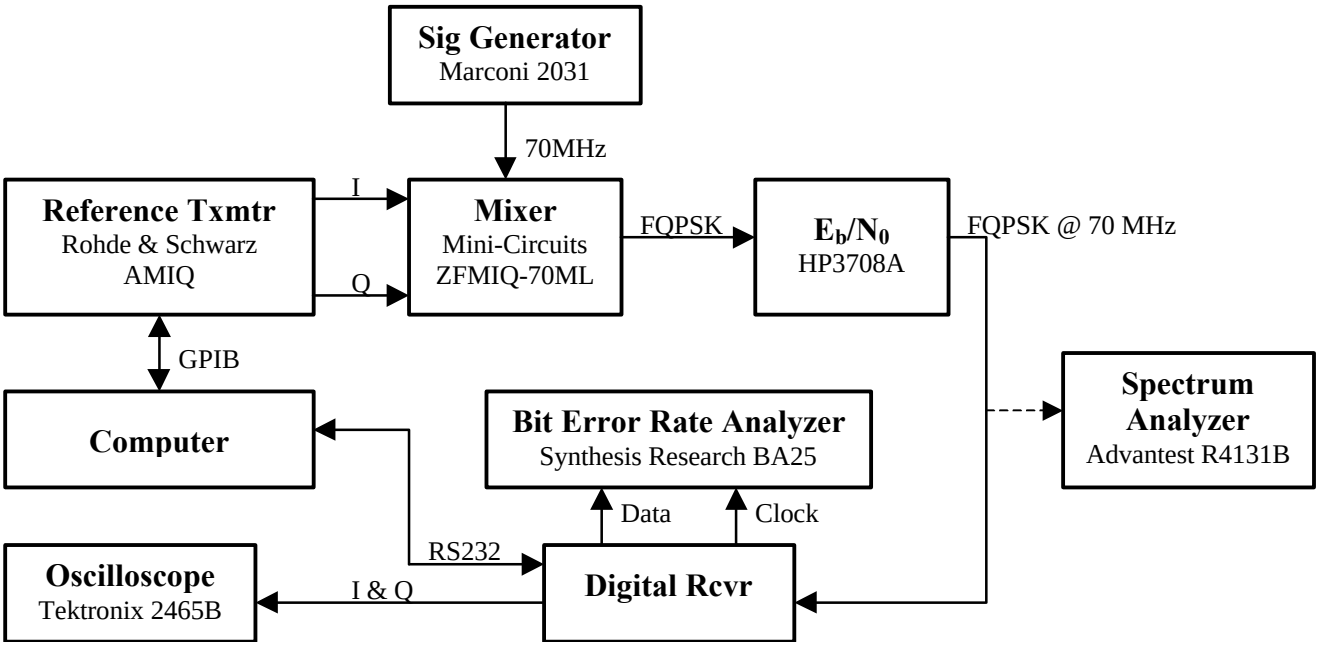

Figure 5. Bit error performance test.

	E_b/N_0 (dB)				
BER	**Allowed [2]**	**2.5 Mbps-N**	**2.5 Mbps-W**	**1.0 Mbps-N**	**1.0 Mbps-W**
10E-3	10.0	9.2	9.3	9.2	9.4
10E-4	12.0	11.1	11.3	11.1	11.3
10E-5	13.5	12.6	12.7	12.6	12.8
10E-6	15.0	13.7	13.7	13.8	13.9

Table 2. Bit error performance test results.

MULTIPATH FADING

All wireless communication systems can suffer from multipath propagation. The receiving antenna sees not only the direct signal but also a dominant secondary signal or signals, which is a delayed version of the direct signal path. This characteristic is known as frequency-selective fading and is indicated by a notch or notches in the RF spectrum. The depth and frequency of the notch vary continuously during multipath fading. The result is severe inter-symbol interference, which can lead to high bit errors and even loss of synchronization in the receiver.

It has been shown that 2-ray and 3-ray multipath models provide an excellent match to the obtained sounding flight data in the aeronautical telemetry channel [4]. Analysis showed that the magnitude of the reflection is the dominant factor in determining bit error rates. Strong multipaths are characterized by short delays on the order of 50 nano seconds (ns) [4]. Multipath reflections with longer relative delays on the order of 200 to 300 ns are much weaker [4].

For the FQPSK-B demodulator static multipath fade sensitivity requirement, the minimum phase critical notch depth shall be a minimum of 22 decibels (dB) when tested at 5 Mbps and a simulated delay of 24 ns [2]. At each frequency, the notch depth is increased until the BER is degraded to the threshold value of 10E-5 [1]. This value of notch depth becomes the “critical notch depth”.

Figure 6 is the test setup for performing multipath fading. The reference transmitter generates the FQPSK-B baseband analog I and Q symbols at programmable data rates [1]. The data content is an 11-bit PRBS. A RF mixer combines the symbols and the composite spectrum is sent to the digital receiver via the HP11759C, which is in the “phase spectrum mode”. In this mode, the delay, phase, and attenuation are set to generate a 2-ray multipath model. Note there is no automatic gain control in front of the receiver, which would affect this test. The FQPSK-B constellation diagram is monitored on an oscilloscope with symbol outputs from the digital receiver. The delays and notch depths were varied for these tests operating at 2.5 Mbps. Short delays and long delays were tested at the critical notch depth of the demodulator at a threshold BER=10E-5. Figure 7 displays these results plotted as nine-point static “M-curves”.

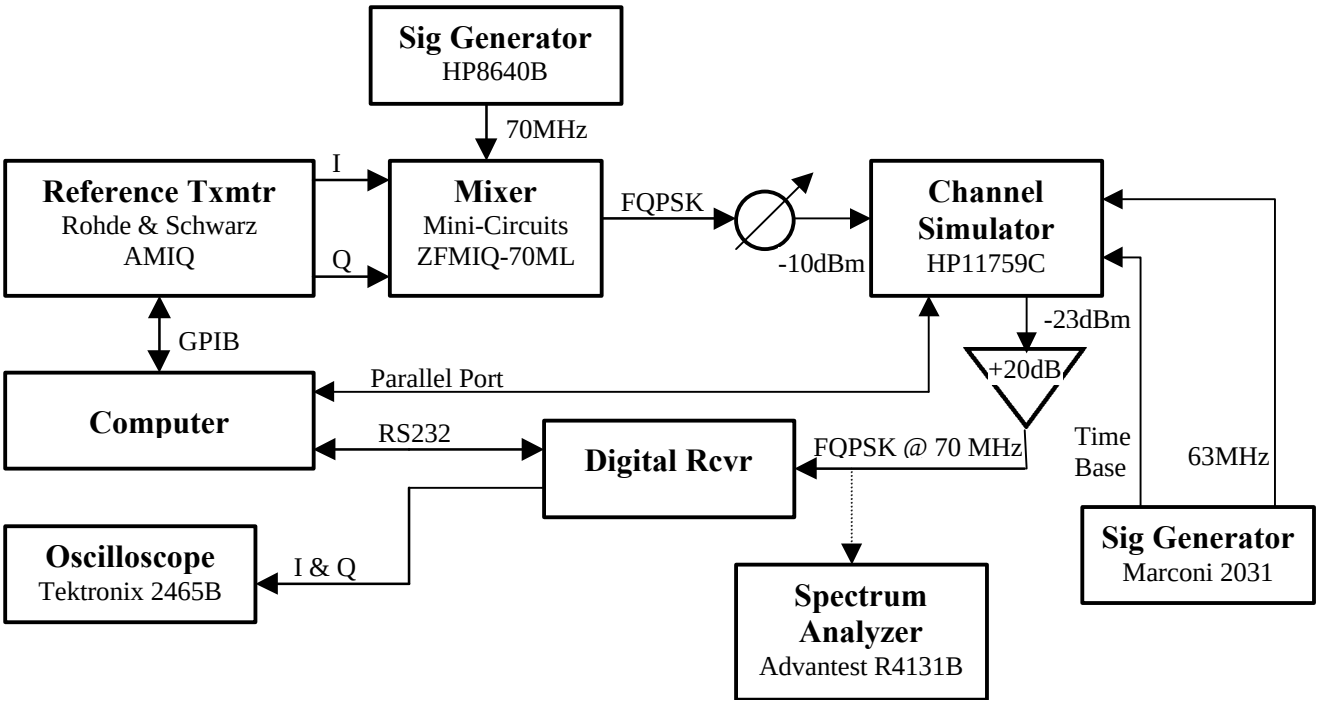

Figure 6. Multipath fade test.

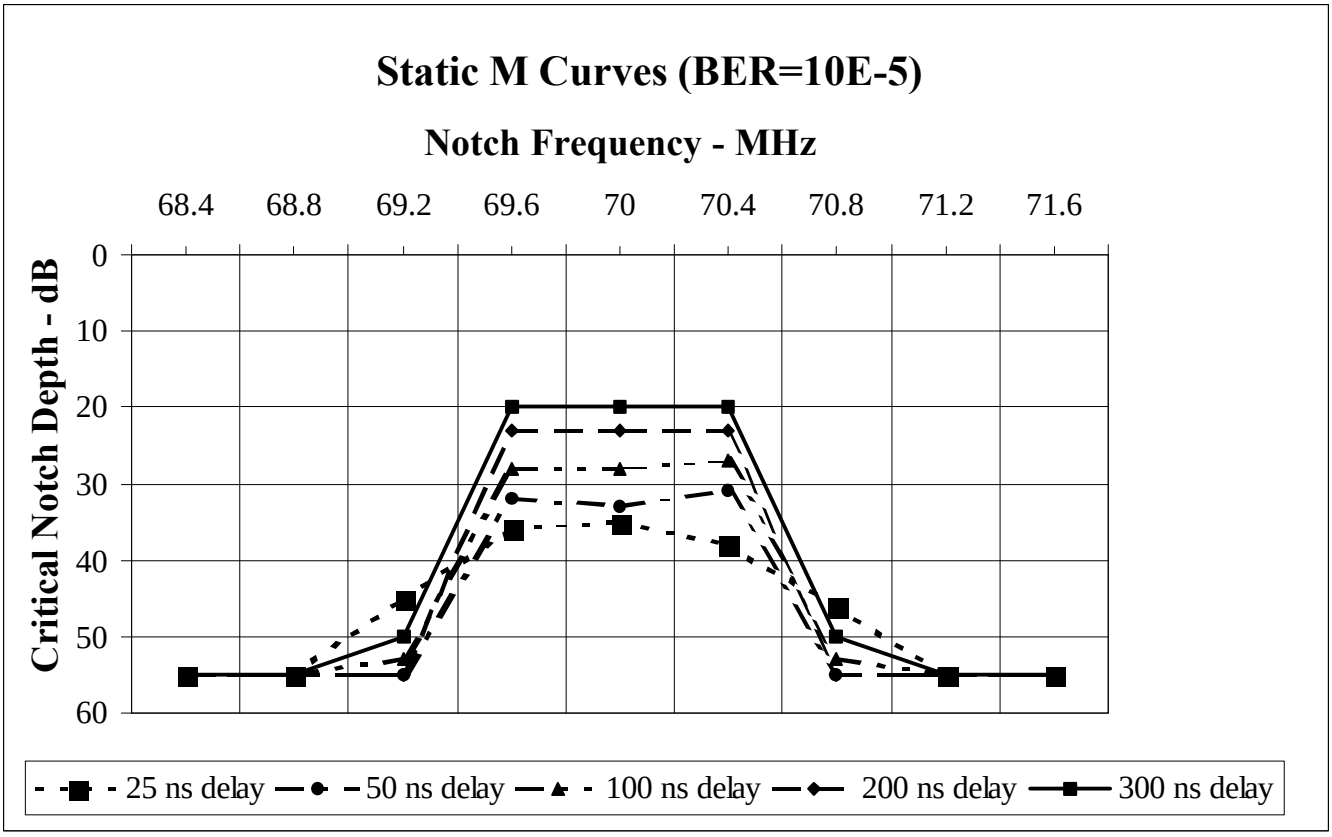

Figure 7. Multipath fade test results.

ADJACENT CHANNEL INTERFERENCE

This impairment relates to the generation of interference by multiple transmitters and the effects of interference at the receiver. ACI can cause eye closure in the demodulator and result in a BER penalty or loss in receiver sensitivity. ACI provides a measure of spectral power of the modulated RF signal spectrum spilling over into adjacent channels. Typically, a spectral mask is utilized to specify spectral efficiency and transmitter ACI indirectly. ACI interpretation and impact depends on the application, and for this reason many definitions exist [5].

For the FQPSK-B demodulator performance requirement, an E_b/N_0 = 13.5 dB maximum at a BER = 10E-5 shall not increase by more than 1 dB when the desired signal is subjected to ACI from one interfering signal [2]. The FQPSK-B interference source will be at the same bit rate as the desired signal, offset from the desired carrier frequency by an amount equal to 1.2 times the bit rate and at a power level 20 dB higher than the desired signal [2]. The requirement applies to ACI tests at both the high and low frequency side of the desired signal [2].

Figure 8 is the test setup for adjacent channel interference. The reference transmitter generates the FQPSK-B baseband analog I and Q symbols at programmable data rates [1]. The data content is an 11-bit PRBS. A RF mixer combines the symbols and the composite spectrum is sent to the digital receiver via the HP3708A, which is in the "carrier-to-noise plus interferer mode". The carrier-to-noise (C/N) ratio of the desired signal is set for a BER = 10E-5. RF power levels of the desired signal and the interfering signal were adjusted to obtain various carrier-to-interferer (C/I) ratios. The FQPSK-B constellation diagram is monitored on an oscilloscope with symbol outputs from the digital receiver.

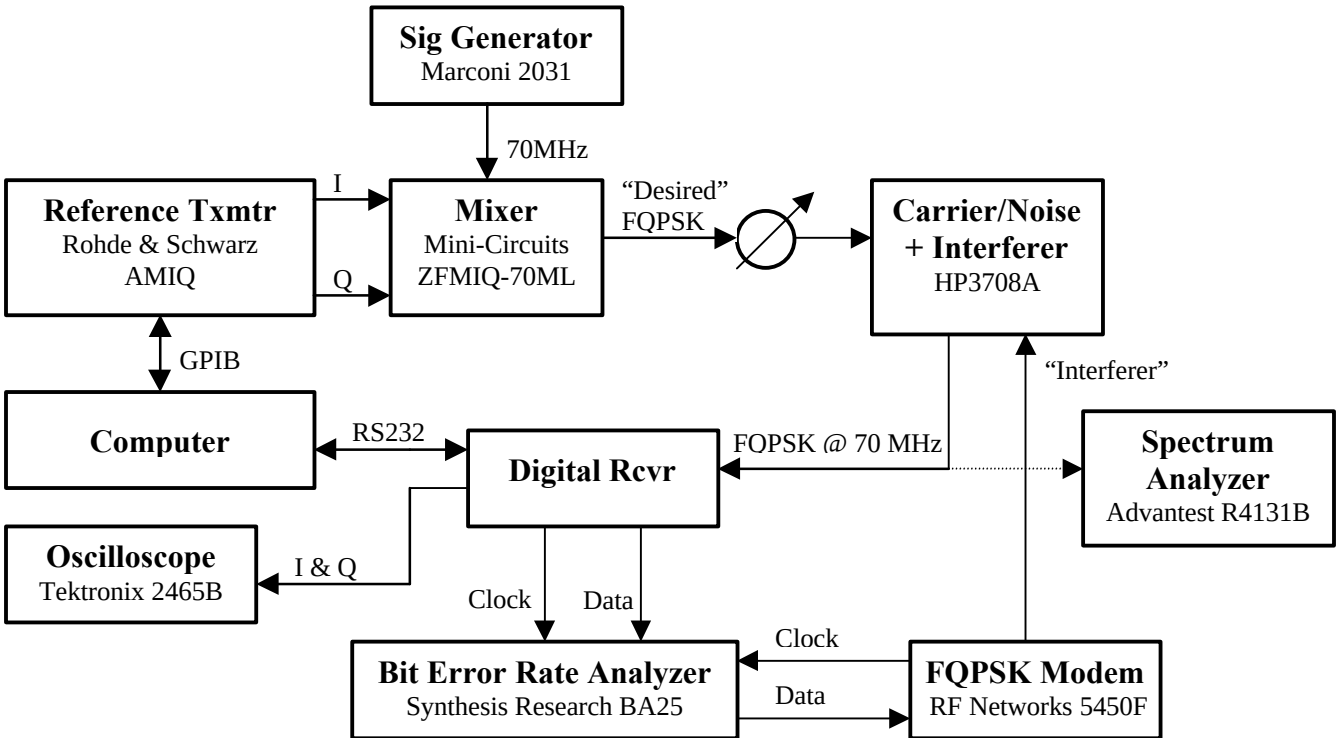

Figure 8. Adjacent channel interference test.

The data rate is 1.0 Mbps and the BER is monitored as the interfering signal power level is varied. The frequency separation of the interfering signal is offset from the desired carrier frequency first by 1.0 times the bit rate and then 1.2 times the bit rate at the high and low frequency sides. The results are tabulated in Tables 3 and 4.

1 Mbps, Carrier = 70 MHz, Interferer = 69/71 MHz		
C/I (dB)	**BER**	**E_b/N_0 Loss (dB)**
-11	1.0 10E-5	0
-17	5.0 10E-5	1.0
-20	1.5 10E-4	1.8

Table 3. ACI test results (Interferer frequency offset at 1.0 times bit rate).

1 Mbps, Carrier = 70 MHz, Interferer = 68.8/71.2 MHz		
C/I (dB)	**BER**	**E_b/N_0 Loss (dB)**
-14	1.0 10E-5	0
-17	2.5 10E-5	0.5
-20	5.5 10E-5	1.0

Table 4. ACI test results (Interferer frequency offset at 1.2 times bit rate).

ACQUISITION TIME & FADE RECOVERY TIME

The amount of time required for a receiver to resynchronize and produce error free data when the input signal is abruptly switched between AWGN and the desired signal is an important measurement.

For the FQPSK-B demodulator specification, the initial acquisition time is 25 milli seconds (ms) maximum for the demodulator to synchronize and produce a BER of 10E-3 or better with E_b/N_0 = 10dB [2]. Fade recovery time is 5 ms maximum for the demodulator to recover from short duration flat fades and frequency selective fades when the fading event causes loss of synchronization [2].

Figure 9 is the test setup for performing acquisition time and fade recovery time. The reference transmitter generates the FQPSK-B baseband analog I and Q symbols at programmable data rates [1]. The data content is a continuous run of 1's randomized with a 15-bit randomizer. A RF mixer combines the symbols and the composite spectrum is sent to the digital receiver via the RF switch, which is alternating between the FQPSK-B signal and AWGN at a 1 Hz rate. The RF power levels of the signal and noise are set equal to each other. The digital receiver's derandomizer is enabled. The FQPSK-B constellation diagram is monitored on an oscilloscope with symbol outputs from the digital receiver. Data recovered at 2.5 Mbps from the digital receiver is monitored on another oscilloscope. Resynchronization is declared when the bit sequence stabilizes at a logic 1. One-hundred contiguous cycles are monitored and a count of the number of times each cycle exceeds the acquisition time or the fade recovery time is noted in Table 5. The test is repeated at low, middle, and high power levels in the

operating range of the receiver. The carrier loop and symbol loop bandwidths are tested at narrow (N), medium (M), and wide (W). Also during this test, the carrier frequency was swept 100 KHz at a slow rate to verify frequency offset tracking. Carrier sweep: 69.95 MHz to 70.05 MHz, 1000 steps, and 200 ms/step.

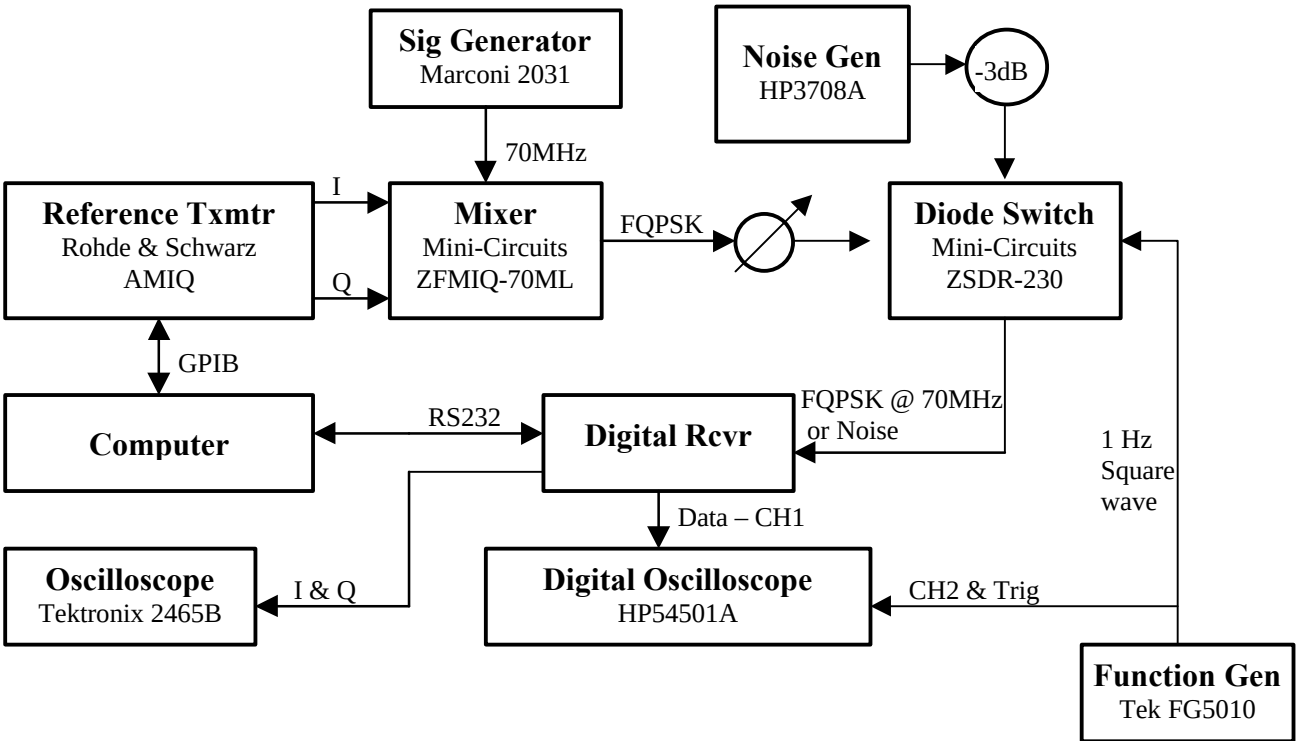

Figure 9. Acquisition and fade recovery time test.

RF Power:	**Low (-46dBm, Eb/No=10dB)**								
Carrier Loop BW:	**N**			**M**			**W**		
Symbol Loop BW:	**N**	**M**	**W**	**N**	**M**	**W**	**N**	**M**	**W**
% > 25 ms:	86	87	88	45	41	40	21	16	12
RF Power:	**Medium (-15dBm, Eb/No=20dB)**								
Carrier Loop BW:	**N**			**M**			**W**		
Symbol Loop BW:	**N**	**M**	**W**	**N**	**M**	**W**	**N**	**M**	**W**
% > 5 ms:	95	95	92	74	77	72	53	60	53
RF Power:	**High (+10dBm, Eb/No=20dB)**								
Carrier Loop BW:	**N**			**M**			**W**		
Symbol Loop BW:	**N**	**M**	**W**	**N**	**M**	**W**	**N**	**M**	**W**
% > 5 ms:	91	93	95	72	73	74	49	53	57

Table 5. Initial acquisition time and fade recovery time results.

ACKNOWLEDGMENT

The Advanced Range Telemetry (ARTM) Program funded and provided technical support for this effort.

SUMMARY

A digital receiver consisting of two Intersil evaluation boards and one custom interface board has been integrated and tested. Performance measurements for various receiver parameter settings have been made and compared to the ARTM performance specification for FQPSK-B demodulation. Bit error performance, multipath fading, adjacent channel interference, acquisition time, and fade recovery time measurements were made.

Bit error performance tests showed the digital receiver operated close to 1 dB better than the allowed specification E_b/N_0 curve. The matched filtering symbol detection is the key element for this test. The implemented filter was a simple RRC. Filters that take advantage of the FQPSK-B waveform properties would yield even lower E_b/N_0 curves. A 1 dB change in E_b/N_0 is significant in that it can result in an order of magnitude change in BER at the steeper end of the curve.

The multipath fade test implemented a 2-ray model. The results exceeded the performance requirement. The static M-curve plots show how the receiver copes with multipath as the notch moves through the passband. The smaller the M-curve, the better multipath rejection. The receiver showed 35 dB critical notch depth at the center of the passband with 25 ns delay of the reflected ray. The receiver showed 20 dB critical notch depth at the center of the passband with 300 ns delay of the reflected ray. This lines up with the flight data on the aeronautical telemetry channel showing strong multipath on short delays rays and weak multipath on long delay rays. Higher rejection is required on the short delay reflections. Inherent properties of the digital filtering, like low passband ripple and excellent linear phase, contribute to this performance operation.

Adjacent channel interference performance measurements met the required specification limit. An interfering signal at the specification requirement caused 1.0 dB of loss in E_b/N_0. When the same interfering signal was moved closer in frequency to the desired signal, a higher loss of 1.8 dB in E_b/N_0 was indicated as expected. Reducing the interfering signal power by 3 dB also reduced the E_b/N_0 loss by about half. The high stopband attenuation and sharp shape factor of the FIR low pass filtering in the channel down-conversion section provides this good isolation.

Acquisition time and fade recovery times were somewhat excessive in this receiver for the aeronautical telemetry channel application. The carrier and symbol tracking loops require integration periods and decision transitions to acquire or reacquire lock, which take a finite amount of time. The design architecture and operational parameter settings of the tracking loops affect the performance for a particular application.

The configuration settings of the parameters in the digital receiver had to be operationally verified across all the performance tests. This can be considered an iterative cross optimization approach. For example, parameter settings that yielded good receiver bit error performance may have resulted in

diminished acquisition time performance. Any receiver should be thoroughly tested via controlled performance measurements before fielded.

REFERENCES

1. Advanced Range Telemetry Project, Edwards AFB, California, "Specialized Test Methods for FQPSK-B Transmitters and Demodulators", Version 1.1, April 29 1999, Document FO4611-99-R-0005.

2. Advanced Range Telemetry Project, Edwards AFB, California, "Performance Specification, FQPSK-B Demodulator", Version 1.0, April 12 1999.

3. Feher et al. U.S. Patents: 4,567,602; 4,644,565; 5,491,457, 5,784,402; post-patent improvements and other U.S. and international patents pending; Digcom, Inc.; 44685 Country Club Drive; El Macero, CA 95618; USA; Tel. 530-753-0738; Fax 530-753-1788.

4. M. Rice, D. deGaston, A. Davis, G. German, C. Bettwieser: " RTM Channel Sounding Results – An Investigation of Frequency Selective Fading on Aeronautical Telemetry Channels", Proceedings of the International Telemetering Conference, Las Vegas, October 25-28, 1999.

5. K. Feher, R. Jefferis, E. Law: "Spectral Efficiency and Adjacent Channel Interference Performance Definitions and Requirements for Telemetry Applications", Proceedings of the International Telemetering Conference, Las Vegas, October 25-28, 1999.

6. Intersil Corporation, "HSP50110/210EVAL User's Manual", January 1999, File Number 4149.1.

7. Intersil Corporation, "HSP50110 Digital Quadrature Tuner Data Sheet", January 1999, File Number 3651.4.

8. Intersil Corporation, "HSP50210 Digital Costas Loop Data Sheet", January 1999, File Number 3652.4.

9. Intersil Corporation, "Using the HI5703 Evaluation Board", January 1996, File Number 9534.1.

APPENDIX

DQT and DCL Register Values

DQT_Register_# 0 40000000
DQT_Register_# 1 10000000
DQT_Register_# 2 0000001B
DQT_Register_# 3 0100FF20
DQT_Register_# 4 00000186
DQT_Register_# 5 00200019
DQT_Register_# 6 00003F28
DQT_Register_# 7 00000000
DQT_Register_# 8 00000000
DCL_Register_# 0 001BC1B1
DCL_Register_# 1 00000034
DCL_Register_# 2 0F68FF00
DCL_Register_# 3 0000000A
DCL_Register_# 4 00000000
DCL_Register_# 5 00000000
DCL_Register_# 6 00000000
DCL_Register_# 7 0000000A
DCL_Register_# 8 0051EB85
DCL_Register_# 9 FFAE147B
DCL_Register_# 10 00026A00
DCL_Register_# 11 0001A66C
DCL_Register_# 12 053544A2
DCL_Register_# 13 00000000
DCL_Register_# 14 00000000
DCL_Register_# 15 0001A36E
DCL_Register_# 16 FFFE5C92
DCL_Register_# 17 00032EEE
DCL_Register_# 18 0000EDCC
DCL_Register_# 19 00000000
DCL_Register_# 20 0000181C
DCL_Register_# 21 FF8EFE2B
DCL_Register_# 22 00000000
DCL_Register_# 23 00002890
DCL_Register_# 24 00000000
DCL_Register_# 25 00000000
DCL_Register_# 26 00000020
DCL_Register_# 27 00000222
DCL_Register_# 28 00000007
DCL_Register_# 29 00000000
DCL_Register_# 30 00000000
DCL_Register_# 31 00000000