UTILIZATION OF FIELD PROGRAMMABLE GATE ARRAYS AND DIGITAL SIGNAL PROCESSING MICROPROCESSORS IN AN ADVANCED PC TT&C SATCOM SYSTEM

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ABSTRACT

L-3 Communications Telemetry & Instrumentation (L-3 T&I) has developed an advanced IBM PC-AT Telemetry, Tracking, and Commanding (TT&C) SATCOM system based on the utilization of Field Programmable Gate Array / Digital Signal Processing (FPGA/DSP) microprocessors. This system includes up-link, down-link, and range processing sections. Physically, the system consists of one IF Transceiver and two or more FPGA/DSP microprocessor boards called Advanced Processing Microprocessors (APMs). The form factor of these PWBs is compliant with full length, full height IBM PC PCI bus cards. This paper describes the features and functionality of an advanced Telemetry, Tracking, and Commanding Processing System (TT&CPS) based on the implementation of FPGA and DSP microprocessors.

The high-level functional attributes of the TT&CPS are depicted in Figure 1. There are four main functional blocks: the IF Transceiver, the Down-Link Processing Section, the Up-Link Processing Section, and the Range Processor. The analog/IF circuitry in the IF Transceiver card interfaces between the 68–72 MHz (70 MHz, nominal) IF I/O signals and the Up-Link and Down-Link Processing Section's DSP equipment. The down-link portion of the IF Transceiver card has two user-selected input ports. From the selected input, the signal is processed through selectable bandwidth limiting, gain control, Doppler correction (optional), quadrature down-conversion to zero hertz (baseband), selectable baseband filtering, and precision Analog-to-Digital (A/D) conversion. The up-link portion of the IF Transceiver card takes I/Q digital data from the APM performing the up-link processing functions. This baseband I/Q digital data is Digital-to-Analog (D/A) converted, filtered, quadrature up-converted to 68–72 MHz, up-link Doppler corrected (optional), output level detected and level controlled, and sent to a two-position output selector switch.

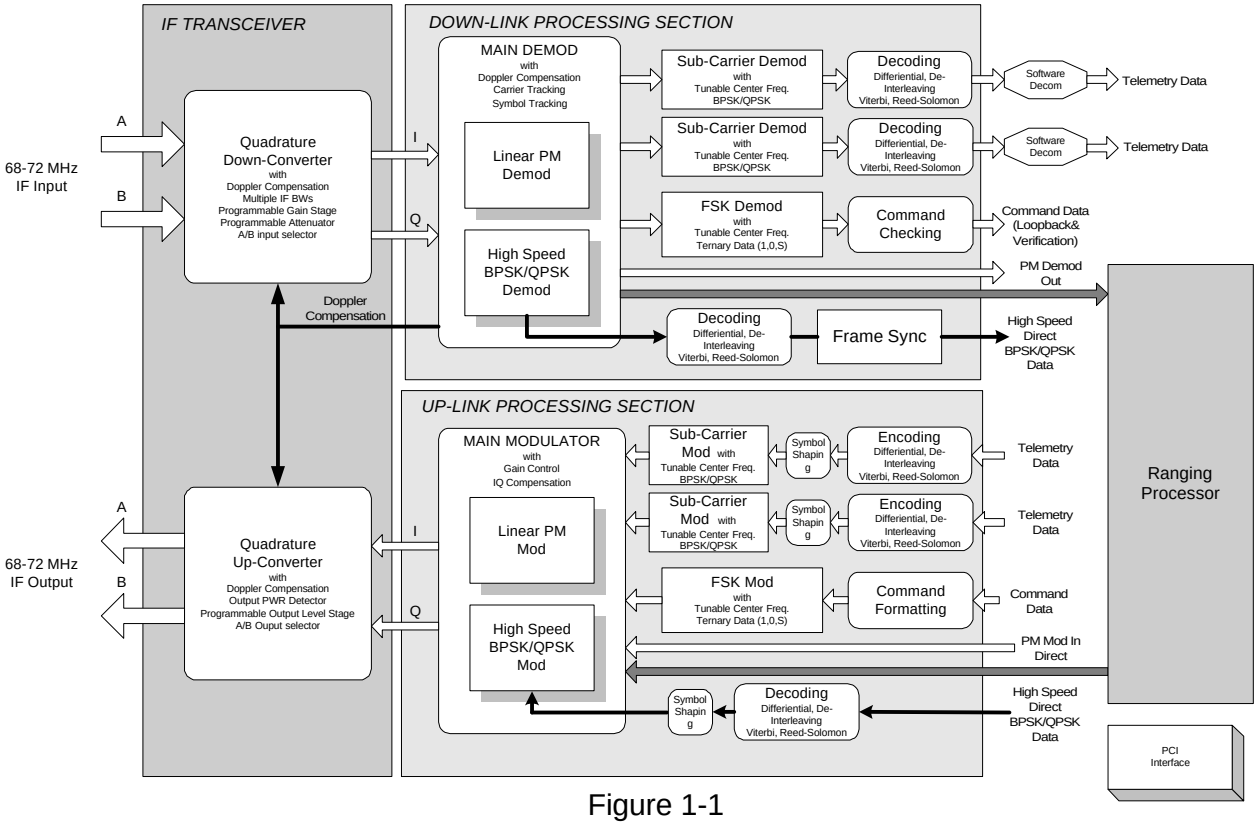

Figure 1-1

Figure 1. Telemetry, Tracking, and Commanding Processing System Functional Diagram

The down-link portion of the TT&CPS provides main carrier linear PM or BPSK or QPSK demodulation and can also, in composite linear PM demodulation mode, receive and demodulate FSK and/or BPSK subcarriers and ranging signals. The demodulators use symbol timing loops and bit decision circuits (matched filters) to perform the bit synchronization function. Several decoding algorithms, including differential, de-interleaving, Viterbi, and Reed-Solomon, are available for the down-link telemetry. Command format checking and CRC status is also available on FSK-demodulated data. Direct carrier BPSK/QPSK demodulation has decoding and frame synchronization capabilities. Because of the modular construction of the firmware and the use of FPGAs and DSPs, the system can be loaded with only the functions in use, lowering initial setup time while increasing overall system capability. To support a particular function, the card is downloaded with an "image," which programs the FPGAs and DSPs at initialization. The user can change configurations by simply downloading a new set of instructions to the FPGA/DSP on the fly to keep the ground station running with minimal downtime. The flexibility of the design minimizes spare board costs, while achieving greater programmability at the end-user location.

KEY WORDS

DSP, FPGA, Digital Signal Processing, Field Programmable Gate Array, TT&C, Ranging, Satellite, Space, PC, Modulator, Demodulator, Decommutator, RF, IF, Doppler, PRN, Tone, MPTS, CCSDS

TT&C PROCESSING SYSTEM FUNCTIONAL OVERVIEW

The up-link portion of the TT&CPS provides main carrier linear PM or BPSK or QPSK modulation, and during main carrier PM mode, can generate tunable FSK and/or BSPK subcarrier commanding/telemetry signals. As with the down-link portion, several encoding algorithms, including differential, interleaving, convolutional, and Reed-Solomon, are available. Command formatting and CRC generation is also available on FSK modulator data. Direct carrier BPSK/QPSK modulation has encoding and symbol shaping capabilities. The subcarrier signals can be summed with ranging baseband signals from the Range Processor.

The FPGA/DSP-based Range Processor can generate tone and/or PRN signals for up-link as well as receive tone and/or PRN signals on the down-link and perform range processing. The ranging signals can either be baseband signals (for summing with other signals and then PM modulating the composite signal) or subcarrier modulated signals (PRN/BPSK, for example). The Range Processor works with the main demodulator in the Down-Link Section, which performs main carrier Doppler compensation. The Range Processor uses the main carrier Doppler to estimate residual Doppler on the ranging signals and to perform the final calculations of range and range rate.

The functional block diagram for the IF Transceiver of the TT&CPS is shown in Figure 2. This transceiver provides all analog signal processing and A/D or D/A conversion for both the down-link and the up-link. The Down-Link Section (shown on the top portion of Figure 2) receives the 68- to 72-MHz center frequency IF signal in one of two user-selectable input ports, potentially from the system's own PC-based RF down-converters. The signal is passed through a fixed pre-selector filter and then to a programmable attenuator. The programmable attenuator is only used during periods of high input signal levels to maintain optimum Signal-to-Noise (S/No) levels in the rest of the down-converter chain.

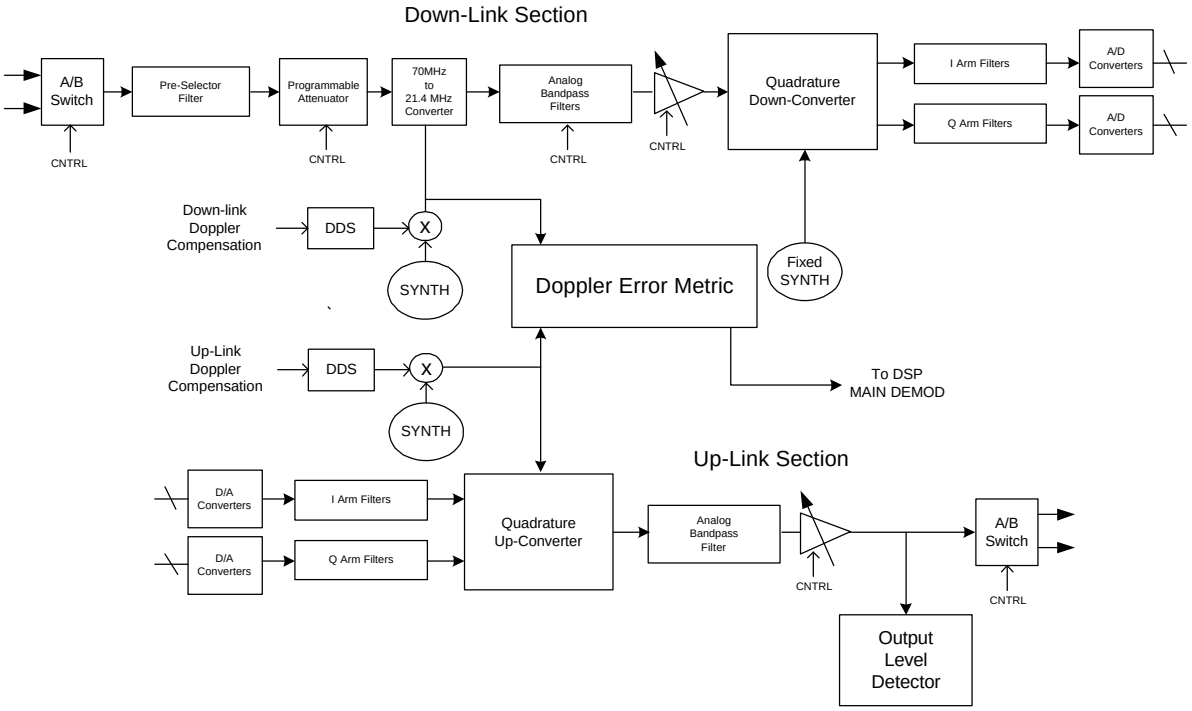

Figure 2. IF Transceiver Card Functional Block Diagram

The next signal processing block is a 70- to 21.4-MHz converter. This converter has several functions. First, it establishes the user-selectable center frequency (68–72 MHz) in 1 kHz steps. Second, it provides an LO signal to the Doppler error metric section for Doppler or frequency error detection of the main carrier. Third, it can be used to compensate for the Doppler or frequency error shift. The control of this Doppler compensation comes from DSP circuits in the Down-Link Section of the TT&CPS.

The next block, the Analog Bandpass Filters block, represents a bank of user-selectable IF bandwidth filters. These filters are used to optimize the S/No of the incoming signal. The signal then passes through a gain control amplifier that is controlled from DSP circuits in the Down-Link Section of the TT&CPS.

The next block is the Quadrature Down-Converter, which takes in the conditioned 21.4-MHz IF signal and performs a quadrature down-conversion to zero hertz. The LO used for this conversion is fixed. The I/Q signals from the Quadrature Down-Converter are passed through user-selectable arm filters (low-pass filters), which limit the bandwidth of the signals into the A/D converters. The 12-bit A/D converters are clocked by a low-phase noise, high accuracy 32-MHz master conversion clock. From this point, both A/D outputs and the 32-MHz clock are converted to differential signals and are sent to the Down-Link Section of the TT&CPS.

The Up-Link Section of the IF Transceiver is shown on the bottom portion of Figure 2. This section receives I and Q data in a differential digital format from the Up-Link Section of the TT&CPS. This data is clocked into the D/A converters using the same 32-MHz master conversion clock that is used in the Down-Link Section. The I/Q analog output signals from the D/A converters are filtered and sent to a quadrature up-converter that converts the I/Q baseband data into an IF signal at 70 MHz, nominal.

The Quadrature Up-Converter has several functions. First, it establishes the user-selectable output center frequency (68–72 MHz) in 1 kHz steps. Second, it provides an LO signal to the Doppler error metric section for Doppler or frequency error detection of the main carrier. Third, it can be used to compensate for the Doppler or frequency error shift. The control of this Doppler compensation comes from DSP circuits in the Down-Link Section of the TT&CPS. The output of the Quadrature Up-Converter is sent through a bandpass filter and through a user-programmable gain/level control stage. The output signal is then sent to both an SPDT RF switch and an output level detector circuit. The output level detector circuit is used to monitor the output level of the Quadrature Up-Converter and also for system-level calibration. The signal is then made available for the TT&CPS' own PC-based RF up-converters or other up-link equipment.

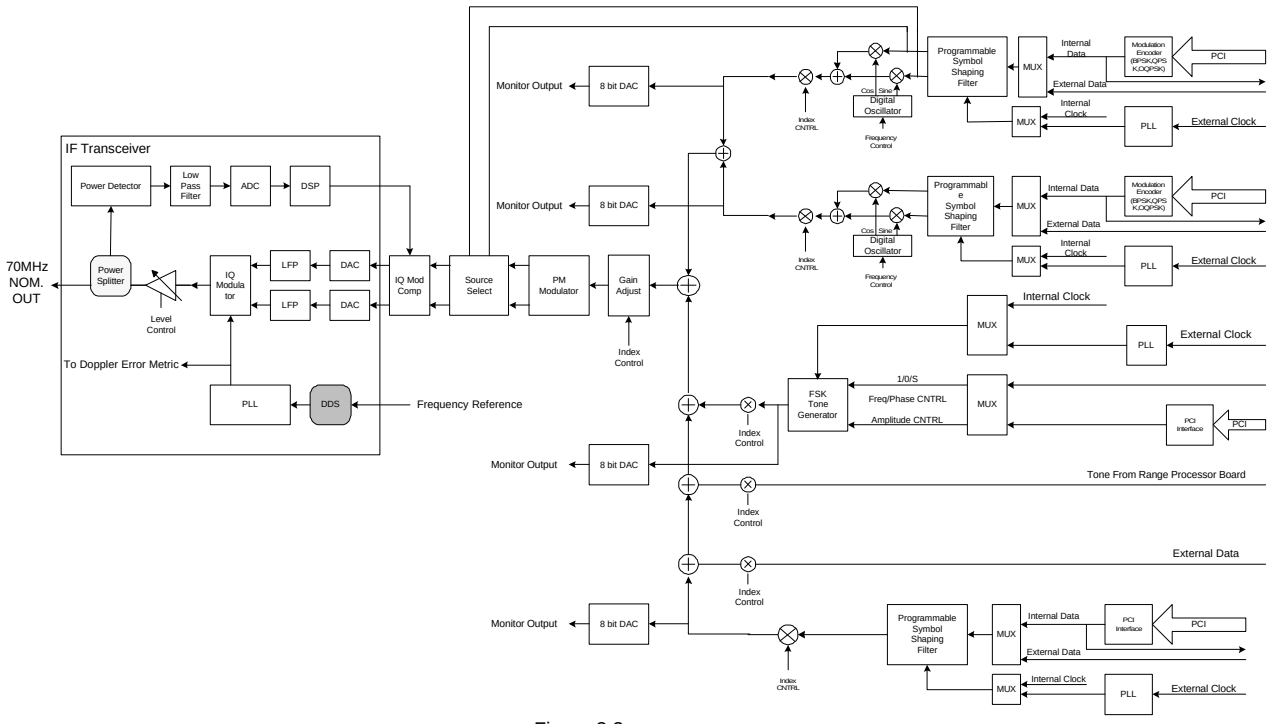

Figure 3. TT&CPS Up-Link Processor

UP-LINK SECTION

The Up-Link Section of the TT&CPS is shown in Figure 3. The functional blocks shown within the dashed box are part of the IF Transceiver card. The remaining functional blocks are accomplished within the FPGA/DSP, also known as the PCI Advanced Processing Microprocessor (PCI APM) card. Overall, this portion of the system provides the capability for:

- Direct BPSK/QPSK or linear PM modulation
- Linear PM with
  - Up to two, tunable BPSK/QPSK subcarriers
  - FSK commanding
  - Tone or PRN ranging
  - Direct data input
- Up-link Doppler compensation
- Output level control

The functional block in the upper right of Figure 3 can be used either for direct BPSK/QPSK modulation or for subcarrier BPSK/QPSK modulation. The data source can be either internal (via the PCI bus) or external. Data can be presented as separate I/Q data or as a single stream that is internally split between the I/Q channels. Also, internally generated data can be output to an external device like an encrypter or encoder, and then the externally processed data can be brought back in via the external data ports for modulation.

Programmable symbol shaping filters are available to provide a variety of symbol shaping capabilities, including Square Root Raised Cosine symbol shaping with user-defined alpha factors from 0.3 to 1.0. The shaped symbols are sent to either a programmable quadrature up-converter (when generating a subcarrier), which establishes the center frequency of the subcarrier, or to the main modulator's I/Q arms (for direct BPSK/QPSK modulation). In the subcarrier generation mode, the I/Q signal is converted to a composite signal and is then passed to a gain control stage. The gain control stage establishes the modulation index of the subcarrier onto the main linear PM carrier. This signal can also be sent to an 8-bit DAC for monitoring purposes. The functional block just below this section provides an optional second BPSK/QPSK subcarrier generator with the same capability as the first. For PRN ranging on a subcarrier, the baseband PRN sequence can be put into either of these subcarrier generators.

The next section down is the FSK Commanding Section. Once again, the data source is either internal (via the PCI bus) or external. Three tones, "1," "0," and "S," can be independently controlled or disabled. The TT&CPS allows the user to use (or not use) the "S" tone in a variety of different ways. The Command Timing Processor (CTP) is a flexible timing processor used to generate four TTL control signals that generate "1," "0," "S" and clock FSK command tones. Each tone control signal is independently controlled with $\leq$50 nS resolution. Complex timing and functional relationships between the four tones can be easily defined. The system supports Non-Return to Zero Frequency Shift Keying (NRZ-FSK), Return to Zero FSK (RZ-FSK), Bi-Phase Low FSK (BP-L FSK), EXECUTE pulses with programmable length and period, automatic command header, command separation, and fill data insertion, as well as a wide variety of error detection encoding. The clock signal can be continuous or a burst format. Its phase relationship to any other signal can be adjusted $\pm$180 degrees with 1 degree accuracy.

Command building is performed either by a commanding software package or by the TT&CPS' Windows NT-based application software. Commanding data can also be sent through the BPSK/QPSK subcarrier modulators described above.

The last few blocks on the lower right side of Figure 3 allow data to be presented directly to the PM Modulator's baseband input. Range tone signals can be summed in at this point as well as generic, external digital data. Each input has an amplitude control (or index control) that sets the PM modulation index for that portion of the complex baseband signal. The lowest input block can input data from either the PCI bus or an external source. Optional symbol shaping can be applied to this data. Once again, the PCI data can be supplied to an external device.

All of the first tier baseband processing elements discussed here are digitally summed into a composite baseband signal and applied to the Gain Adjust Block at the input to the PM Modulator. This block sets the overall mod index of the PM Modulator. The next processing block is the PM Modulator. The PM Modulator output I/Q data, which goes through an I/Q modulation compensation network, compensates for all amplitude and phase imbalances in the system, including the Analog Output Section. The remaining elements within the dashed block belong to the IF Transceiver.

DOWN-LINK SECTION

Figure 4 is a functional block diagram of the Down-Link Processor Section of the TT&CPS. The Down-Link Processor supports a wide variety of modulation schemes and data rates, including:

- Direct carrier linear PM and AM
- Direct carrier BPSK/QPSK (rates to 4 Msps)

- Direct carrier linear PM with
  - Up to two BPSK/QPSK subcarriers per board, with up to 4 optional per stream
  - FSK commanding
  - Ranging (tone, PRN, ESA (old), and ESA MPTS)

The IF signal (68- to 72-MHz center frequency) is input into the Down-Link Section of the IF Transceiver card. After the initial BandPass Filter (BPF) stage, the signal is sent through a voltage-controlled amplifier. The amplitude control is digitally derived in the DSP chain. This scheme will be described when we reach the amplitude measurement section.

After level adjustment, the signal passes through a 70- to 21.4-MHz down-converter and a bank of selectable analog BPFs. The system will select the optimal BPF that will pass (as close as possible) only the signal of interest. The filtered signal is then sent to the I/Q Quadrature Down-Converter. The Quadrature Down-Converter mixes the band-limited 21.4-MHz IF signal with a fixed 21.4-MHz LO signal. The I/Q output signals are therefore mixed to approximately zero hertz (baseband). In reality, these signals will initially be less than or greater than zero because of overall system-level frequency errors and Doppler frequency shifts. Note that the LO signal used in the 70 - to 21.4-MHz converter is derived from a Phase Lock Loop (PLL) synthesizer that uses a Direct Digital Synthesizer (DDS) for Doppler compensation. Also, the PLL's reference is derived from a master system reference that is used throughout the TT&CPS.

The DDS provides very fine granularity frequency control (<0.03 Hz), and no matter what the size of the step, provides phase continuous transitions. The Doppler correction signal also comes from digital DSP circuits (see the high-speed I/Q Demod Section). Next, the I/Q signals are sent through selectable analog low-pass filters. Once again, the system will select the optimum cut-off frequency. The filtered I/Q signals are then A/D converted at a fixed rate of 35 Msps. From this point on, all of the signal processing is performed digitally.

The digitized I/Q signals and the 35-MHz conversion clock are passed from the IF Transceiver card to the APM Down-Link Processor via differential drivers and receivers. The first DSP block is the Adaptive Equalizer. The Adaptive Equalizer is used for the removal of inter-symbol interference in direct BPSK or QPSK demodulation mode. The I/Q samples then go into a Filter and Decimate block. The amount of filtering and decimation performed in this section is a function of the information bandwidth within the complex signal. Another function within this block is level detection. The output level of both the I and the Q channels will be sampled and sent to one of the DSPs on the Advanced Processing Microprocessor (APM). This DSP will apply a second-order AGC control loop to the I/Q samples and output a continuous stream of digital words to control the AGC amp in the IF Transceiver through a D/A converter.

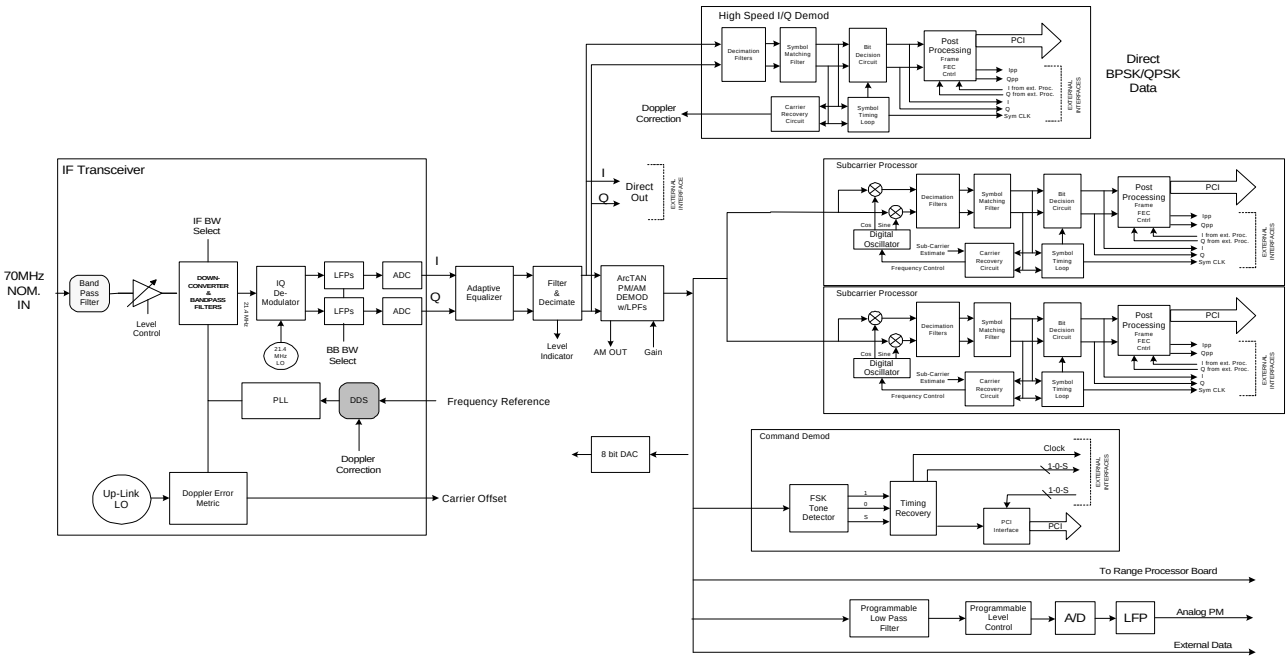

Figure 4. TT&CPS Down-Link Processor

The filtered I/Q samples are then sent to two separate demodulators and are available to the outside world through an external interface. The ARCTAN Demodulator performs linear PM and coherent AM demodulation. A gain control section is included in the ACRTAN Demodulator to set the deviation/bit sensitivity of both the AM and PM Demodulators. The recovered AM signal is sent to a programmable filter section and then to an A/D converter. Note that the recovered AM signal is available as both an analog and a digital signal and is compatible with most antenna control systems. The recovered PM signal is also sent to its own programmable filter section. If the recovered PM signal is the desired signal, it also can be taken either as a digital signal or as an analog signal (see the lower right-hand section of Figure 4). Since most ranging signals are in some fashion linear PM modulated onto the carrier, the system provides a digital interface of the recovered linear PM signal to the Range Processor.

The High-Speed I/Q Demodulator Section has two functions. First, it provides the detection of carrier (whether real or reconstructed) offset, which is sent to one of the DSPs in the APM for carrier tracking. A second-order control loop algorithm is applied to the carrier offset information, and the resulting stream of digital control words is sent to the DDS in the IF Transceiver to correct the Doppler frequency shift. This carrier detection function is present during all operational modes.

The second function of this section is to provide high-speed demodulation of directly modulated BPSK or QPSK signals. The incoming I/Q samples may, depending on the symbol rate, be further bandwidth limited and decimated. Then, depending on the demodulator's mode, another filter process will be applied. The two modes are Integrate

and Dump and Matched Filter/Sample. In the Matched Filter/Sample mode, a Symbol Matching Filter is applied that is specifically designed to match the characteristics of the modulator's shaping filter. This Symbol Matching Filter will create an output signal, which at one point in time optimally represents the symbol's state. The Bit Decision Circuit is used to sample the waveform at that point in time. The timing is established through the Symbol Timing Loop block just below the Bit Decision block. This circuit is essentially a bit synchronization circuit that creates a sample clock coherent with the incoming symbols. If the demodulator is in Integrate & Dump mode, the Symbol Matching Filter Section is used to establish the final bandwidth of the signal. Then, the Bit Decision Circuit performs an integration process over the bit period and samples the final result of the integration to decide the state of the symbol.

The final processing block in this section is the Post Processing block. This block contains frame synchronization and a variety of FEC algorithms (differential, Viterbi, Reed-Solomon, V.35, de-interleaving, etc.) as well as symbol de-multiplexing. The sequencing of these FEC algorithms is fully selectable. Also, provisions have been made to accommodate external processors (like decryptors). The externally processed data can be returned to the system for further processing and/or distribution on the PCI bus. The final processed data can be accessed either through the PCI bus (or Ethernet) or directly through the data/clock external interface.

Several subcarrier processors are available at the output of the PM demodulator. These include two BPSK/QPSK tunable subcarrier demodulators (processors), one FSK demodulator, and a variety of range processors (via a hand-off to the Range Processing card). The subcarrier processors are very similar to the high-speed I/Q Demod with one notable exception at their input. The subcarrier's center frequency is tuned very close to zero hertz via the Quadrature Down-Converter and a Digital Oscillator. The carrier recovery circuit (Digital Costos Loop) controls the Digital Oscillator and compensates for any residual Doppler. Note that initial acquisition of the signal is aided by an estimate of the residual Doppler derived from the main carrier Doppler. The remainder of the subcarrier processors operate the same way as the high-speed I/Q Demod except that the data rates are much less (<500K sps). The Command Demodulator is actually an FSK demodulator. It can detect up to three tones (1-0-S), each with tunable center frequencies. The 1-0-S data is sent to a Timing Recovery Circuit, which derives a coherent clock. Then, the 1-0-S data and clock is available to the outside world via the external interface or the PCI bus. External processing elements can also be applied to the commanding data via the remote interface and can then be routed back to the PCI interface.

RANGING FUNCTION

The development of a universal ranging system was a prime goal of the TT&CPS. Because of the wide variety of satellite-specific ranging solutions, the task of achieving this goal was a significant challenge. To meet the need for processing power and flexibility, a closely coupled system that utilizes analog processing, high-density Field Programmable Gate Arrays (FPGAs), Digital Signal Processors (DSPs), and the latest advancements in digital signal processing presents the best approach.

Satellite ranging systems typically can be divided into three types of designs: tone, digital-sequential ranging/PRN (pseudo-random noise), and hybrid (tone/digital combination) designs. Commercial GEO satellite systems often incorporate tone ranging systems because they are a simple and cost-effective solution to slow moving vehicles. One of the limitations of most tone ranging systems is that the period of the lowest frequency (MINOR) tone must be longer than the two-way range being measured. This limits the maximum range of these types of systems because the systems' modulators and demodulators have low frequency limits.

Ranging systems developed for deep space exploration overcome this problem by making use of long serial digital sequences or PRN codes. These digital signals appear to be random in nature, but always repeat over a descrete period, which resolves range ambiguity. The PRN code period can be made to be very long (days, months…), enabling ranging in the longest deep space missions. One problem brought on by these long codes is the long time required to acquire them, especially in low S/No environments. To combat this problem, some PRN ranging systems have been designed with PRN sequences that are a linear combination of several shorter PRN sequences. These shorter codes have unique properties that allow faster detector acquisition and sometimes intermediate range estimates using unique mathematical functions like the Chinese Remainder Theorem. These sequences are combined so that each of the individual codes can be independently detected, but the overall combination is unique and long enough to resolve the maximum range. It should be obvious, even with this limited introduction, that PRN systems can get very complicated and expensive. Note that the Chinese Remainder Theorem has also been used to overcome the maximum range limit problem in tone ranging described above.

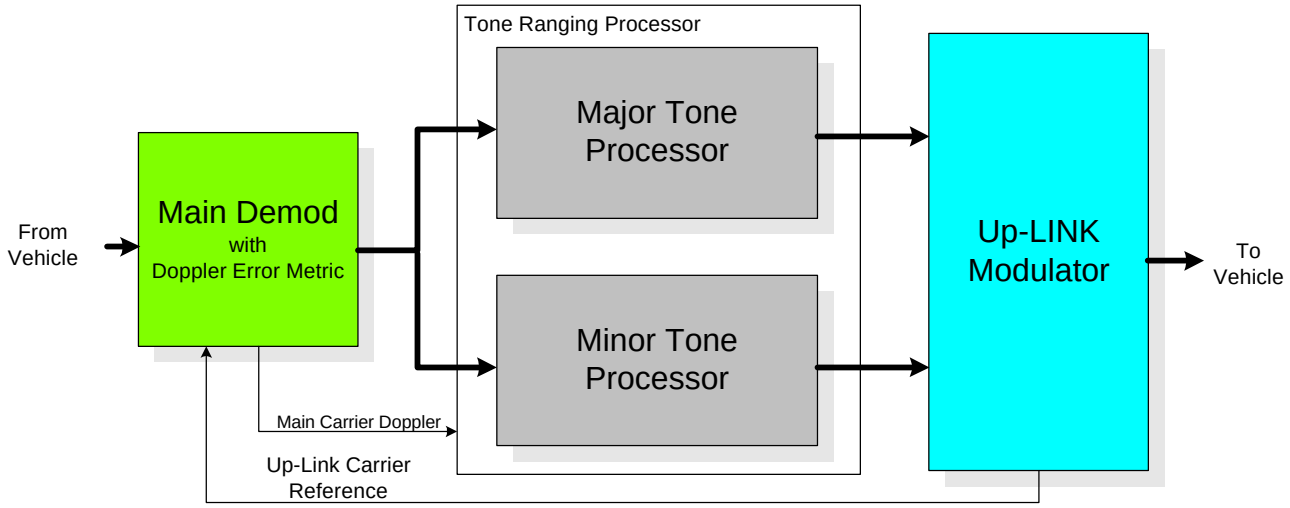

Figure 5. Tone Ranging Simplified System-Level Block Diagram

TT&CPS TONE RANGING*

The TT&CPS Tone Range Processor (TRP) uses Digital Signal Processing (DSP) techniques that are implemented partially in FPGAs and partially in a DSP processor. A simplified system-level block diagram is shown in Figure 5. The TRP can simultaneously generate and process one or two tones per Tone Range Processor-APM (TRP-APM). Up to one additional TRP-APM can be added to provide a maximum of four simultaneous tone signals. In any configuration, multiple tones or tone sets can be output in a sequential manner and can then be processed as a group. This is described in detail below.

The ranging tones are sent from the TRP to the Up-Link Modulator via a parallel digital word interface. The Up-Link Modulator combines the ranging tones with any other required up-link signals, PM modulates the composite signal, and then up-converts it to 70 MHz (nominal). As previously described in the IF Transceiver Section, the 70-MHz LO from the Up-Link Section is used as a reference in the Doppler error metric in the Down-Link Processor (DLP) to measure main carrier Doppler. The down-link IF signal from the vehicle is PM demodulated in the DLP, and the baseband information is presented to the TRP. The TRP uses a Digital Phase Lock Loop (DPLL), vector processing, and regression algorithms to generate an accurate measurement of the phase of each tone as well as the residual Doppler of the tone. Several acquisition aids are used, including FFT analysis, to quickly lock on to the tones and enable use of narrow loop bandwidths. Tone phase and Doppler information are presented to the PC via the PCI interface. The system software then either provides this tone phase information to an outside processor or performs the required processing to make a range determination. Note that both the vehicle and ground station propagation delays are accounted for in the range determination. Ground station

calibration is performed on a user-selected interval and requires a loop back of the test signal through the entire ground station (loop back at the antenna).

** Because of its complexity, PRN ranging will be discussed in another paper.*

SUMMARY

L-3 Communications Telemetry & Instrumentation has employed Field Programmable Gate Arrays and Digital Signal Processing microprocessors to great extent in creating an advanced PC TT&C SATCOM system. The FPGA/DSP microprocessors impact each critical subsystem within the TT&CPS, including up-link, down-link, and ranging. Advantages of the FPGA/DSP microprocessors realized by the system include increased capability and flexibility over other designs along with unparalleled integration of functions into a single chassis. Cost-savings are also enjoyed in comparison with other systems, especially over traditional individual rack-mounted components.

L-3's TT&CPS, called NETstar™, can be expanded greatly when users take advantage of the system's software functionality. The system has complete decommutation capabilities, full CCSDS processing, data processing power, a wide variety of data displays and archiving tools, distribution of data to remote sites via a remote access server (RAS), remote control / setup / status abilities over a network, and interfacing to commanding software. NETstar can also be made available with PC cards to provide RF up- and down-conversion at various frequencies.