PERFORMANCE EVALUATION METHODS FOR PCM BIT SYNCHRONIZER/SIGNAL CONDITIONERS

B. PEAVEY
NASA-Goddard Space Flight Center
Greenbelt, Maryland

Summary PCM Bit Synchronizer/Signal Conditioners (BSSC) possess 3 basic performance characteristics[1] which directly affect the processing of PCM telemetry data. These characteristics are: bit error rate (BER), bit slippage rate (BSR), and bit sync acquisition (BSA). This paper describes proven methods to meaningfully, and accurately measure these characteristics with particular emphasis on BSR and BSA. These methods require relatively simple and inexpensive procedures and instrumentation, and could be used by manufacturers and users to evaluate and acceptance test BSSC. The basic principle employed in these methods is "fixed threshold frame synchronization" with a unique strategy. Thus, there is no requirement for bit delay between the reference and BSSC output data, and synchronization of the reference data in the comparator with the BSSC output data takes place automatically. Moreover, this approach to testing BSSC represents the actual situation in which the BSSC would be operating as part of the telemetry data system, and hence would provide a direct measure of system performance. In actual application, these methods proved to be very effective and accurate for input SNR of $E_b/N_0 > O$ dB, and slightly less accurate for $E_b/N_0 < O$ dB (data having more than 10% errors). In general, BSA and BSR measurement accuracies of 20-30 bits can be achieved. A detailed discussion of accuracy is presented in the paper. In addition, the BSR and BER measurement methods are applicable to assessing the performance of tape recorders (TR) as it affects the actual system performance, rather than just the peculiar TR characteristics of TBE (time base error), bit dropout, and wow and flutter.

Introduction PCM telemetry systems which receive raw demodulated (from carrier or subcarrier) signals and process them to extract the telemetered information (telemetry data) employ BSSC as the "front end" or the first stage in the system. As such, the BSSC is almost entirely responsible for the overall system performance, assuming that an optimum frame synchronizer is used, which is characterized by BER and data recovery (DR). Data recovery is directly affected by BSA and BSR, where BSR includes both frequency tracking and phase lock. In other words, BSR is the effect of loss of bit synchronization either due to the BSSC' s inability to track the changing bit rate or to maintain proper phase due to noise and jitter (Δf, f_m present in the signal. Thus,

measurement of BSA and BSR completely determines how much data can be recovered from a given signal, whereas BER is the measured bit error rate of the recovered data.

Although adequate attention has been given to BER measurement, BSA and BSR have not been dealt with to a satisfactory degree by either manufacturers or users of BSSC. To mention 2 extremes of simplicity and sophistication, neither of which is recommended, one could use a stop watch and oscilloscope, and observe the time that the BSSC requires to establish bit rate and phase with respect to the reference clock to measure BSA, and observe the time during which bit synchronization was maintained to measure BSR. On the other hand, one could design instrumentation to automatically sense frequency and phase of the BSSC clock and, by using the reference clock, record the respective times (in bits) required to establish bit sync, and during which bit sync was maintained--a complex piece of instrumentation indeed. Though both methods examine the BSSC clock, the first is very inaccurate and tedious, while the second is too complex.

The purpose of this paper is to present simple and effective methods to measure BSA and BSR and, as a side benefit inherent in these methods, point out that a much simpler technique than is presently used to measure BER can be employed without any measurable difference in accuracy. The application of these methods to measure TR performance is discussed also. It is suggested that the BSA and BSR measurement techniques be adopted as a standard procedure for evaluating and acceptance testing of BSSC.

The discussion of the subject is presented in 5 sections entitled: Principle of Methods, Implementation of Methods, Application of Methods, Application of Methods to Testing TR, and Application of Methods to PCM System Performance Monitoring. The first section describes the basic principle on which the methods are based and why the “fixed threshold” approach is appropriate for this application. The second section discusses several possible implementations and attendant accuracies. The third section describes the actual operation and results obtained on various BSSC. The fourth section treats the TR application. The last section suggests a possible adaptation of these methods to monitor system performance of PCM telemetry processors.

Principle of Methods The basic principle of the BSA and BSR measurement methods is the fixed threshold frame synchronization with a unique strategy for acquisition and maintenance of frame sync (FS), and an appropriately chosen frame sync code (FSC) in the reference data. Since BSA and BSR are really characteristics of the BSSC clock, one might question the seemingly indirect approach of using frame synchronization as a measure of bit synchronization. Actually, the BSSC clock is indeed being tested, since it is responsible for achieving and maintaining frame sync as shown in Fig. 2. Although frame sync detection is based on successful correlation of the FSC mask with the incoming data, this cannot be accomplished before the BSSC has acquired bit sync.

Similarly, frame sync cannot be maintained in the absence of bit synchronization. Thus, it is seen that, in principle at least, a measure of time (in bits) required to achieve frame sync, and a measure of time between frame sync losses can yield BSA and BSR, respectively.

Of course, in order to provide unambiguous and accurate measurements, the frame synchronizer must not introduce any measurement errors in terms of prolonged frame sync acquisition time or false frame sync loss. Exhaustive tests have shown that by using an appropriate strategy and FSC such errors are completely eliminated for SNR > O dB (E_b/N_0), and are minimized to a negligible degree for SNR < OdB. It should be mentioned that no attempt was made to validate this approach for SNR < -3dB (expected BER of 18%-20%). Tests have shown that by using “random-like” FSC patterns of 20 bits or longer, and allowing between 5%- 10% bit errors in search mode and 30%-40% bit errors in lock mode, true frame sync can be achieved and maintained without verification. Again, for SNR > OdB, frame sync can be acquired within 1 frame better than 90% of the time, and practically all the time for SNR > 3 dB. It takes, on the average, 2 frames to acquire frame sync for SNR < O dB, with 1 FS used for verification (2 consecutive hits or misses), to correctly establish and maintain frame sync better than 99.99% of the time. Actually, no false acquisition or loss was ever observed inthese exhaustive (billions of bits) tests using the strategy described above. Now, it should be stated that the BSSC used in these tests operated within 1 dB of the optimum curve. Thus, in the preceding discussion of strategy and performance vs SNR, it was assumed that the BSSC under test would have a similar BER vs SNR performance. In fact, it might be more appropriate to talk in terms of expected BER rather than SNR as far as frame synchronization is concerned.

The results of those tests proved conclusively that frame sync loss was due to bit slippage, or loss of bit sync, and therefore BSR could be determined on this basis. The accuracy of BSA and BSR measurement depends solely on the reference data frame length, L, as shown in Fig. 1. It turns out that the BSSC tested were not sensitive to L, and no difference in performance was observed between L = 24 bits and L = 2048 bits. This indicates that an accuracy of 24-48 bits can be achieved. This is further discussed in the following section.

It should be observed that this method of testing BSA and BSR requires no delay adjustment of any kind, no alignment of signals, no measuring devices other than counters. It is not frequency sensitive (up to 50 MHz bit rate is within the state of the art) and, above all, does not require access to internal circuits such as PLL error voltage. The measurements directly characterize the performance as it applies to actual system operation without the need for inference or interpretation of the test data. Of course, BSA and BSR measurements are average quantities, and as such require many samples

of observation. However, as discussed later, this can be accomplished automatically, and it depends merely on the implementation method.

Implementation of Methods There are several ways in which the BSA and BSR measurement methods can be implemented. A general implementation scheme is shown in Fig. 3. For BSA measurement, the required counter inputs are the reference data frame or bit rate (depending on whether one wishes to count in terms of frames or bits), and the number of samples (observations, tries, etc.). The frame rate is generated by the simulator and it is the same as that applied to the BSSC under test. This frame rate is gated with the gate control (GC) level which is the same for controlling the signal input to the BSSC. This gating function enables one to produce the desired number of test samples in order to obtain an average measurement of BSA. The sample count (input to the T counter) is actually generated by the frame sync detector (FSD) each time the BSSC input signal is inhibited by the GC level, since the frame synchronizer loses frame lock whenever this takes place. The gated frame rate is controlled by the FSD search/lock level so that the input to the E counter lasts only from the time Gate B is enabled to the time when LOCK is achieved (Gate C is disabled), which is the BSA time within 1 frame accuracy. Fig. 4 shows how these count pulses are derived. It is noted that the counters are operated in the "totalizing" mode in order to obtain more accurate results than having only one counter operate in the "ratio" mode.

The GC level for gates A and B can be generated either manually or automatically as one's time and patience may dictate. This level need not be generated at equal time intervals, therefore making the automatic implementation rather simple. Though Fig. 4 shows both signal and noise being inhibited, it is more realistic to suppress just the signal (data), as is the case in actual situations, and force the BSSC to acquire bit sync under this condition.

For BSR measurement, the T counter receives the same input as in the BSA case, however, the E counter counts the frames-in-lock (FL) pulses generated by the FSD. Thus, each time the BSSC loses bit sync the T counter receives I pulse as a result of the frame synchronizer having lost frame lock. In this measurement, the signal to the BSSC is not interrupted for the duration of the entire test. Again, the T and E counters continue to accumulate pulse counts to produce a reasonably large test sample depending on the anticipated BSR. The average measurement of BSR is then obtained from BSR = T/E. As for BSA, it is possible to use only one counter operating in the "ratio" mode to measure BSR at the expense of accuracy.

The frame synchronizer, as shown in Fig. 3, consists of a frame sync detector (FSD), frame sync code register, and frame sync strategy control. The frame synchronizer receives data and clock directly from the BSSC under test. The FSD establishes the frame sync window (1 bit wide), and correlates the FSC mask with the incoming data

under strategy control. Depending on the type of data simulator employed, e.g. stored program multiple frame length, single frame length, or pseudo random shift register type, the frame sync window is derived from a bits /frame counter, or directly from the PR shift register (since it has a recycling property). The strategy control is set up in accordance with the desired minimum SNR, or maximum expected BER from the BSSC. Thus, considering BER < 5%, the allowed bit errors are: E_s = 5%-8% (to the nearest bit) and E_L = 30%-40% of the FSC. For example, assuming a 24 bit FSC, E_s would be 1 or 2 bits and E_L would be 8 bits. No verification would be required in either search or lock mode. This means that frame sync will be acquired or lost on the first hit or miss, respectively. For BER between 5% and 15% E_s would be 2 bits, E_L would be 9 bits, and verification of 1 hit or miss would be required. For practical reasons, however, cases of BER > 5% seldom arise. In fact, in presence of jitter, the BSSC hardly functions at SNR < 6 dB, or BER > 0.2%! Of course, the FSD automatically selects E_s or E_L based on whether it is in the search or lock mode, respectively.

The simulator consists of a data generator and appropriate perturbation generators such as noise, jitter, baseline, and amplitude modulation. The data generator may produce low transition density data, prefiltered waveform, or any other desired distortions to simulate the anticipated signal conditions. Except for lack of control of transition density, the data generator can be a very simple device such as a PR shift register connected in a maximal length manner to produce sequences of 2^n -1 bits, where n is the number of register stages. However, regardless of what type generator is employed, the data format must be as shown in Fig. 1.

To perform BSA and BSR measurements the bit comparator shown in Fig. 2 is not required. It is a simple matter, however, to extend the capability of this implementation in order to measure BER also. In fact, by using a PR data generator (shift register) in the simulator and an identical generator for the bit comparator, a rather simple and effective method for measuring BER is provided. Thus in one fell swoop, all 3 characteristics, viz., BSA, BSR, and BER can be measured with the same basic device and 2 counters (or one in the ratio mode). The bit comparator implementation is shown in Fig. 5. The n-stage shift register is an exact replica of the data generator in the simulator, and it serves the purpose of generating reference data. This reference data generator (RDG) operates in conjunction with the frame synchronizer which provides the control signals (LOCK and SEARCH) for synchronizing the RDG with the BSSC output data. The START control is used only to initialize the RDG after the power is turned ON. From that point on the RDG is initialized (preset) automatically by the Search signal. The RDG is preset to the n-bit pattern which follows the 24-bit pattern selected for the frame sync code (assuming that the FSC was chosen to be 24 bits long, however, it can be longer or shorter as the user desires). An illustration of this is given in Fig. 6. As an example, a 10 stage SR is used to generate repetitive sequences of 1023 bits. The output is taken from the 10th stage, and the feedback is derived from stages 3 and 10 through an exclusive

OR (modulo 2 adder). Several SR states at sequential bit times (truth table) are shown in Fig. 6, in order to illustrate the presetting and synchronization procedure. If the FSC is chosen in the manner shown in Fig. 6 then, after achieving frame lock, the SR will have a pattern of "0001010111". This means that the output bit following the FSC will be due to this pattern. Therefore, under these specific conditions, the SR must be preset so that the aforementioned pattern is contained therein. Now, each time frame sync is lost and the FSD generates a Search pulse, the SR is forced to assume that state. No shift pulses occur until the FSD acquires frame sync and the LOCK signal is generated. At this point, the BSSC output data, because it is supplied by an identical SR configuration in the simulator, will be synchronous with that of the RDG regardless of the amount of delay in the BSSC. The LOCK signal enables the shift pulse gate, and the BSSC data is compared bit for bit with the RDG output, as shown in Fig. 5.

Although used as an example, the SR configuration shown in Fig. 6, including the FSC, is indeed valid for actual application, if one wishes to use a 1023 bit sequence. This length is certainly adequate for making BER measurements, however some consideration should be given to accuracy when BSA and BSR measurements are made with such a long sequence (or frame). With respect to BSA it should be noted that, depending on SNR, jitter, and transition density, BSSC can acquire bit sync within 100 to 3000 bits (See reference 1). Thus, if BSA of less than 1000 bits is of interest, it is clear that L = 1023 is too long, and a much shorter frame length, say 31 or 15, is required if a reasonable accuracy is to be achieved. Assuming L = 31 (2^5 - 1) is used, the inherent accuracy of the measurement as recorded by the counters will be 31 bits. Therefore, if the measured BSA for certain signal conditions is 500 bits the attendant accuracy is (31/500) x 100, or roughly 6%. This means that the minimum BSA might have been 500-31 = 469 bits rather than the measured 500 bits. In general, BSA accuracy can be expressed as L/E/T, or in per cent as 100LT/E%, where L, E, and T are defined as shown in Figs. 1, 2, and 3.

With respect to BSR, however, L need not be as short as for BSA. This can be seen by considering the BSR of interest to be, say 10^{-4} bits or less (not unusual for SNR < 10 dB and jitter of $\Delta f \pm 1$ % at f_m. = 1 %)! If L = 1023 bits, and the measured BSR = 10^{-4}, the actual BSR might have been 1/10,000-1023), or roughly 1/9,000, a small difference indeed. Thus, the BSR measurement accuracy in this case turns out to be 0.1 or 10%. Admittedly, a BSR of 10^{-4} is quite severe for data recovery and is not likely to be acceptable. For lower BSR, say 10^{-5} or 10^{-6} ,the accuracy is considerably better, viz., 1% or 0.1%, respectively. Of course, even for BSR 10^{-4} ,the accuracy can be improved by an order of magnitude by choosing L 63. The BSR accuracy can be expressed in terms of

$$\left(1\Big/\left[(E/T-L)\right]\right) - (1/E/T) = T\left(\frac{1}{E-LT} - \frac{1}{E}\right) \times 100\% .$$

The preceding discussion points out that by implementing a 10 stage SR to produce either L = 31 or L = 1023, both in the simulator and comparator, the capability to measure BSA, BSR, and BER with the described accuracies can be provided. In fact, if only a 5 stage register is used, and the appropriate FSC is chosen, then the implementation will be greatly simplified at no loss in accuracy, and L = 31 will be applicable to all 3 characteristics. The advantage of using a short L will also be observed when this method is applied to testing tape recorders.

Application of Methods As mentioned previously, the primary purpose of developing these methods was to measure BSA and BSR of BSSC. BSSC performance characteristics presented in reference 1 were indeed obtained by using these methods. Presently, instrumentation employing these methods is used to evaluate and acceptance test BSSC at Goddard Space Flight Center (GSFC). In addition, they provide a means for checking out telemetry links, including spacecraft and ground tape recorders, communication channels, receivers, demodulator s and coders, all from a system' s point of view. This is so because it is the quantity and quality of the transmitted data through the "system" which is of greatest importance to the user.

In applying these methods to the measurement of BSA and BSR, it is important to keep in mind the desired accuracy, and the expected range of BSSC performance. For instance, if the expected BSA is not to exceed 10 bits, then the BSA method cannot be applied successfully. On the other hand, if a system is known to operate with a 10 bit BSA then it need not be tested, for in most applications a 10 bit BSA is not critical (as compared with 3000, bits !). The BSA method described in this paper is recommended for use only if the expected BSA may exceed 30 bits. This, one may rest assured, will happen when the telemetry signal is disturbed by noise, jitter and waveform distortion. Some BSA values are given in Table 1, and BSR values are given in Table 2. These measurements were made with simulated data from a stored program simulator to which noise and jitter were added in accordance with definitions given in reference 1. It should be pointed out that the user must decide what input signal characteristics are of interest to him, for which the BSSC performance characteristics, viz., BSA, BSR, and BER are desired. As far as BSR and BER measurements are concerned, there is no reservation as to applicability of these methods in all practical situations.

A direct consequence of measuring BSA and BSR is the assessment of data recovery (DR). The amount of data which can be recovered under given signal conditions may be estimated in the following manner. First, a BSA measurement is made. Then the BSR measurement is made, preserving both E and T counts. DR in per cent is then expressed in terms of

$$\frac{E \times 100\%}{E + T(BSA) + T} \qquad \text{or} \qquad DR\% = \frac{100\,E}{E + T(1 + \overline{BSA})},$$

where E is the number of frames-in-lock, T is the number of frame sync misses, and BSA is given in integral frames. Because the telemetry data is framed, the minimum BSA = 1. Therefore, in the optimum case,

$$DR = \frac{100\ E}{E + 2T}\ \%$$

Note, if T = 0, DR = 100% which is perfect recovery. This method of DR assessment was verified both under controlled conditions, where the exact amount of transmitted data was known, and by applying it to an actual satellite tape where the amount of recorded data was established on the basis of the recorded start and stop times. In the simulated case, the assessment was within 1%, whereas for the satellite tape it was within 10%. The 10% difference was, at least in part, attributable to the uncertainty of the actual time of recording, and to the greatly varying signal conditions on that particular tape.

Application of Methods to Testing Tape Recorders The following discussion is intended to demonstrate the applicability of BSR and BER methods to testing tape recorders with respect to bit dropout and effective jitter due to inherent time base error (TBE), as it might affect system performance. This method is not suggested to replace existing methods for measuring TBE, rather, it is recommended for the purpose of making a direct assessment of performance as the tape recorder is operated in conjunction with BSSC. Knowing the performance characteristics of a given BSSC, it is possible to directly determine the additional degradation of performance, if any, due to this tape recorder. This is accomplished by recording simulated data on the tape recorder, playing it back into the BSSC, and measuring the BSR and BER. The test setup is shown in Fig. 7. Noise free data in any desired code, e.g. NRZ-L or SP-L, is generated by the simulator (5 stage SR) and recorded on tape. This tape is played back into the BSSC having 2 or 3 PLL's to accommodate the expected amounts of jitter due to the TR. For minimum jitter, the narrow (0.1- 0.3%) PLL is selected, and BER and BSR measurements are made. Since every data bit is checked while the system is in frame lock bit dropouts occurring in bursts of less than 10 bits (30% of the 31 bit FSC) will be detected as errors, while bursts of more than 10 bits will cause frame sync misses. If the TR produces excessive jitter, the BSSC will lose bit sync which will be recorded by the T counter. Actually, the T counter does not distinguish between burst errors and excessive jitter, however, the observer can differentiate between them because the burst errors would occur much less frequently than the deleterious jitter. Bit errors due to amplitude or phase distortion would, in general, occur in a much more dispersed manner than burst errors and, therefore can be observed. It should be noted, however, that regardless of what caused the bit errors or bit slippage, this method will detect their occurrence and, thus, provide a measure of TR performance which is most meaningful from a system's point of view. It can be seen in this application that the data frame

length should be short, and preferably the same as the FSC, i.e., the data would indeed be comprised of the FSC only, and it would be 31 bits long, as shown in Fig. 7.

Use was made of these methods to identify malfunctioning tape recorders, as well as to evaluate their performance, with unqualified success. Again, performance was measured in terms of BSR and BER for various speeds, data codes, bit densities, and signal waveforms. For example, one of the tests indicated that when the tape was played back at higher speeds (60 ips and 120 ips) the BSR was slightly increased, which resulted in lower data recovery. Another test showed that the jitter (wow and flutter) in a properly functioning instrumentation TR, such as Ampex 600 or 1600, is insignificant, so that a narrow (0.1%- 0.3%) BSSC PLL can be used to provide the best SNR vs BER performance. In general, it should be realized that, regardless of the various signal conditions and TR modes of operation, the unique and meaningful performance characteristics of TR are BER and DR (data recovery) or BSR, as far as telemetry data processing is concerned.

Application of Methods to System Performance Monitoring This section presents a brief discussion of how the BSA, BSR, and BER measurement methods could be used to monitor the performance of PCM telemetry data handling systems. A simplified block diagram of the required instrumentation is shown in Fig. 8. The frame synchronizer operates in the same manner as discussed previously. It should be capable of accepting various FSC patterns up to K bits long (where $K \leq 32$ bits in most applications which use data formats shown in Fig. 1). Data and clock are provided by the system BSSC under normal operation. In order to accommodate various frame lengths a bits/frame counter is included to establish the frame sync window (1 bit). BSR is measured directly by counting frame sync misses and frames-in-lock (FL). To measure BER, a slightly different approach is used than described before. Here, because the only data which can be used for reference is the FSC, a special SR is provided to shift out the frame sync bit errors. These FS bit errors are loaded into the SR in parallel each time FS is detected (once per frame). This takes place in one bit time, and in coincidence with the FS window. The shift pulse, which is derived from the clock, is enabled immediately following FS detection, and it is stopped at the end of each frame. Thus, all bit errors, which are loaded as 1’s into the SR, are shifted out and counted during the first K bit times. Following this, the SR is cleared automatically by shifting 0’s through all stages (note the ground connection in Fig. 8). The BER obtained in this manner is, of course, based on the FSC sample. However, if the signal remains stationary, i.e., the SNR does not vary rapidly, the BER so obtained is equally applicable to the entire data.

It should be recognized that a separate construction of the Frame Synchronizer is not needed if an identical one is used in the system proper. Whatever the case, it can be seen that the BSR and BER measurement methods can indeed be used to monitor system

performance. It should be observed, however, that since T is given in terms of number of frames, the actual BER = E/TK, where K is the frame sync code length.

Conclusions This paper described methods to measure BSSC performance characteristics in a direct, accurate, and simplified manner. These methods were shown to be applicable to testing tape recorders, and monitoring telemetry system performance as well. The required instrumentation and operational procedures to implement these methods are straightforward, and are independent of data bit rate, or the particular equipment under test. These methods treat the subject equipment as a "black box", examining the "black box" output only, without recourse to the internal circuits or signals. The simulator was shown to consist of a 31 bit sequence generator, which was proven to be sufficient for generating data having random transition density in actual applications. It is recommended that these methods be exploited for the various applications described herein.

References

1. B. Peavey, "Performance Characteristics and Specification of PCM Bit Synchronizer/Signal Conditioners", Proceedings of ITC/68.

2. T. LoCasale and R. Margraff, "Specifying PCM Telemetry Decommutation Systems", ISA Instrumentation Conference, November 18, 1969, Cape Canaveral, Florida.

Table 1. -BSA vs. SNR

E_b/No (dB)	$\overline{BSA}$ (bits)	Notes:
15	50	1. Signal = Split Phase
9	100	2. Noise = White Gaussian
7	150	3. Bit Rate = stable.
3	500	4. PLL = narrow (< 0.3%).
0	1000	5. Data = random.
-3	3000	6. Samples/measurement >10.
		7. Accuracy = 32 bits.

Table 2.-BSR vs. SNR + Jitter

(E_b/No) + $(\Delta f, f_m)$		$\overline{BSR}$ (bits)
(dB)	(% bit rate)	
7	±1.5, 0.5	3×10^{-5}
7	±0.5, 0.5	$<10^{-6}$
4	±0.5, 0.5	10^{-5}
7	±1.5, 1	$>10^{-3}$

Notes:

1. Jitter = sinusoidal
2. Data, signal, and noise = same as in Table 1.
3. Accuracy = 256 bits. This means that the $\overline{BSR} = 1/10^5$ was actually $1/(10^5 - 256)$.

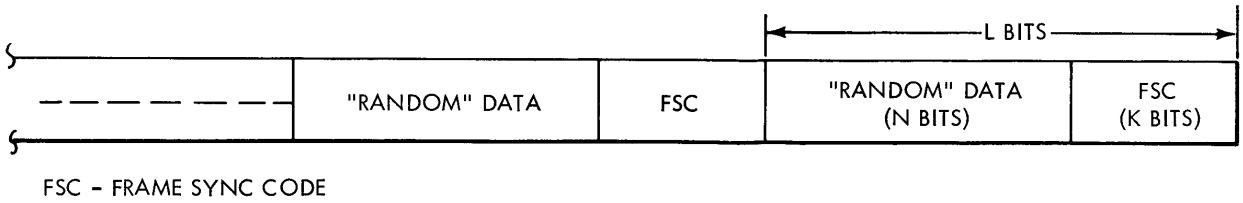

Fig. 1-Reference Data Format.

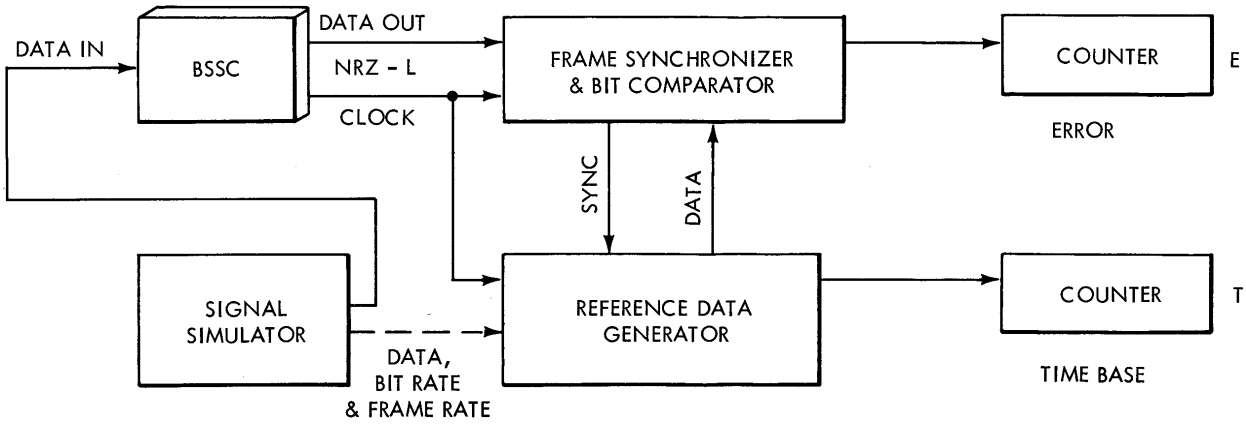

Fig. 2-Instrumentation Block Diagram.

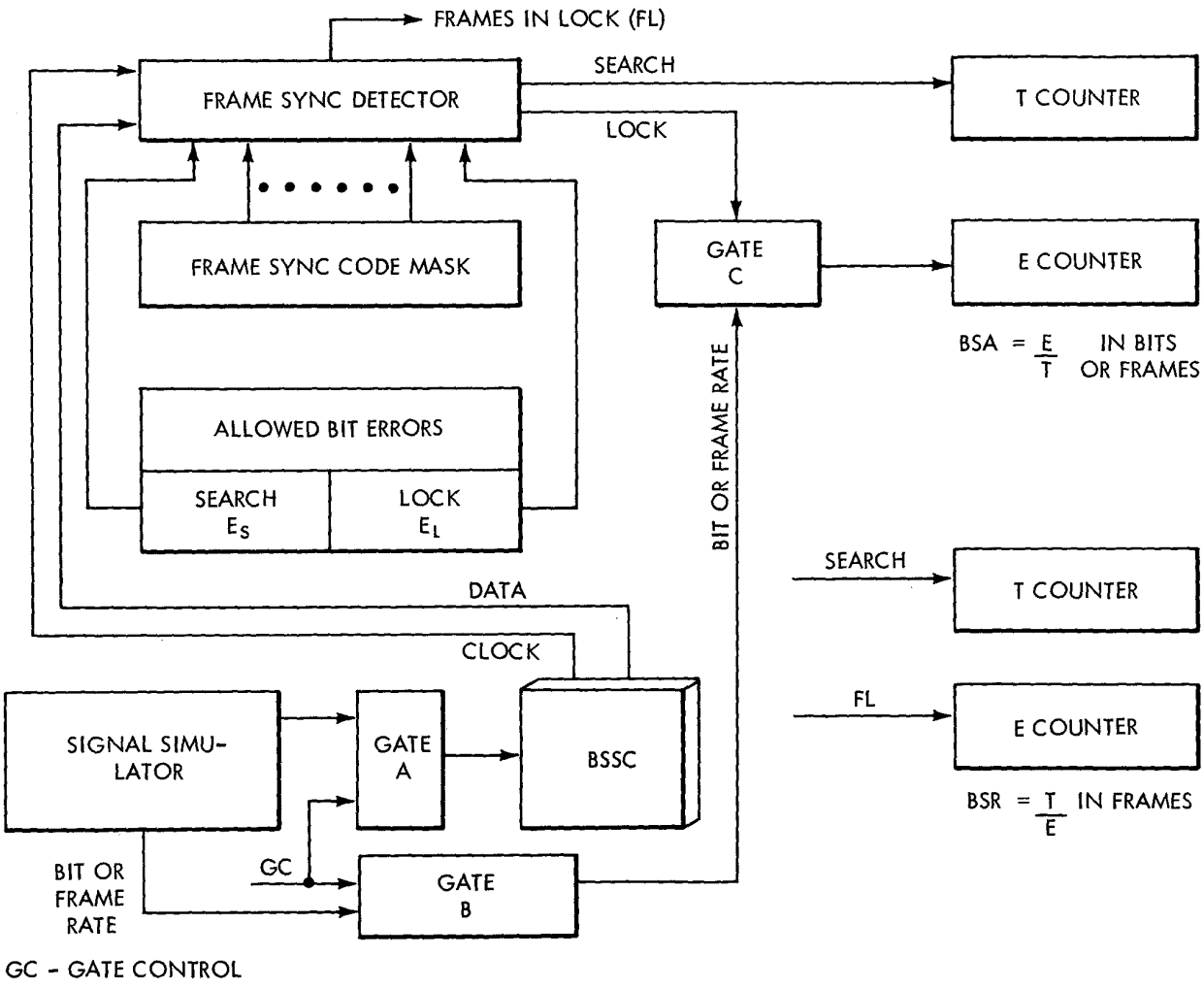

Fig. 3-Implementation of BSA & BSR Measurement.

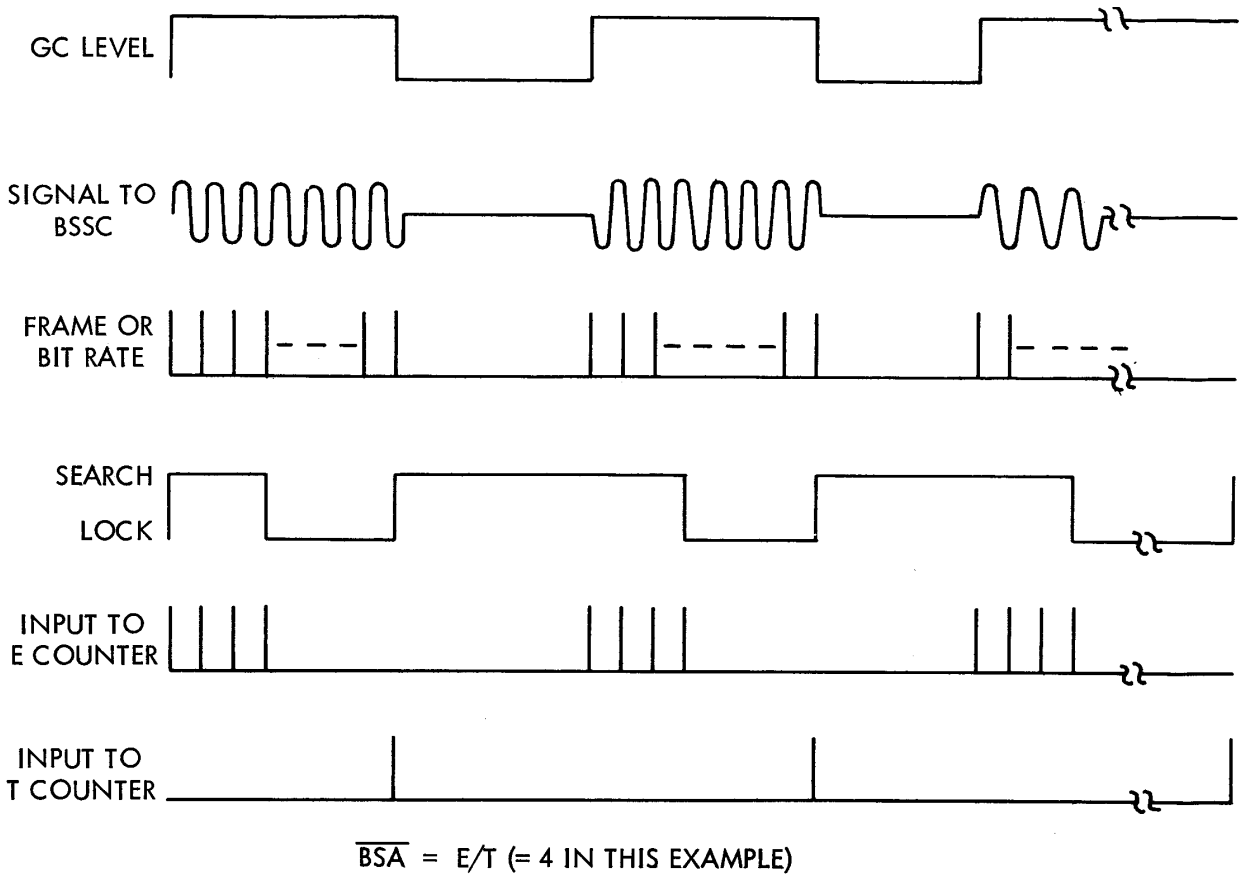

Fig. 4-BSA Measurement-Derivation of Counts.

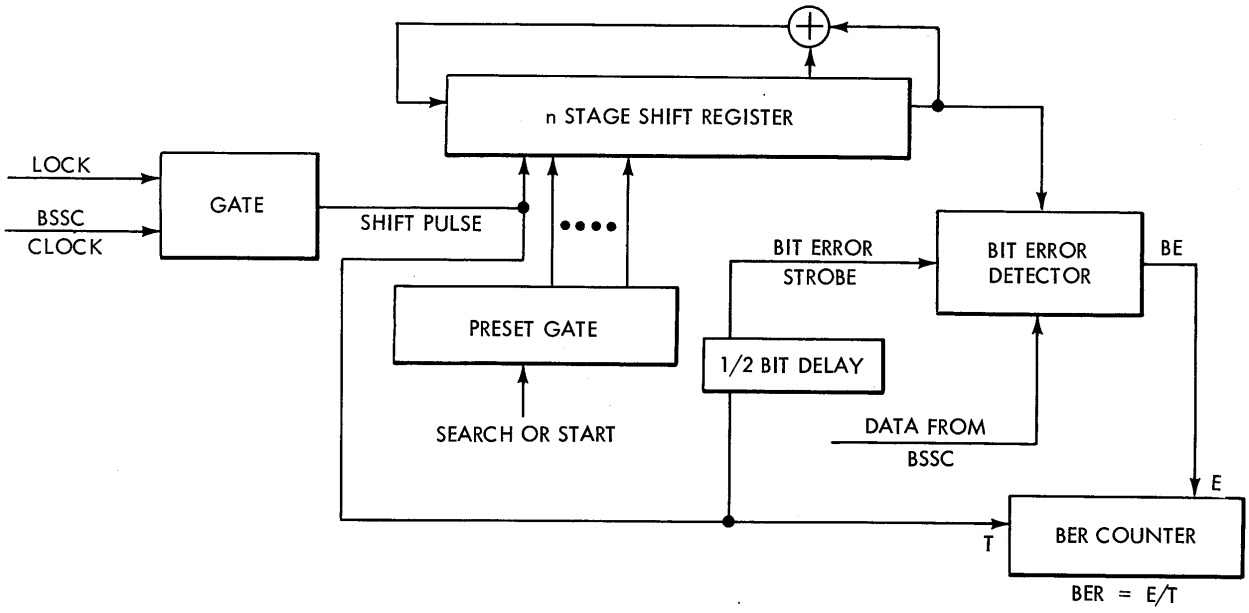

Fig. 5-Bit Comparator For BER Measurement.

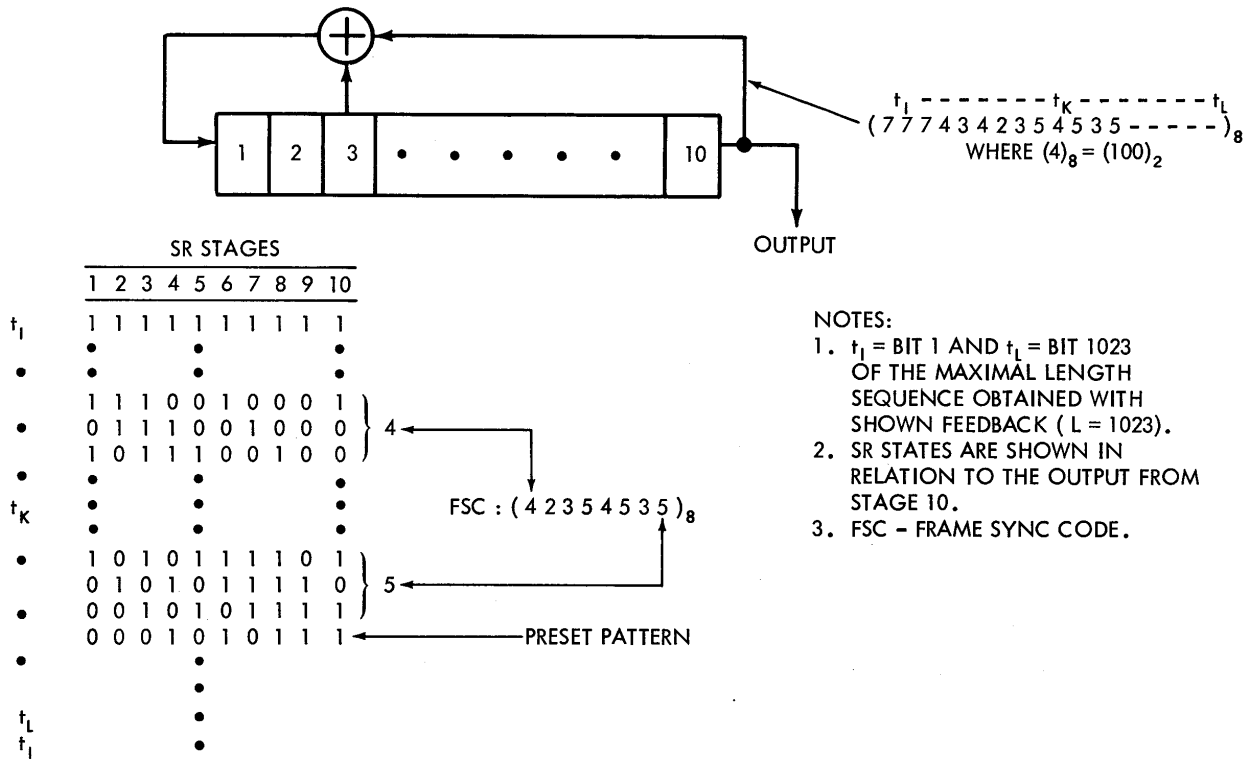

Fig. 6-Simulator and Reference Data Generator.

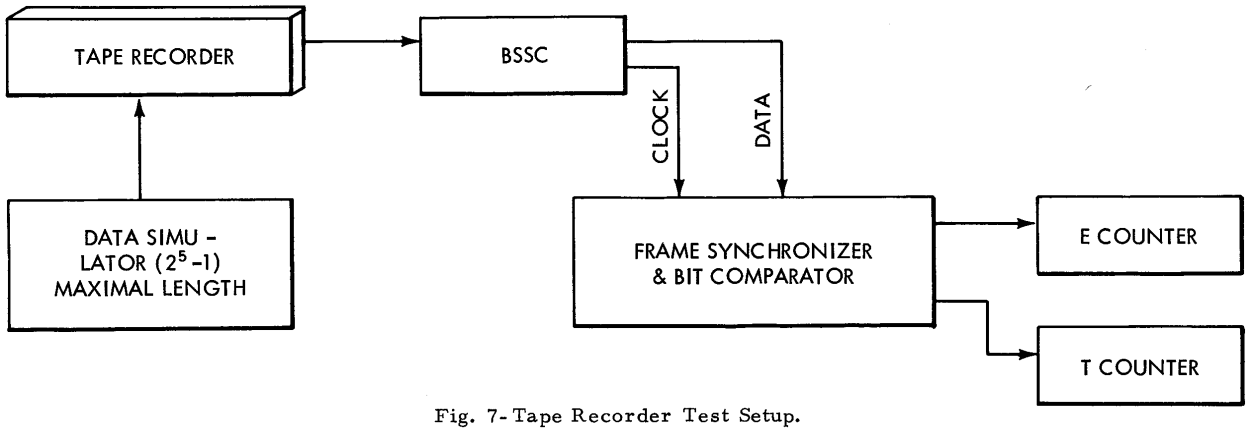

Fig. 7- Tape Recorder Test Setup.

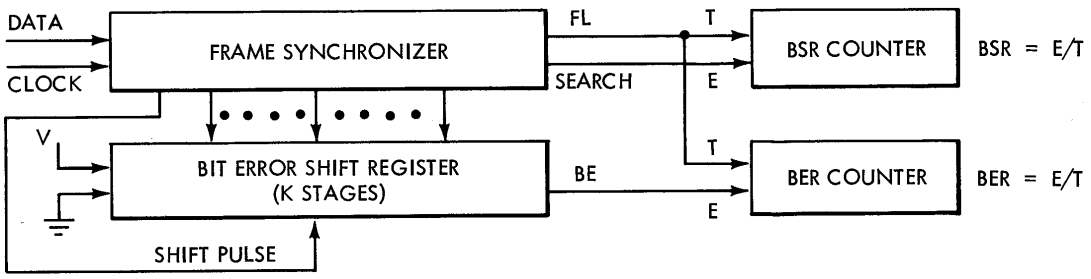

Fig. 8-System Performance Monitoring Setup.