HIGH DATA RATE CODING FOR THE SPACE STATION TELEMETRY LINKS

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Summary This paper summarizes a study of coding systems for high data rates with potential application to the space station telemetry links. Among the approaches considered were convolutional codes with sequential, Viterbi and cascaded Viterbi decoding. It was concluded that a high-speed (≈40 Mbps) sequential decoding system best satisfies the requirements for the assumed growth potential and specified constraints. Trade-off studies leading to this conclusion will be reviewed. Some sequential (Fano) algorithm improvements will be discussed as well as real-time simulation results.

Introduction Space station concept definition studies' have defined communication requirements for the basic Solar-Powered Space Station concept. The three major links of the external space station communication system are:

1) Space station - ground via relay satellite system link
2) Space station - ground via direct link
3) Space station - deployed experiment modules

The relay satellite was selected as a primary link to the ground with a direct link as back-up; the down-link transmission requirements consisted of:

1) One standard color television channel
2) Four voice quality channels
3) Telemetry and down-link data rate of 10 Mbps

In a more recent version of this space station concept, namely the Shuttle-Launched Modular Space Station[2] the down-link communication requirements are outlined and slightly reduced from the earlier version; however, the original data volume design point

was retained for the purpose of projected growth. In the space station concept definition studies' the experiment and systems telemetry data are PCM; however, the voice and TV channels were assumed analog. Other studies[3] have investigated in detail digitizing the TV and voice links with some redundancy elimination techniques for bandwidth reduction. Further efforts[4] provide a design for a baseline external communications system for the original 12-man space station concept using a time-division multiplexed (TDM) digital channel for the TV and PCM data. For this design the highest data rate is 20.2 Mbps for the space station-to-ground link via relay satellite.

System Constraints and Requirements To bound general coding system parameters, certain guidelines were established. The coding system must be capable of operating at data rates in the tens of Mbps range (greater than 20 Mbps) with a potential of growth to more than 50 Mbps. The time-division multiplexed channel will derive information from various sources, with varying speed and error rate requirements, and the coding system is expected to meet the demands of each information source. These bit-error-rate requirements may vary from 10^{-3} to 10^{-8} depending on the extent of source coding. As more onboard space station processing and redundancy elimination is accomplished, the error-rate requirements will decrease for larger portions of the data.

The allowable bandwidth expansion due to coding may be an important factor when operating at high data rates via a relay satellite. It is assumed that a bandwidth expansion factor of 2, or a code rate of 1/2, is the greatest expansion due to coding that can be tolerated. During the study, optimum rate 3/4 and 2/3 codes were found, and their performance was studied theoretically and by computer simulation. However, the channels currently considered do not appear to be so bandwidth-constrained that detailed implementation assessments of these high-rate codes are warranted. Due to the wide variety of information sources it is not feasible to use data format framing information as synchronization (as is done on Pioneer 9 and Pioneer F/G spacecrafts, for example) for blocking the data before encoding. Although synchronization information, necessary for coding, can be provided, it is most desirable to eliminate this requirement for the coding system. The decoder is required to perform necessary synchronization after acquisition of the transmitted signal and after bit detection. Specifically, the decoder must resolve the phase ambiguity and code node sync for binary phase shift keyed (BPSK) or quadriphase shift keyed (OPSK) modulated signals. The decoder is to monitor and measure system perforrnance and to detect link malfunction or unreliable link operation. In satisfying these general guidelines of requirements, three coding approaches are considered: convolutional coding with Viterbi decoding, cascaded Viterbi decoding, and sequential decoding.

Viterbi Decoding A performance and implementation study of the Viterbi decoding algorithm[5] was undertaken[6] to determine its feasibility for efficient communication at

data rates of 20-50 Mbps. The bit error rate performance of rate 1/2 Viterbi decoders, using 3-bit quantization, is shown in figure I for constraint lengths K = 4, 6, and 8.

As a result of numerous algorithm modifications and simplifications, involving in particular metric compression, add-compare-select logic optimization, metric overflow design, and memory storage minimization, several designs of a K = 4 decoder, operating at 40 Mbps with 3-bit quantization, were performed using alternate IC logic families. Important features of these implementations were the self-synchronization and the channel reliability monitoring capabilities of the decoder. Both capabilities are derived directly from the decoder metric behavior. No block or state synchronization is required since the algorithm automatically achieves this after decoding at most a few constraint lengths of data. On the other hand, incorrect symbol synchronization (one of two positions for code rate 1/2) and incorrect phase (180° ambiguity in a BPSK and 90° ambiguity in a QPSK system) will be detected as inordinately high metric increases with consequent overflows. These overflows are accumulated in an up-down counter that, upon its own overflow, causes a change in node or phase synchronization position. The decoder will continue the search until the metric overflow count ceases to rise. The metric overflow is also used to monitor performance, for the rate of overflow of a synchronized decoder is proportional to channel error rate.

The conclusion of the design study was that a 40 Mbps, K = 4, rate 1/2 decoder with 3-bit quantization is feasible using either four parallel 10 Mbps decoders employing TTL logic, or one decoder employing MECL II 1/2 logic. Introduction of the new MECL 10,000 high-speed MSI logic line appears to render a K = 5 decoder feasible at this data rate with a resulting efficiency improvement of nearly 0.5 dB. For bit error probabilities in the range of 10^{-3} to 10^{-5} , Viterbi decoders with 3 -bit quantization are competitive or superior to sequential decoders using hard (1-bit) quantization. However, the latter becomes preferable at error rates of 10^{-8} and below, as described in the section on sequential decoding.

Cascaded Viterbi Decoding For a single data stream consisting of several information sources of diverse origins, the data rates and channel bit error probability requirements may differ widely. Little or no data compression of real-time video-type data produces a large data volume for which bit error probabilities (P_B) as large as 10^{-3} are acceptable. On the other hand, some experiment data has required error rates of 10^{-6} or lower. A K = 4 Viterbi decoder requires about 2.5 dB more power to achieve a 10^{-6} bit error probability compared with 10^{-3}.

For this discussion, the data are classified into two categories: data type I with $P_B = 10^{-3}$ to 10^{-5} and bit rates of 10^7 to 10^8 bps; data type II with $P_B = 10^{-6}$ to 10^{-8} and bit rates of 10^4 to 10^6 bps. One method of more efficiently accommodating these data types[6] is to use cascaded coding (fig. 2). The basic high data-rate inner code will be assumed to be a

constraint length 4, rate 1/2 convolutional code with Viterbi decoding. The goal is to find an outer code for the low-rate data that can reduce the error probability to the required level. To avoid burst errors for the outer channel, interleaving can be introduced. Five constraint lengths (or 20 bits for K = 4) are quite adequate to achieve nearly independent errors. If the inner code has a rate R_I and the outer code a rate R_{II}, then the composite code rate is

$$R_T = R_I[(1 + x)/(1/R_{II} + x)]$$

where x is the ratio of the quantity of data of type I to data of type II. For example, with x = 10 and rate 1/2 inner and outer codes, the total code rate loss id 3.4 dB, where the 0.4 dB additional loss is due to the inner code. If x = 2 for the rate 1/2 codes, the composite rate loss is 4.25 dB. Thus the resulting required increase in overall E_b/N_o is 0.4 dB and 1.25 dB, respectively.

To evaluate specific outer codes it will be assumed that type I data requires $P_B = 10^{-3}$ and the lowest bit error probability that is needed for type II data is $P_B = 10^{-8}$. With inner decoder $P_B = 10^{-3}$, the two-error correcting and three-error correcting BCH codes (namely, the (I 5,7) and the Golay (24,12) codes) used as outer codes achieve a $P_B \approx 2.1 \text{ X } 10^{-7}$ and $P_B \approx 1.7\text{X } 10^{-9}$, respectively. The (15,7) code does not meet the requirement for $P_B = 10^{-8}$ and the (24,12) code requires a moderately complex decoder. In either case, block synchronization must also be implemented.

A more acceptable approach for the outer code is to use a very short constraint convolutional code. A two-error correcting, rate 1/2 convolutional code gives $P_B \approx 5\text{X}10^{-8}$, and the optimum three-error correcting, rate 1/2 code yields $P_B \approx 5.6\text{X } 10^{-10}$. These results for the binary symmetric channel (BSC) assume a Viterbi decoder that is simpler to implement than a decoder for the corresponding block codes. Further reduction of the decoder complexity can be achieved with only a moderate increase in P_B, if the outer Viterbi decoder is replaced by a feedback decoder, which is nearly optimum for the BSC.

Sequential Decoding While the cascaded decoding technique can provide very low error rates for a small fraction of the data without significantly reducing the overall efficiency, it is reasonable to provide for a growth potential to the point where half or more of the data requires bit error probabilities of the order of 10^{-8}. This situation will occur even for color television channels if truly sophisticated, practical, highly efficient data compression techniques become available. For this purpose, cascaded decoding becomes very inefficient, and in fact, the most economical approach is to design for very low bit-error probability for *all the data*.

With this goal in mind, the study[6] was directed toward a comparison of the efficiencies of the various convolutional decoders for data rates up to 50 Mbps and $P_B = 10^{-8}$. Sequential decoders exhibit very steep performance (P_B vs. E_b/N_o) curves, which render them less desirable at moderate to high P_B, but definitely superior at very low P_B .

In designing a sequential decoder for very high speed operation, one is quickly forced to limit the channel output quantization to two levels (one bit). The reasons for this are several, the two most important being: 1) since the computational effort is variable, several thousand branches of received quantized data must be stored; a fixed buffer size will allow storage of only one-third as many branches* if 3-bit quantization is used, causing a considerably higher overflow probability; 2) while Viterbi decoding is relatively insensitive to AGC variations,[6] a change of 10% in AGC will cause significant performance degradation in sequential decoding.

Computation effort is relatively insensitive to constraint length. Making K large assures a low probability of undetected error. Then the primary cause of errors is buffer overflows. The bit error probability due only to overflows is approximately

$$P_B \approx K(\mu B)^{-\alpha} \tag{2}$$

where μ is the speed factor (computation rate/data rate), B is the buffer size (in branches), α is the Pareto exponent and k is a constant which depends on the constraint length and the resynchronization strategy after overflow. Table 1 shows the measured Pareto exponent as well as the undetected bit error probability for a constraint length K = 37, rate 1/2 systematic code decoded by a Fano sequential decoder, operating on $8X10^6$ bits in each case, in real-time simulations.

Table 1. Measured Pareto exponent and undetected error probability for modified Fano sequential decoder operating on $8X\ 10^6$ bits

Eb/No, dB	Channel symbol error probability	α	P_B
4.7	0.043	0.97	$2.5X10^{-5}$
4.9	.039	1.12	$1.5X10^{-5}$
5.1	.035	1.29	0
5.5	.030	1.44	0
5.8	.025	1.66	0

* At low data rates, this reduced storage can be compensated for by increasing the computation speed, but at 50 Mbps data rates, only small speed factors are possible.

The Pareto exponent is essentially maximized using the Fano algorithm. However, the average number of computations per bit can be reduced by algorithm modifications, which are easily implemented. The effect of one such improvement, "modified quick threshold loosening," is shown in figure 3. The average number of computations per branch, $\bar{c}$, is reduced by almost one-third, although the Pareto exponent (asymptotic slope of the curve) is unchanged.

With this algorithm modification, a complete sequential decoder with K = 41 and rate 1/2 was designed for operation at 40 Mbps.[**] It employs a $64X10^3$ bit (branch) buffer and provides for a maximum computation rate of 10^8 computations per second resulting in a speed factor $\mu = 2.5$. This very high speed is achieved by using MECL III logic in the algorithm functions where speed is most critical. The remainder of the system uses MECL 10,000, MOS, and TTL logic. With this long constraint length the predominant source of errors is buffer overflow; complete system simulations with these parameters show that $P_B = 10^{-5}$ is achieved at $E_b/N_o \approx 5.2$ dB. Performance at the $P_B = 10^{-8}$ level appears to require approximately 1 dB more.

For sequential decoding, lack of symbol synchronization can be detected by observing the metric behavior just as for Viterbi decoding. Here the difference between metric threshold loosenings and tightenings (in the Fano algorithm) are counted. When this number exceeds the capacity of the counter, the symbol position is changed and resynchronization is initiated.[***] Also, as discussed in the section on Viterbi decoding, this number can be used during synchronized operation as a channel reliability parameter.

With sequential decoding, resynchronization must be initiated not only whenever incorrect symbol sync is detected but much more frequently, every time an overflow occurs. The "guess-and-restart" strategy' involves setting the syndrome to zero (corresponding to no information errors for a systematic code). If the guess was correct, or nearly so, the decoder ultimately arrives at the correct path. Otherwise, overflow recurs and a new guess-and-restart is initiated. This may cause the loss of several thousand branches. During this decoder failure period, the uncorrected information bits of the systematic code are output. However, since the channel error probability is less than 4%, only a few hundred bit errors will occur whenever overflow occurs. The combination of the above events results in the bit error probability expression of equation (2), with $K \approx 200$ in the range of E_b/N_o between 5 and 6 dB.

[**] It is being fabricated under Contract NAS2-6411.

[***] For Viterbi decoders operating on short constraint length codes, code resynchronization is automatic once the correct symbol sync is achieved.

For the decoder described, operation with speed factors as low as $\mu = 1.5$ will be possible, provided error requirements are relaxed or E_b/N_o is increased, resulting in potential data rates in excess of 60 Mbps. At a data rate of 40 Mbps, the coding gain of the sequential decoder is approximately 4.4 dB at $P_B = 10^{-5}$ and nearly 6 dB at $P_B = 10^{-8}$.

References

1. North American Rockwell, "Solar-Powered Space Station Definition, Volume III Subsystem Definition, Part 4, Information Subsystem," NAS9-9953, July 24, 1970.
2. North American Rockwell, "Shuttle-Launched Modular Space Station, Volume 1, Concept Definition," NAS9-9953, January 1971.
3. Robert B. Blizzard, "Potential Applications of Digital Techniques to Apollo Unified S-Band Communications System (Final Report)," NAS9-9852, Martin Marietta Corp., February 1970.
4. Dennis Eggert, John Godwin, and Frank Joyce, "Parametric Analysis of RF Communications and Tracking Systems for Manned Space Stations (Final Report)," NAS9-10409, Hughes Aircraft Co., January 1971.
5. A. J. Viterbi, "Error bounds for convolutional codes and an asymptotically optimum decoding algorithm," *IEEE Trans on Information Theory*, Vol. IT-1 3, April 1967.
6. Linkabit Corp., "Coding Systems Study for High Data Rate Telemetry Links (Final Report)," NAS2-6024, Ames Research Center, Moffett Field, Calif.
7. Codex Corp., "High Speed Sequential Decoder (Final Report)," DAA B07-69-C-005 1, U. S. Army Satellite Communication Agency, Ft. Monmouth, New Jerse , June 1969.

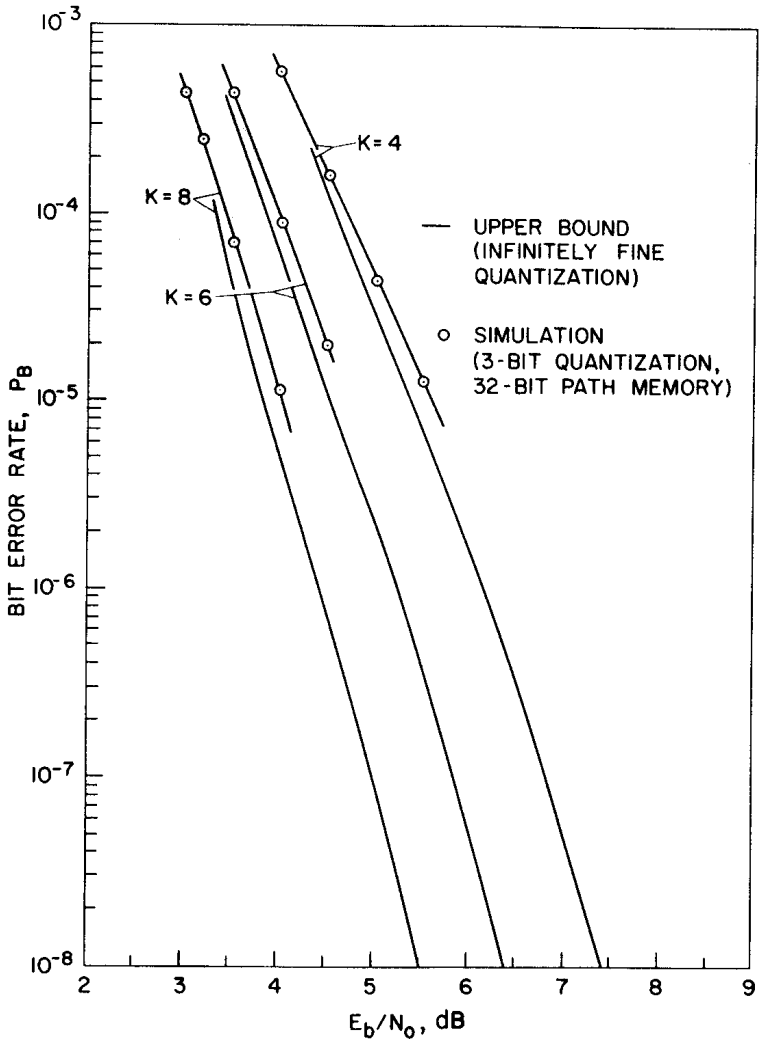

Fig. 1 - Bit Error Rate vs. E_b/N_o for Rate 1/2 Viterbi Decoding.

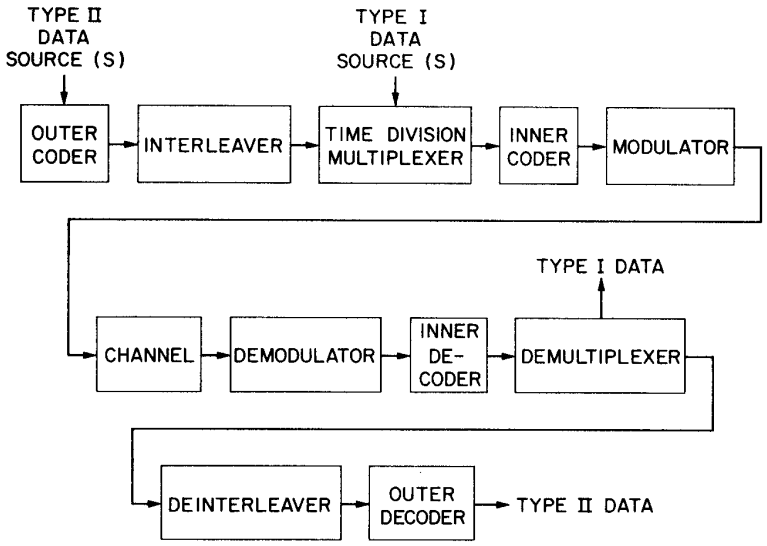

Fig. 2 - Coding for Data of Varying Error-Rate Requirements.

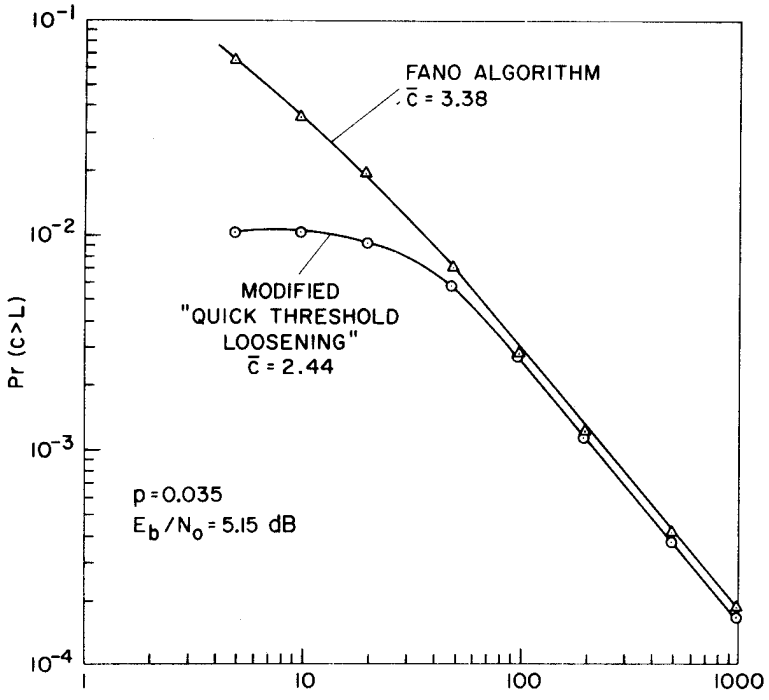

Fig. 3 - Distribution of Computation Comparison for the Standard Fano Algorithm and the Modified "Quick Threshold Loosening" Sequential Decoders.