A MULTISPECTRAL SCANNER DATA DECOMMUTATOR/ PROCESSOR FOR THE EARTH RESOURCES TECHNOLOGY SATELLITE

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Summary This paper describes the design of the telemetry decommutator/processor for multispectral scanner data to be returned by the first two Earth Resources Technology Satellites (ERTS). This unit, referred to as the Multispectral Scanner Tape Decommutator/processor (MSS TDP), is a versatile data handling system which accepts multipletrack tape inputs, providing output formats compatible with a multipletrack tape recorder or a single channel film recorder. The system is organized as a parallel processor, being capable of decommutating and formatting five spectral bands of digital video data. Synchronization and decommutation of skewed multiple-track data is performed with housekeeping and calibration data being transferred to a control computer. A six scan line buffer is asynchronously loaded and synchronously unloaded to remove data skew and reformat the video data. The unit includes a highspeed arithmetic processor which performs radiometric calibration of a single spectral band of video data prior to film recording. The primary function of the MSS TDP will be the processing of receiving site data tapes for conversion to film images.

Introduction Earth Resources spacecraft employing multispectral scanners (MSS) require data handling equipment which can process multiple spectral bands simultaneously with a high throughput rate. The MSS TDP has been developed to process multispectral data for the ERTS A and B spacecraft to be launched in 1972 and 1973. The TDP is an integral part of the NASA Data Processing Facility, Goddard Space Flight Center, which will handle all ERTS data. This unit processes tapes from STADAN receiving site Multispectral Scanner Video Tape Recorders (MSS VTR), providing inputs to an Electron Beam Recorder (EBR) or High Density Digital Tape (HDDT) unit.

The three modes of operation of this unit are as follows:

1. MSS VTR Tape to Film Conversion - Receiving site MSS VTR tapes are decommutated, and a single spectral band is reformatted into sequences of single scan lines for the EBR. The continuous strip data is divided into “framed” images for film recording and two processing operations may be performed on

the video data: (1) decompression of data which has been compressed onboard the spacecraft, (2) digital radiometric calibration of data using linear correction coefficients calculated by the control computer.

2. MSS VTR Tape to HDD Tape Conversion - MSS VTR tapes are decommutated, with all five spectral bands being simultaneously reformatted for recording on the HDDT unit. This HDD Tape is the primary medium for transfer of data between ERTS processing groups.

3. HDD Tape to Film Conversion - HDD Tapes are decommutated and a single spectral band is reformatted for inputting to the EBR.

Mode 1 is used to convert all MSS data to film for initial analysis. Data of interest may be converted to HDDT in mode 2, with these tapes being computer processed by other ERTS processing groups. Mode 3 is finally used to convert the processed HDDT to film images.

Multispectral Data Formats Figure 1 summarizes the flow of MSS data and the various formats in which it is presented. The MSS includes a scanning mirror which sweeps perpendicular to the satellite ground track, providing the ground image to an array of optical detectors. The MSS scans six lines for each mirror sweep, in each of four ERTS A spectral bands simultaneously. A fifth spectral band to be included on ERTS-B will have one-third the spatial resolution of bands 1-4, scanning two lines per mirror sweep. The spacecraft orbital velocity and mirror sweep rate are adjusted such that consecutive mirror sweeps represent information from adjacent swaths of the ground below.

The scanner analog detector output (A) is shown for a single scan line. The first portion of the sweep includes video data for the ground scan, while every other retrace includes a radiometric calibration wedge which continuously varies from white to black. The analog detector outputs are A/D converted into 6-bit bytes with additional digital codes being multiplexed into the format. The video data for each scan begins with a short Line Start Sync code (I byte) and is concluded with an 8-byte End Line Code. A BCD spacecraft time code is included which encodes each time code bit into I byte. Each line contains 1 byte of the code following line start sync, providing 24 BCD bits across 4 bands. (Two consecutive sweeps provide a complete 48 bit time code.) A 3 -byte binary line length code (LLC) is inserted following the end line code, providing a measure of the total number of picture elements in all scan lines of the sweep. A preamble consisting of an alternating one-zero pattern occurs at the conclusion of each retrace interval. Upon ground command, the video data for 3 bands may be passed through non-linear amplifiers, providing an optional signal compression mode.

The MSS multiplexes the multiple scan lines for all bands onto the 20 Mbps telemetry link. The receiving site demultiplexes the data and records it on the 28-track MSS VTR. The format (B) includes four groups of six tracks each, representing the four ERTS A spectral bands with each track allocated to a single scan line. The fifth spectral band is multiplexed onto a single tape track. This tape data is Miller encoded at a 10 Kbpi packing density. Record and playback speeds are 60 ips, resulting in a 0.6 Mbps data rate on all 25 tracks used for data. The HDDT format (C) provides a standard interface tape between all ERTS processing groups. The data is formatted with a single spectral band on each of 4 tracks, with the fifth band having quarter lines multiplexed on the 4 tracks.

General Description The MSS TDP is organized as a highly parallel digital system since it is required to simultaneously synchronize and decornmutate multiple inputs, while being capable of formatting and processing multiple outputs. The design is modular, consisting of 5 parallel data paths for the five ERTS B spectral bands. The block diagram in Figure 2 shows the parallel organization of the system. The TDP and all input/ output devices are controlled by a common control computer.

MSS VTR and HDDT Data Input Logic Separate data input assemblies are provided for accepting data from the MSS VTR and HDDT tape units since the tape formats, data rates, and number of tape tracks differ. The MSS VTR data decommutators acquire synchronization with the parallel data streams from the 25 tape tracks and strip off spacecraft time code, video data and calibration data. The time code and calibration data are transferred to the control computer while the video data is loaded into a buffer memory. The HDDT data decommutators likewise acquire synchronization with the data from the 4 tape tracks, stripping off frame identification codes and video data. The frame identification is transferred to the control computer and the video data is loaded into the buffer memory in the same format as for the MSS VTR input.

Figure 3 shows the tape data input logic for a single MSS high resolution spectral band (six tape tracks). The input logic units asynchronously acquire Line Start Sync and decommutate data from the six serial digital inputs under control of a common set of control logic. Data from each individual tape track is shifted into a 36 bit input shift register (1), with the first six bytes being compared by the sync correlator to detect line start sync. Once line start is detected, the data synchronizer counts bytes in the format, generating transfer clocks to decommutate the various data from the format. The time code byte is shifted into a register and a major ity voter decodes the byte into the single BCD time code bit. Video data is shifted into the I register, assembling the data for transfer to the buffer memory. Once a 36 bit word is accumulated it is strobed into the transfer register, M, and the group memory address programmer is requested to transfer the data to the buffer memory. The memory address programmer services the 6 tracks at random since the data is skewed. The MSS VTR data rate provides 6 data ready requests

every 60 microseconds, requiring a buffer clear-write cycle time of less than 10 microseconds.

The data synchronizer for each track enables a cal detector to search for the calibration wedge when the transfer of video data is completed. Once the black-to-white transition preceding the wedge is detected, a cal byte counter is enabled to count the bytes in the wedge. Six samples are then decommutated from the wedge by enabling the six bytes to be shifted into the I register in order. The location of these six samples within the wedge are predetermined for each sensor, and are wire-wrap “programmed” into the cal decommutator gate network. Once the 6 cal samples are assembled, the memory address programmer is again requested to transfer the data to the memory. In the case of the cal word, the 36 bits are transferred to the buffer memory (for formatting on the HDDT) or to the Data Transfer Interface (for transferring to computer).

The technique for acquiring synchronization with each sweep is based on the following considerations: (1) Verification of preamble permits the line start search to begin. (Probability of false acquisition in preamble is small.) (2) The maximum expected data skew (due to tape skew) defines a period of time in which all tracks should acquire line start. This period can be used to correlate line start acquisition across tracks - providing verification of line start sync. (3) The probability of false sync acquisition in video data and cal data is significant since the 6 tracks represent spatially parallel data (adjacent tracks have a high probability of containing identical data). This group synchronization technique provides reliable acquisition and verification of the short (6 bit) line start sync word by using the format preamble and cross-track correlation of line start acquisition.

The control of each group of six tracks is accomplished by the group synchronizer and memory address programmer. The state transition diagram for the 6 track group synchronizer is shown in Figure 4. The states of the synchronizer describe the sync procedure and are as follows:

(1) Preamble Search: A single track is searched for verification of the alternating 101010 --- preamble upon receipt of a begin preamble search command (this occurs each sweep) from the Central Timing and Control, (CTC).

(2) Search Mode 1: All tracks search for the single line start sync byte.

(3) Search Modes 2 & 3: One or two (respectively) tracks have acquired line start and are decommutating data, all other tracks searching for line start.

(4) Partial Sync: The first track in sync has counted n bytes after line start (i.e. n is the maximum tolerable number of data bytes due to tape skew) and all tracks have not acquired line start. Line start search is disabled on all tracks.

(5) Full Sync: All tracks have acquired line start prior to the n^{th} byte on the first track in sync.

The line length code (LLC) is decommutated by the group synchronizer from a single track which has correctly acquired line start sync. The 18 bit LLC is transferred to a holding register, and the CTC is issued a LLC ready flag. Each spectral band input logic group decommutates the LLC, and a bit-by-bit majority voter located in the CTC provides the LLC value which is transferred to the control computer.

The memory address programmer loads data from the 6 tracks into six sectors in the buffer memory. An individual address counter is required for each track to provide the sector address for loading the assembled video data into memory. As an individual track input indicates that data is ready, the programmer enables the T-register data for that track and the appropriate address to be gated to the memory inputs. Once the memory write cycle is completed, the address counter is incremented and the programmer is ready to service any other track that has data ready for loading.

Data Transfer Interface This logic provides an interface with the control computer for the transfer of data which has been decommutated by the input logic. Table 1 summarizes the data which is transferred across this interface.

All data transfers to the computer are preceded by a specific data ready interrupt. The DTI provides holding registers for all data to permit the computer to accept data asynchronously (with respect to operations.)

Table 1 - Data Transferred to Control Computer

Data Transfer	Mode	Rate of Transfer	Use by Control Computer
Time Code	1,2	Once per Sweep	Used to relate mirror sweep time to other sensor data for partitioning data into frames.
Calibration Data	1	Once per 2 Sweeps	Used to calculate gain and offset corrections for radiometric calibration.
Line Length Code	1,2	Once per Sweep	Used to compute the number of picture elements in each line.
Frame ID	3	Once per Sweep	Used to identify the framed blocks of imagery.

Memory Buffer Since the MSS VTR tape format provides six MSS scan lines in parallel on six tape tracks for Bands 1-4 (representing a single MSS mirror sweep), a buffer is required to store a full sweep of video data to permit the data to be read out as a sequence of six individual lines. This reformatting operation effectively interfaces the MSS (6 lines per mirror sweep) and EBR (I line per beam sweep on film) or HDDT (1 serial line of data per tape track). A large buffer memory system, consisting of ten core memories performs this reformatting. The buffer is organized as 5 pairs of memories, each pair assigned to a spectral band. The buffers are operated in alternating mode, i.e., one group of 5 memories is loading data under control of the individual input data decommutators while the other group of 5 memories is being read out under control of the output data formatter.

The memory buffer capacity for each spectral band is dictated by the number of bytes (picture elements) per MSS sweep. Bands 1-4 require a 19, 800 byte capacity while band 5 requires a 2, 200 byte capacity. Memory cycle time is determined by the maximum input or output rates for all modes. The cycle time/memory word length/memory size trade-off for both MSS VTR and HDDT input modes shows a 4096 word x 36 bit memory with 1 microsecond full cycle time to be the most efficient buffer for bands 1-4. The band 5 memory is identical to permit full buffer hardware compatibility for all bands. The 36-bit memory word contains a group of six consecutive bytes from the serial data stream, representing six consecutive picture elements in a scan line.

The spectral band 1-4 memories are divided into six major sectors, each sector being accessed by an individual tape track decommutator and containing the video data for a single MSS scan line. The data is loaded such that the nth memory word in a sector contains the nth group of six bytes (picture elements) in the scan line. Spectral band 5 buffers are divided into 2 major sectors, representing the Z scan lines per MSS sweep. This buffer is loaded by the single track decommutator (MSS VTR input) or by all 4 track decommutators (HDDT Input). Six memory locations are also provided for storage of the calibration bytes which are decommutated from the MSS VTR format. Bands 1-4 require six memory locations (six calibration bytes per line) for 1 sweep while Band 5 requires two memory locations for 1 sweep.

The data is asynchronously loaded into the memories due to the interline asynchronism introduced by tape recorder skew. As the data from all bands (HDDT output) or a single band (EBR output) is synchronously read out by the data formatter, all input skew effects are removed. By sequentially reading data from the lowest to highest location of each sector, starting with sector I and finishing at sector 6 (bands 1-4) or sector 2 (band 5) the data is conveniently reformatted from the parallel input to an output of 6 or 2 lines in sequence.

Central Timing and Control The central timing and control performs the following functions: (1) accepts all control computer commands and issues internal timing and control as required (2) provides verification of command receipt and status of system operation (3) generation of fault or status change interrupts (4) interfaces control computer (remote) and control panel (local) command inputs, (5) provides major state timing for synchronization of all inputing and outputting operations.

The major state timing is the most critical function performed by this logic. A master clock oscillator is divided to generate synchronous timing for all logic in the MSS TDP. Input state (search, lock), buffer state (input/output) and output states are generated by this clock. The master clock also provides a reference frequency which is used to phase-lock (by the tape reproducer tape sync servo) the incoming data and to servo the EBR film transport. This synchronization assures that the data buffers do not overflow or underflow due to tape speed variations.

Output Data Formatter and Interface The output data formatter generates addresses for reading the data from the buffer memories and controls the passage of the data through the four Output Data Interface Units. The formatter provides addressing and timing in two primary output modes: (1) EBR mode - a single memory pair is accessed (one spectral band) and the data is passed through the single EBR interface (2) HDDT mode - all five memory pairs are accessed in proper sequence to generate the HDDT tape format, multiplexing sync and ID codes into the output data.

Figure 5 shows the configuration of the output data interface which includes holding registers, A and B, buffer the memory access operation and the demultiplexer which divides the 36 bit memory word back into a sequence of 6 bytes. A multiplexer permits the formatter to insert the line sync, frame ID, and frame sync codes required for the HDDT tape format. A final holding register provides the parallel output interface with the EBR and HDDT.

A high speed parallel processor is utilized to operate on the MSS data prior to outputting to the EBR. The figure shows the location of this processor in the logic which interfaces with the EBR. The processor employs a ripple-through technique and requires less than I byte-period delay. The processor consists of two sections; a table lookup memory and an arithmetic operator. A semiconductor read-write memory performs a one-to-one mapping from the six bit data into eight bit data. This table lookup is capable of performing the inverse of the non-linear data compression applied on the spacecraft, linearizing the data prior to radiometric calibration. The control computer provides a gain and offset correction for each scan line to radiometrically calibrate the video data. (These coefficients are derived from the cal wedge data, decommutated and transferred to the computer by the TDP.) A parallel array multiplier, and a parallel adder apply the gain

and offset (respectively) to the video data. The combined multiply/add processor has a ripple-through time of less than 260 nanosec.

In the HDDT output mode, the output byte rate is controlled by the CTC master clock, while in the EBR output mode, this rate is controlled by an EBR-generated byte-rate clock. The external rate control permits the EBR to vary the D/A conversion rate. This capability permits compensation of scan mirror velocity and line length variations.

System Operation The total input - output operational sequence of the MSS TDP will be described for the MSS VTR to EBR mode. Figure 6 presents the operation timeline for this mode, showing hardware - software interaction. The following sequence of major events occur each sweep:

(1) Upon detection of preamble and acquisition of line start sync, the TDP decommutates spacecraft time code and issues a T/C ready interrupt. The control computer accepts this data and uses it to partition the strip data into frames.
(2) The video data is loaded into the buffer memories, LLC is decommutated and a LLC ready interrupt is issued. The computer accepts this data and calculates the number of bytes (picture elements) in all scan lines for that sweep. This number is transferred to the EBR for control of the data output rate.
(3) The calibration wedge is detected on alternate sweeps and six bytes are sampled from the wedge for each scan line. A cal ready interrupt is issued and the computer accepts these samples from the data transfer interface. The computer performs the following operations on this data to obtain radiometric gain and offset corrections for the output processor: (1) sensor gain and offset are estimated from the six samples using linear regression, (2) gain and offset estimates are smoothed by a recursive filter operation. Once the gain and offset corrections are computed, they are transferred to the MSS TDP for application to the corresponding sweep.
(4) MSS TDP concludes the decornmutation cycle and the central timing and control issues a begin preamble search command to all MSS decommutators as the search window opens.

Conclusion The MSS TDP performs the operations of multiple-track decommutation, reformatting and high-speed processing required for conversion of ERTS multispectral data tapes to a more useful form. The parallel organization permits simultaneous handling of multiple spectral bands at a high rate. The modular design also permits future expansion of the units I capabilities (e.g., calibration of multiple bands simultaneously as would be required in color film recording.) Future spacecraft employing scanners with increased spatial resolution and additional spectral bands will require advanced tape decommutators/processors to handle the increased volume and rate of information acquired. The MSS TDP system configuration and operating timeline provides a foundation for the design of these systems.

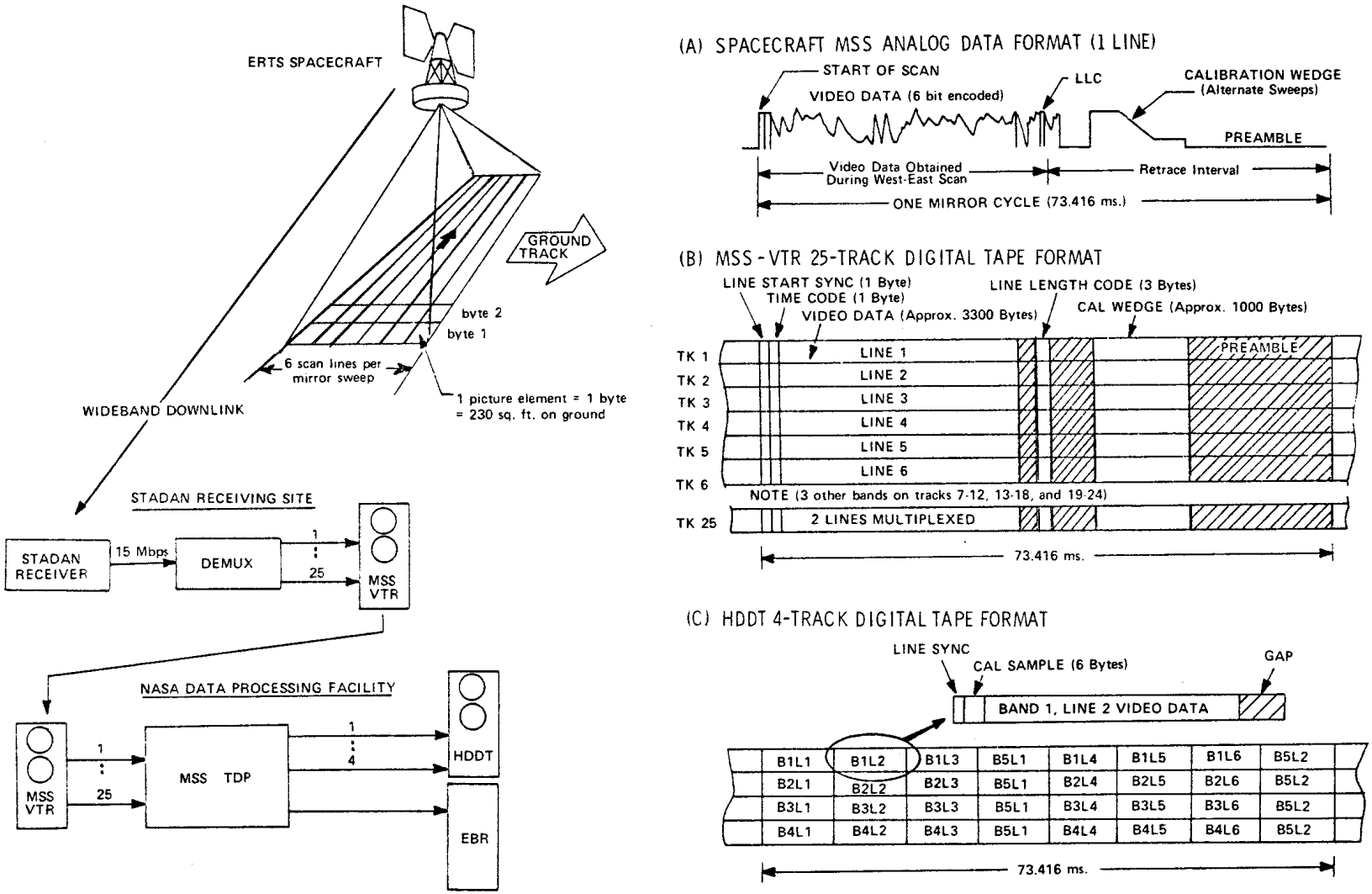

Fig. 1 - Multispectral Scanner Data Flow and Formats.

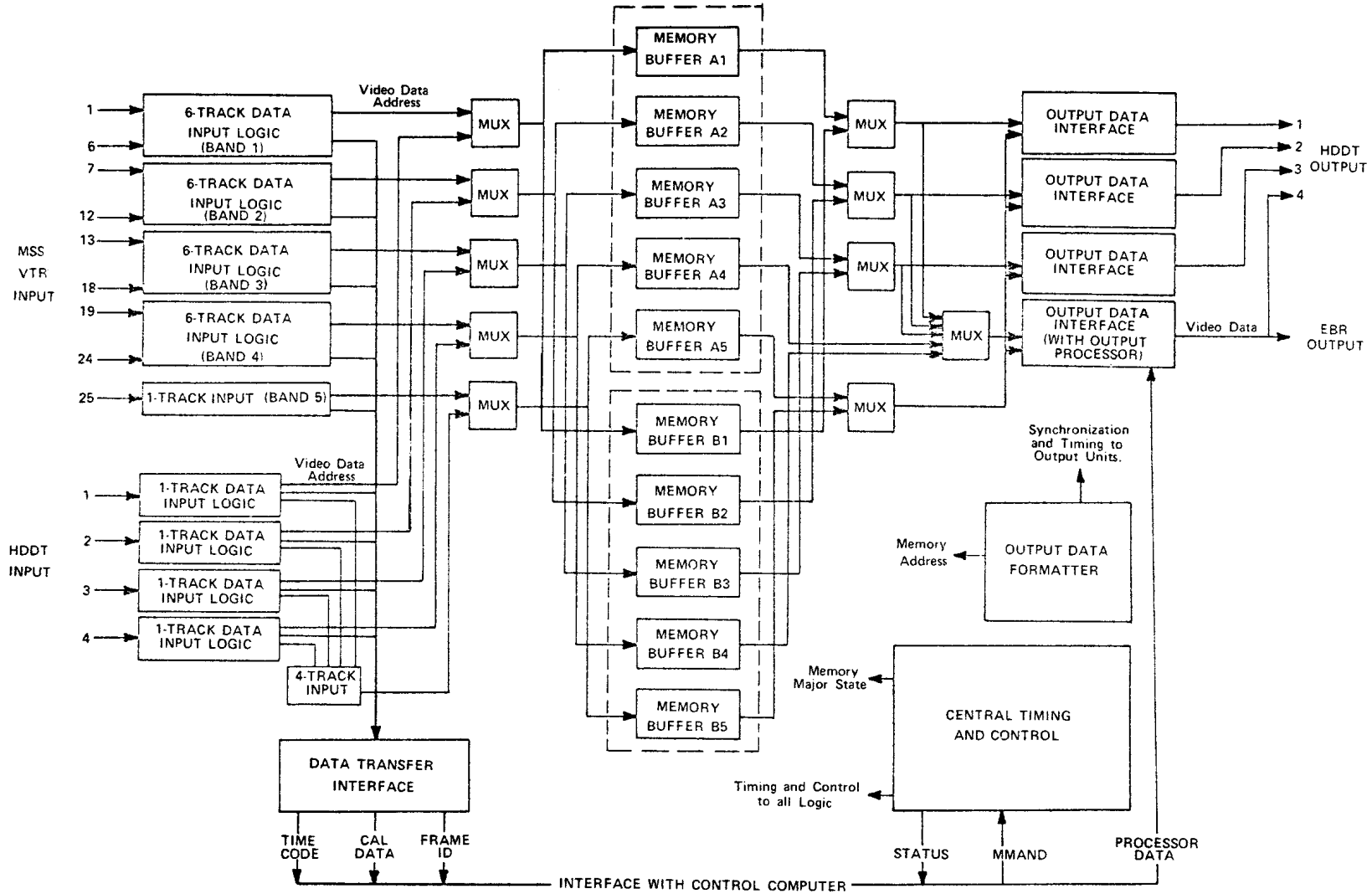

Fig. 2 - MSS-TDP Block Diagram.

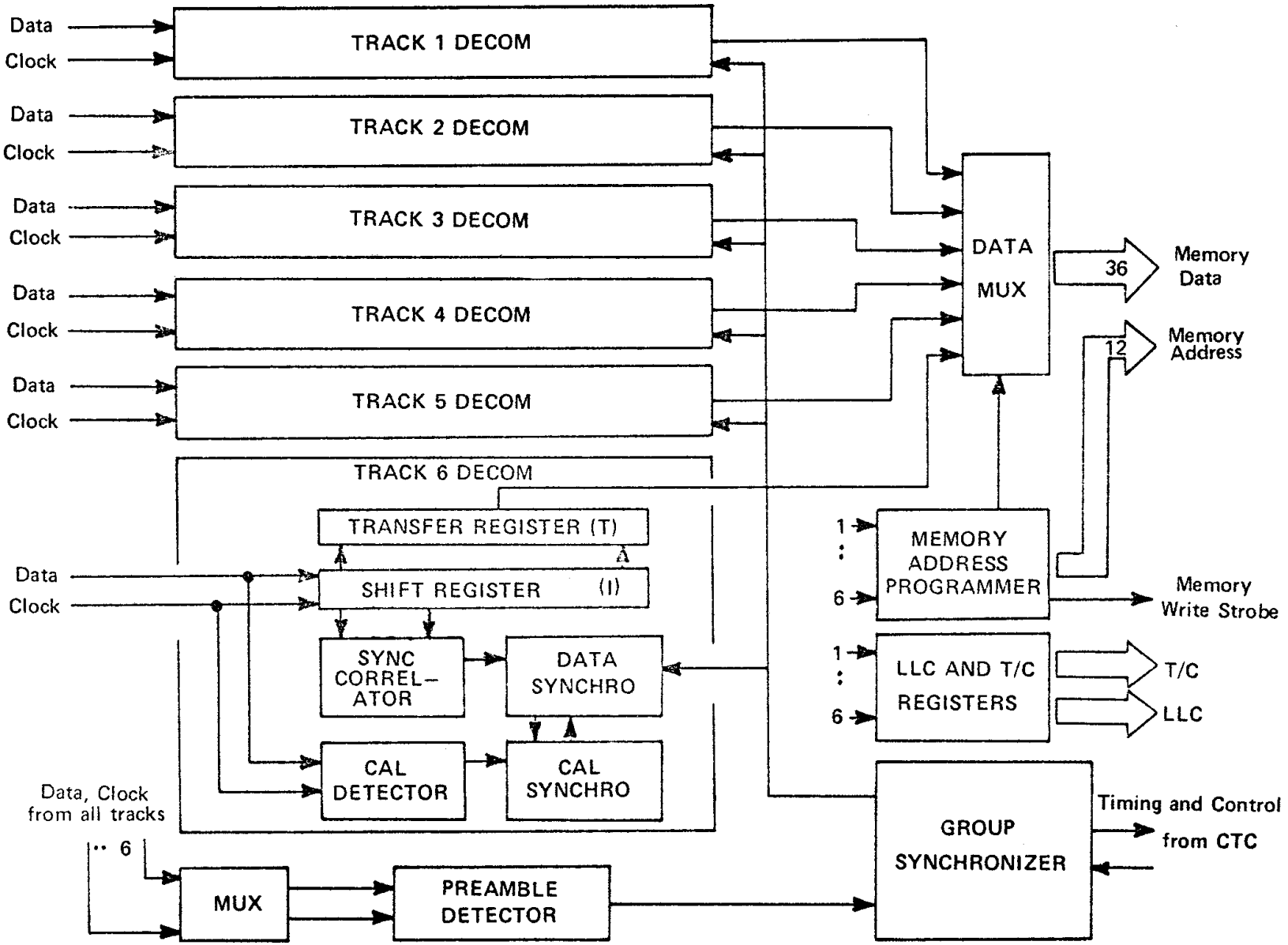

Fig. 3 - MSS TVR 6-Track Input Decommutator/Synchronizer.

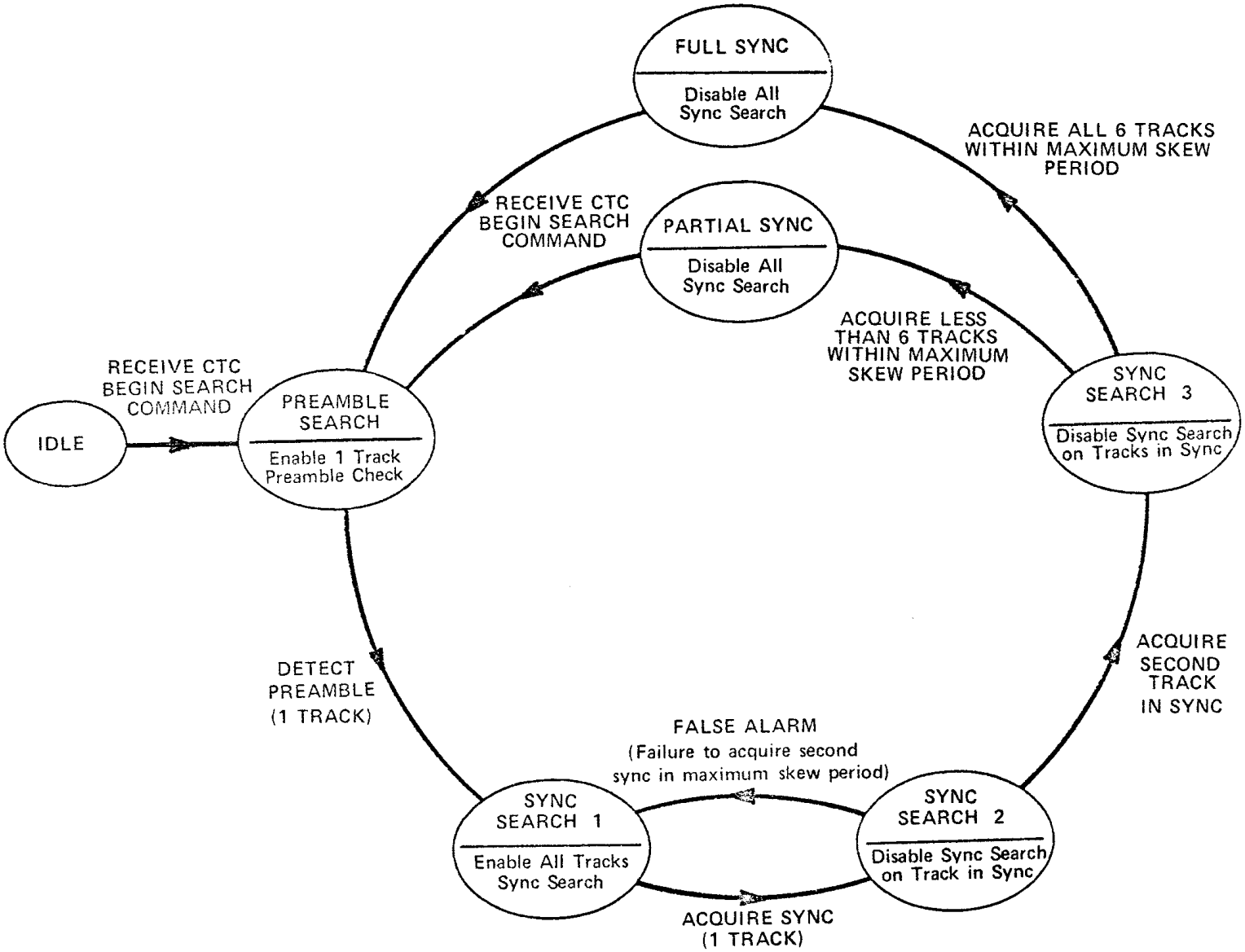

Fig. 4 - Group Synchronizer State Transition Diagram

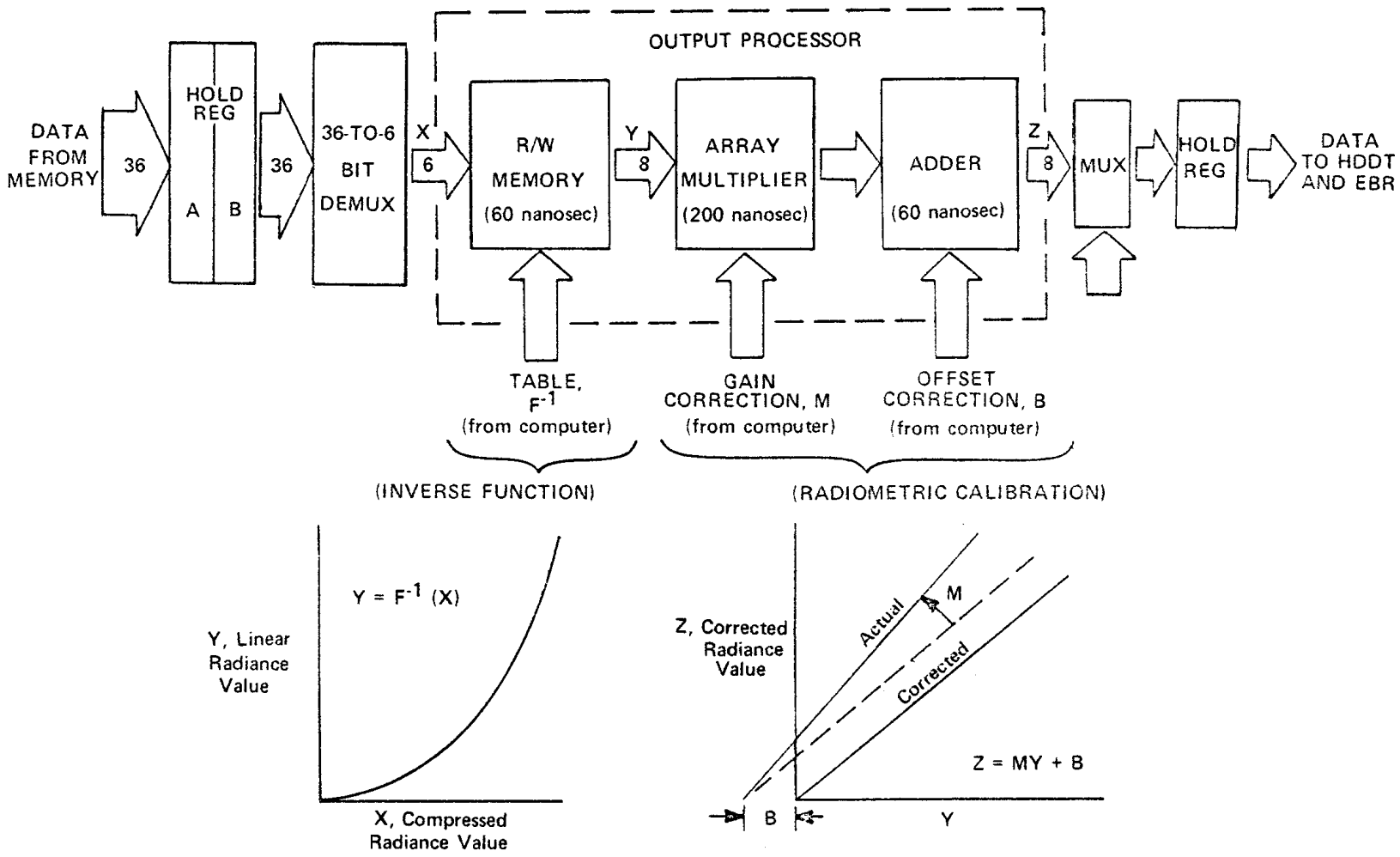

Fig. 5 - Processor Operations and Hardware Configuration.

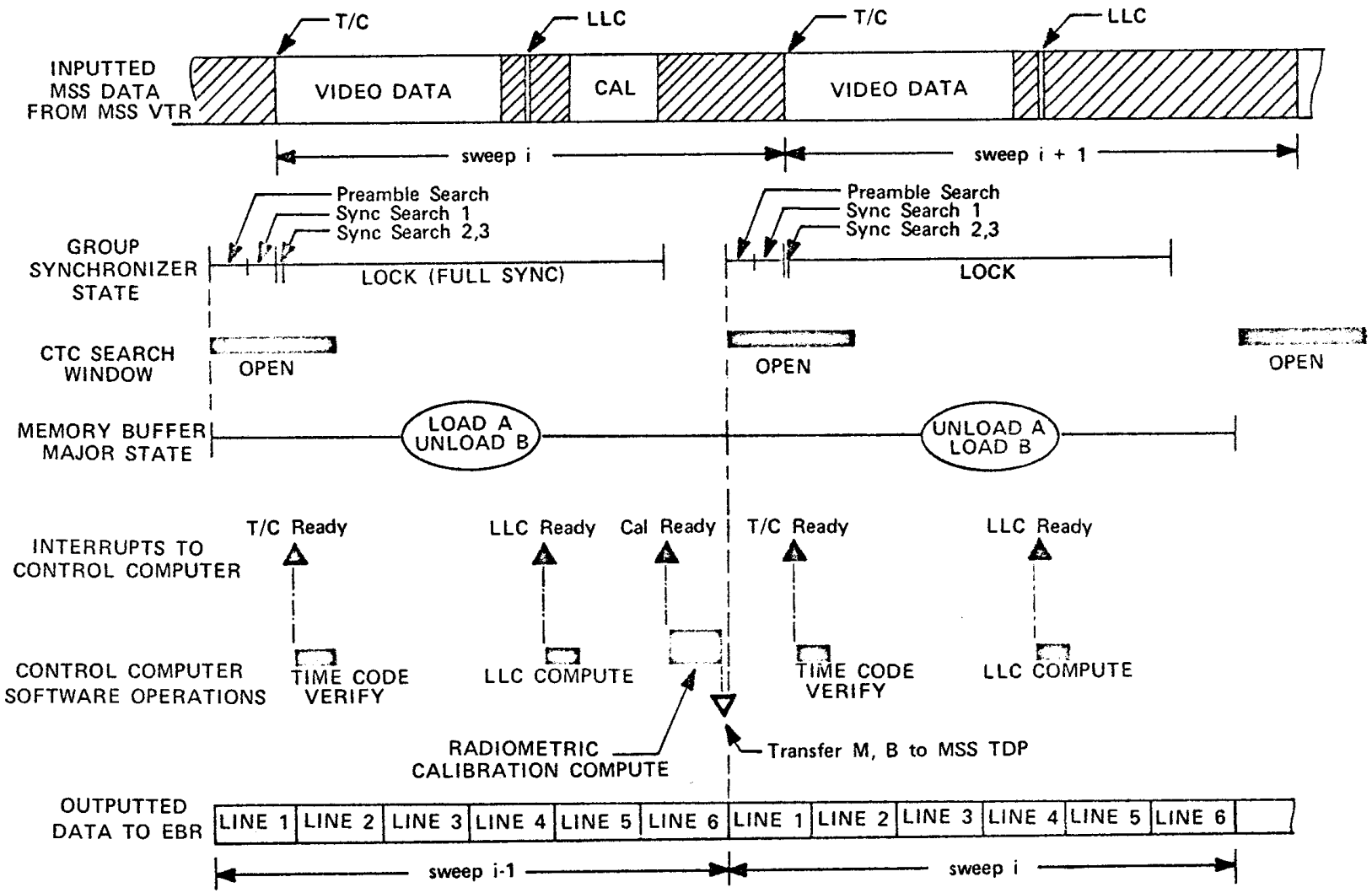

Fig. 6 - MSS TDP Operational Timeline (MSS VTR to EBR Mode.)