SIGNAL PROCESSING TECHNIQUES FOR A 1000 MB/S MICROWAVE COMMUNICATION LIN K

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Summary Special circuit design techniques must be used for wideban@! signal processing systems. These techniques are based on the use of a limited number of circuit types with the multiplier/signal switch as the dominant active signal processing element. The capability of this approach is illustrated in the construction of a 1000 MB/S QPSK Modem and a ZOO MB/S data regenerator which uses a true reset integrator for optimum bit-by-bit data reconstruction.

Introduction Motorola has developed a unified set of building block functions which can be interconnected to meet a broad range of application requirements with a minimum of specialized design effort. This set of functional elements is based on the concept that:

1. Most signal processing (analog and/or digital) can be accomplished with a few circuits. These are:
   a. Video amplifier
   b. Multiplier and signal switch[(1)]
   c. Emitter coupled logic

2. Microstrip transmission line is suitable for circuit interconnect.

The three circuit types listed under 1. are also supplemented by the hot carrier diode/transformer circuits in applications requiring accurate dc stability such as phase detectors. The tunnel-diode and the snap-diode are not suitable signal processing elements because of the difficulties encountered in interfacing with these components for general purpose applications.

The family of active circuits capable of processing signals in excess of 1000 MB/S is very limited - in fact, consists of only two circuits. These circuits are an amplifier and a multiplier/signal switch. Both of these circuits are capable of processing either analog or digital information and. have bandwidths of greater than 1000 MHz and propagation delays of less than 0. 5-nanosecond. The circuits are constructed by hybrid circuit techniques and housed in a 3/8 x 3/8-inch Rat-pack (Figure 1).

Multiplier/Signal Switch This circuit is the dominant component in the active signal processing family. The schematic diagram of the circuit shown in Figure 2 illustrates the conventional arrangement used for the circuit and is designed for operation as either an analog or digital signal processor.

This circuit operates from a +5V and a -5V power supply and requires approximately 110 mW of power. The diagram of Figure 3 illustrates the functional operation of this circuit. The control line, W, determines the gain of the amplifiers A_1 and A_2[(2)] The operation is such that $A_1 + A_2$ is always a constant. The time required to switch from A_1 to A_2 is less than 0.5-ns. The curve of Figure 4 illustrates the frequency response of the unit. The speed and accuracy of the switching characteristics are illustrated in Figure 5. The use of a new transistor family provides an increase of the frequency response to 2 GHz.

When operation only as a digital processing element is required., the circuit of Figure 2 is modified slightly in order to reduce the power consumption to approximately 70 mW per function when ac coupling can be used on the output. The power consumption is increased to 100 mW when dc coupling is required (the output coupling capacitors must be replaced by zener diodes).

Logic Applications Three different logic equations can be obtained with the circuit by different input connections. The logic diagram of Figure 6 illustrates the functional diagram of the network. With reference to this figure, the three sets of output functions are:

$$X_1 = U \cdot W + V \cdot \overline{W}$$

$$X_2 = U \cdot W + \overline{V} \cdot \overline{W}$$

$$X_3 = \overline{U} \cdot W + \overline{V} \cdot \overline{W}$$

An exclusive OR function is obtained from X_2 by setting U = V. The memory element can be obtained from X_1 by setting

$$X_1 = U, \text{ which gives}$$

$$X_1 = X_1 \cdot W + V \cdot \overline{W}$$

From this equation, it is evident that the output will follow the V input when W is on “zero”. When W is a “one”, the output will remain in the state just prior to the “zero” to “one” transition time. This operation is similar to the clocked RS flip-flop function. A master-slave flip-flop function can be constructed with two of the RS flip-flop functions. Operation of the circuit as a memory element has been demonstrated by constructing a divide-by-2 which will operate at 2 GHz on the input. This circuit has also been used to

retime digital data to obtain a 20 picosecond timing accuracy on the output transitions. A 5 stage PN generator has also been constructed with this logic familywhichoperated at 1000 MB/S(see Figures 5 and 7).

Quadriphase Modulator Subsystem Figure 8 illustrates the functional block diagram of the modulator subsystem. This subsystem consists of a precision retiming circuit and a phase shifter/amplifier.

The Digital Phase Shifter/Amplifier makes use of transistor type switches to perform the modulation on a low power level subcarrier. This modulation scheme has several advantages over modulation at the X-band output frequency. The most dominant ones are:

1. Modulator construction follows the conventional microstrip transmission line technique and does not require any special circuit or construction techniques.

2. No high power modulator drivers are required.

3. Modulator design does not depend upon output frequency.

4. Bandwidth capability exceeds 1000 MB/S for quadriphase modulation.

The most significant disadvantage of this scheme is that an up-converter is required to convert the subcarrier to the desired output frequency. This conversion process makes use of conventional circuit elements, and therefore does not require any significant additional design effort.

Table 1 shows the relative carrier phase relationship with respect to the digital input signals. Figures 9 and 10 illustrate the performance obtained from Motorola's Quadri-phase Modulator. [(3)]

Table 1. Carrier Phase Relationship vs Modulation Signal

Digital Input		Relative Carrier Phase
A	B	
0	0	0°
0	1	180°
1	0	90°
1	1	270°

A precision retiming circuit must be used for retiming the two digital input signals to insure proper transition times of both channels. This retiming must be accomplished just before modulation to insure optimum system performance as well as eliminate the need for matching the digital input signal lines from the digital data source.

One channel of the retiming circuit is illustrated in Figure 11. This circuit makes use of the fast/accurate switching properties of the CRA. The connection illustrated converts the signal switch to a clocked RS flipflop. The digital input signal is sampled for 1/2 of a bit time and then the sampled, signal is stored for the other 1/2 bit time. The timing accuracy is obtained by this sampling action and thus insures that all output transition times will be determined by when the clock makes its negative to positive transition. This method of retiming will maintain a transition accuracy of better than ±0.03 nanoseconds on both digital channels and for either polarity transition.

Quadriphase Demodulator This demodulator follows the conventional approach used in quadriphase demodulation, i.e. , obtaining a phase-locked reference carrier and using this reference to demodulate the inphase and quadrature components of the incoming signal.

Figure 13 illustrates the basic IQ loop used for the demodulator. The operation of this loop is Little different from conventional IQ types of demodulators which have been thoroughly discussed in the literature.[4] The major difference here is the construction techniques used. Successful construction of the IQ loop requires the use of two wideband analog multipliers which normally would pose a significant problem in the circuit. In this case, the use of the standard multiplier units developed by Motorola makes this a straight forward task. The phase detectors required in the demodulator are made with hot carrier diode/transformer circuits.

The basic specifications of this unit are:

Input Signal

Amplitude:	-10 to -20 dBm
Frequency:	Approximately 800 MHz
Load Impedance:	50 ohms

Acquisition Time

Less than 1 μs for a frequency offset of up to 500 kHz.

Tracking Loop Noise Bandwidth

Less than 2 MHz after acquisition. Greater than 8 MHz during acquisition.

Combined Static and RMS Phase Jitter (+12 dB input signal to noise ratio).
Less than 5° RMS for a 500 kHz offset in center frequency.

The unit consists of two modules as illustrated in Figure 14. The first module contains the phase detector, baseband output buffers, and the voltage controlled oscillator. The second module consists of the chopperstabilized multiplier network and the loop filter.

Data Reconstruction The two outputs of the demodulator module are applied to two independently operating bit synchronizer modules - one for each channel. The functional block diagram of the unit is illustrated in Figure 15, and a photograph of the unit is in Figure 16. This unit is an extremely efficient, accurate matched filter which utilizes a true reset integrator for data detection. The bit synchronizer follows a conventional approach for obtaining a clock reference.

A current mode reset integrator capable of operating in excess of 500 MB/S is used for optimum bit-by-bit data reconstruction. Circuit operation is explained in the simplified diagram of Figure 17. During bit integration time SI is closed and S2 is open. The current in the inductor is proportional to the integral of the input signal when the L/R time constant is large relative to the bit period. At the end of the bit time, SI is opened and S2 is closed simultaneously and then S2 is opened. This produces an inductive voltage impulse at the input of amplifier A which is proportional to the current at the bit termination time. The voltage impulse is then amplified and stretched for threshold detection. The remainder of the bit time is used for discharge of the energy in the circuit. Two of these circuits are used such that they operate on alternate bits of data; while one circuit is integrating, the other is sampling and discharging.

The performance of the 200 MB/s data- regenerator is within 0. 6 dB of the theoretical obtainable performance for bit-by-bit detections of input data band limited to 200 MHz. This performance was obtained over a bit error rate of 10^{-3} to 10^{-7}.

The performance of the entire QPSK Modem operating at 400 MB/S with an RF bandwidth of 600 MB/s has been measured to be within 1.5 dB of the theoretical true matched filter detection. Modifications in 400 MB/S system are currently under way to permit a complete system evaluation of the 1000 MB/S Modem.

Conclusion The small family of signal processing circuits permits construction of a large variety of complex signal processing functions. These processing functions can be both analog and digital and data rates in excess of 1000 MB/S can be handled. successfully. System performance of high data rate processing equipment is better than that obtained using more conventional circuit design techniques and considerable less engineering time is required to perform the design.

REFERENCES

1) C. Ryan, U. S. Patent No. 3452Z89, June 24, 1969.

2) C. Ryan, “Applications of a Four Quadrant Multiplier, “ IEEE Journal of Solid State Circuits, February, 1970.

3) The 1000 MB/S modulator/demodulator was demonstrated at the ITC and the AFCEA conference in 1970.

4) L. N. Ma, M. S. Stone, D. P. Sullivan, “Synthesis of High Data Rate Coherent Telemetry Systems, 11 ITC Proceedings, October, 1968.

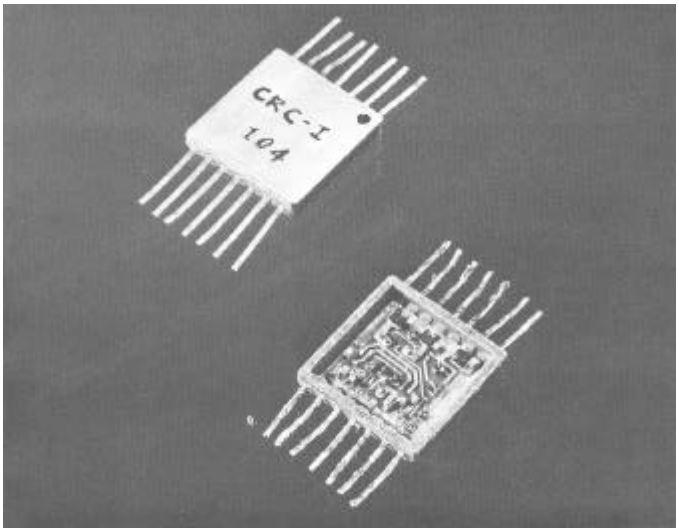


Figure 1. Switch Constructed on a Sapphire Substratae

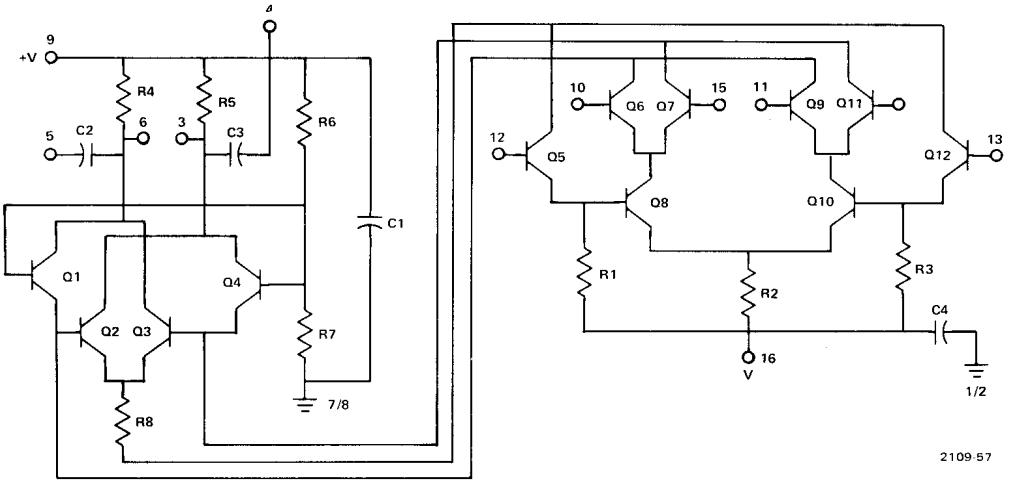


Figure 2. Schematic of the Multiplier/Signal Switch

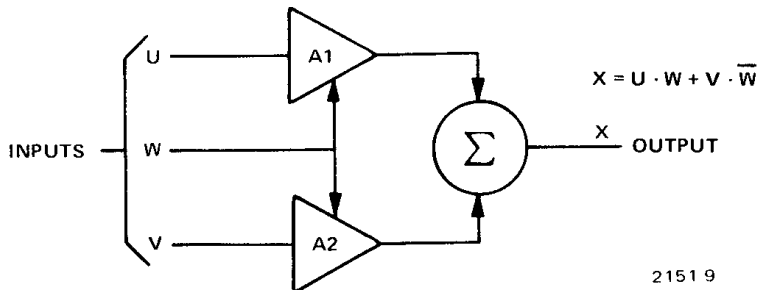


Figure 3. Functional Arrangement for the Multiplier/Signal Switch

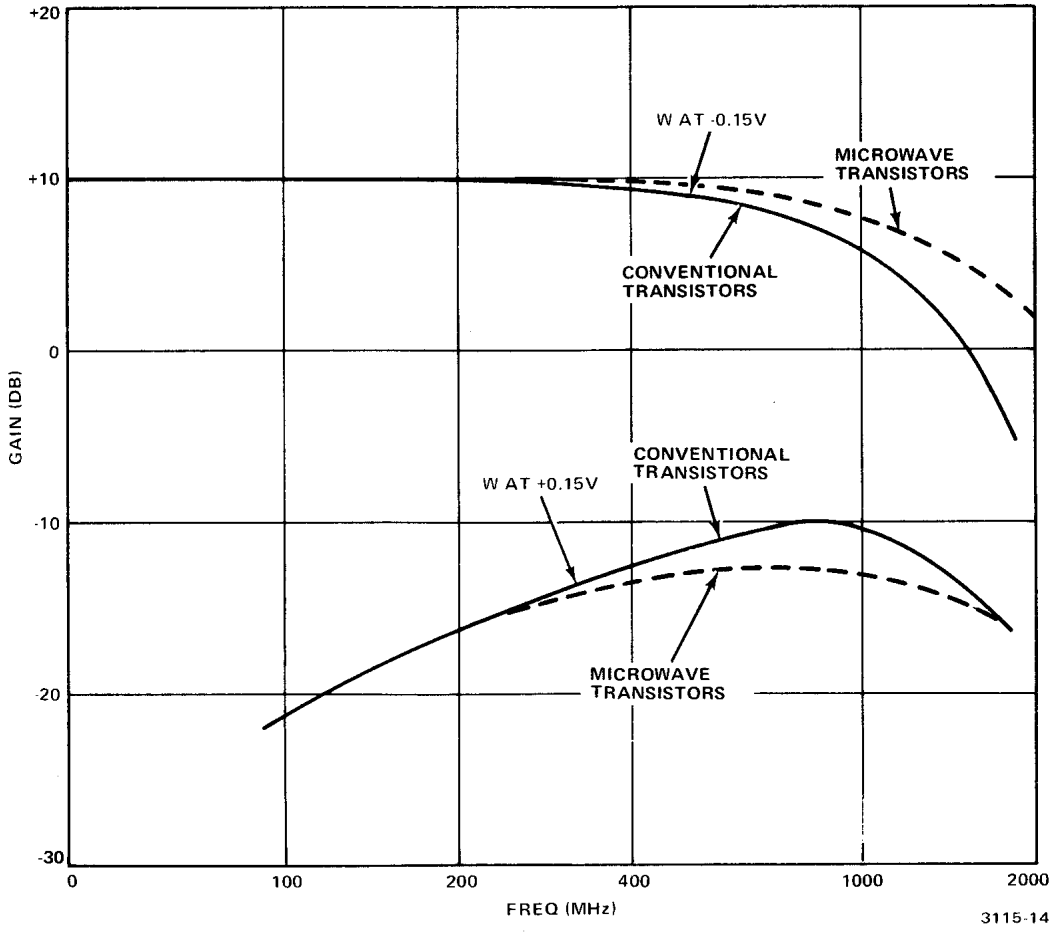
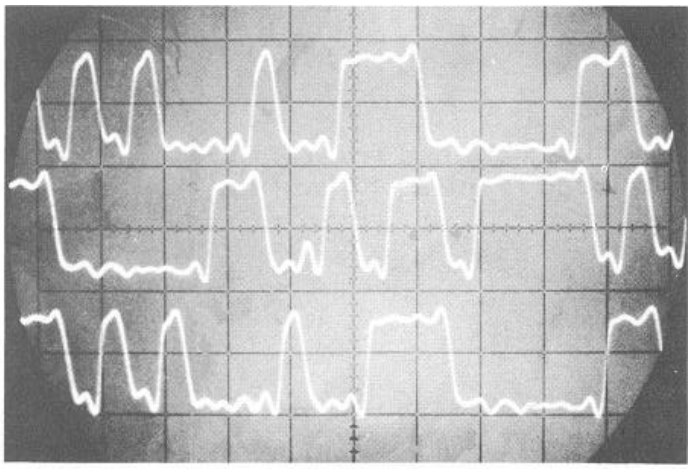


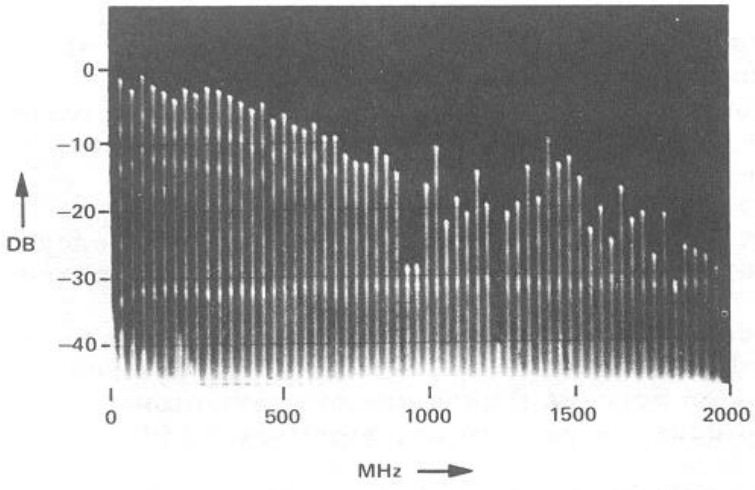
Figure 4. Frequency Response and Isolation Characteristics of the CRA-II



A. OUTPUT OF A 5 STAGE PN GENERATOR OPERATING AT 1000 MB/S

2 NS/DIVISION HORIZONTAL
.4 VOLT/DIV VERTICAL

THE RISE TIME OF THE SCOPE USED TO TAKE THIS RESPONSE WAS 0.09 NANOSECONDS



B. SPECTRUM OF THE PN SEQUENCE IN A

Figure 5. Switching Characteristics (Sheet 1 of 2)

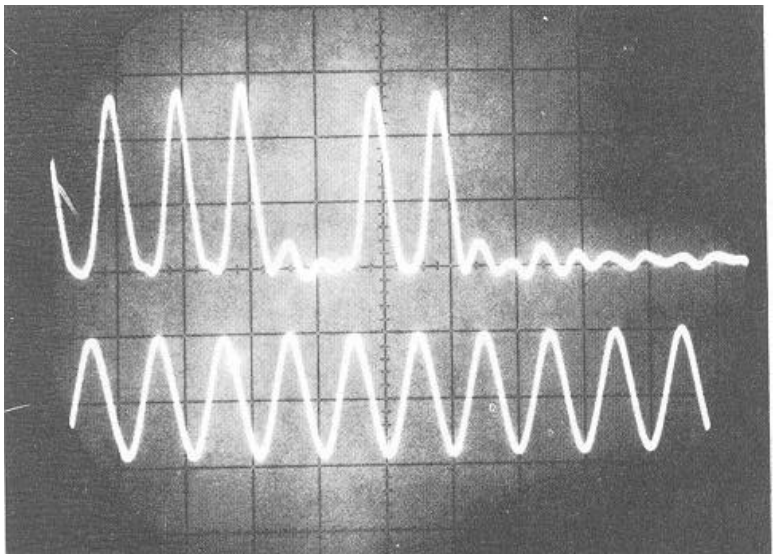


Figure 5. Switching Characteristics (Sheet 2 of 2)

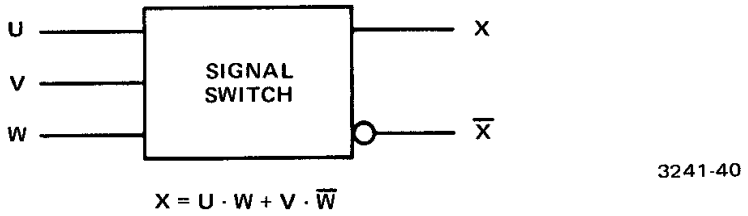


Figure 6. Logic Diagram for Gain Controlled Amplifier

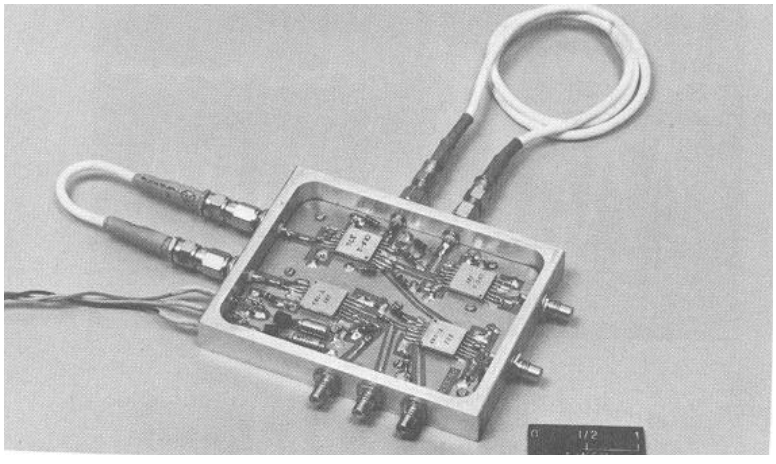


Figure 7. Photograph of the 1000 MB/s PN Generator

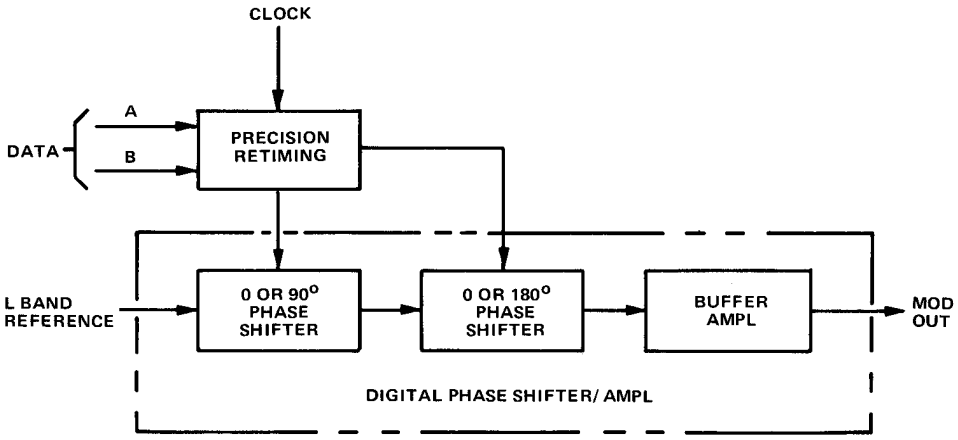


Figure 8. Modulator Subsystem Functional Block Diagram

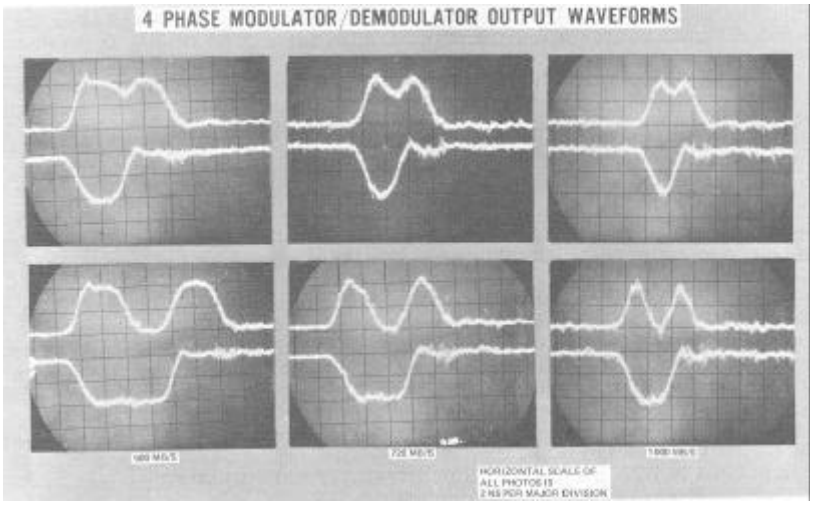


Figure 9. Demodulator Output Waveforms

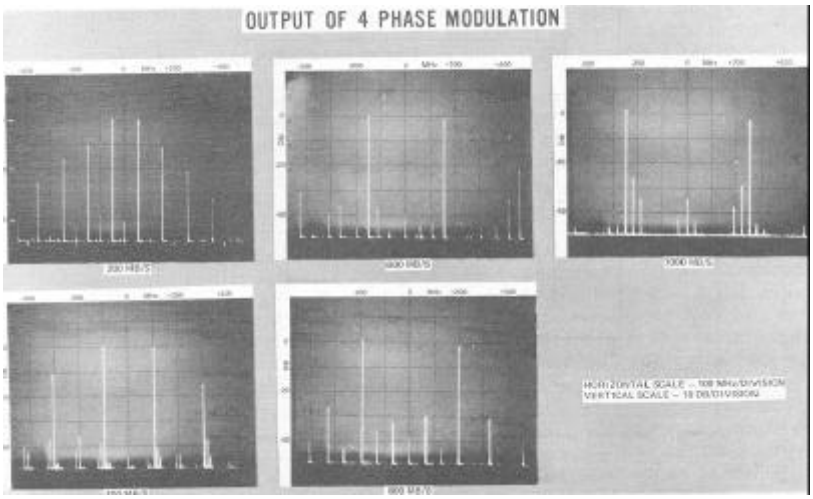


Figure 10. Spectrum of Modulator

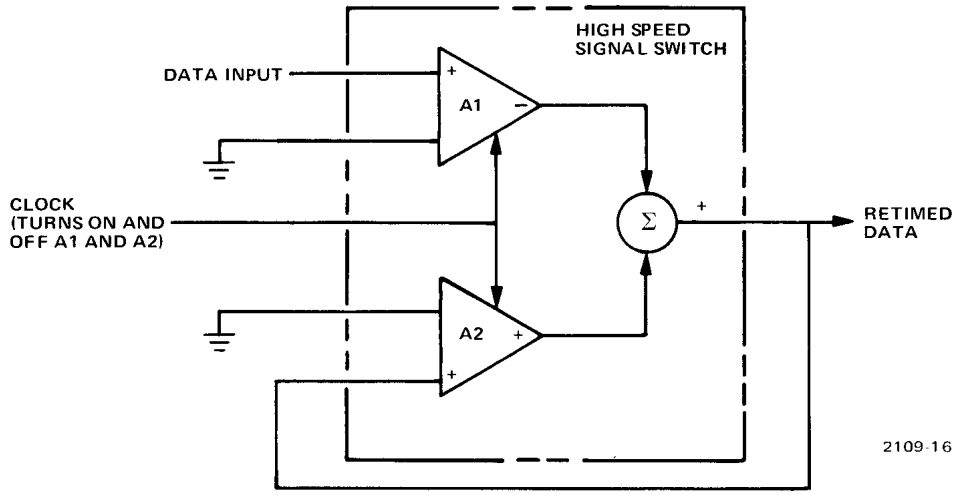


Figure 11. Precision Signal Timing

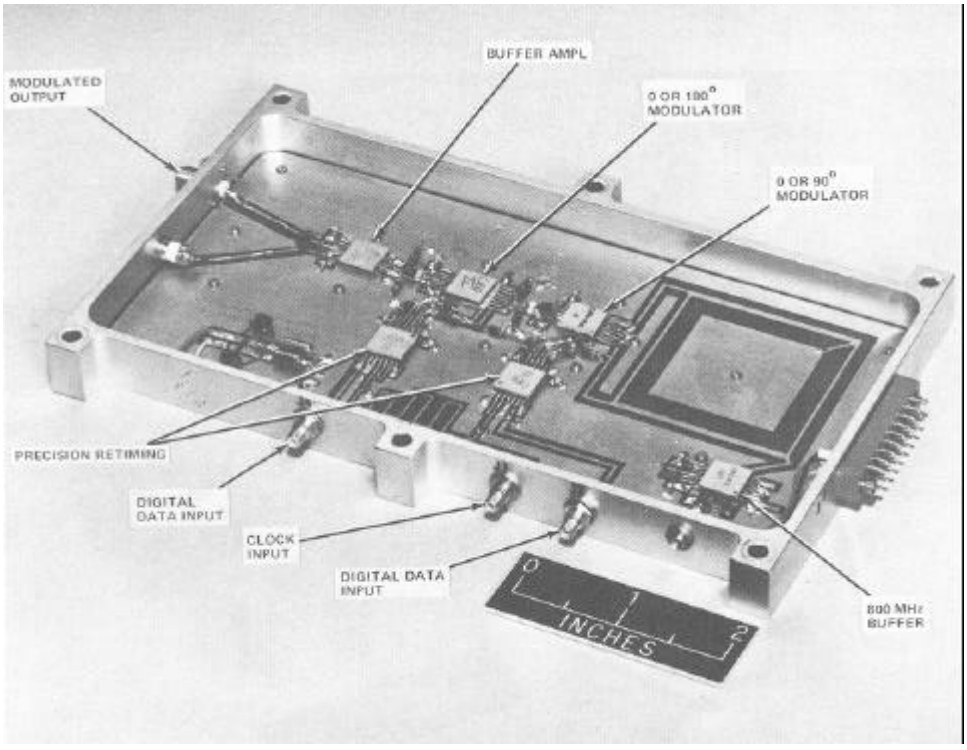


Figure 12. Quadriphase Modulator and Precision Retiming Module

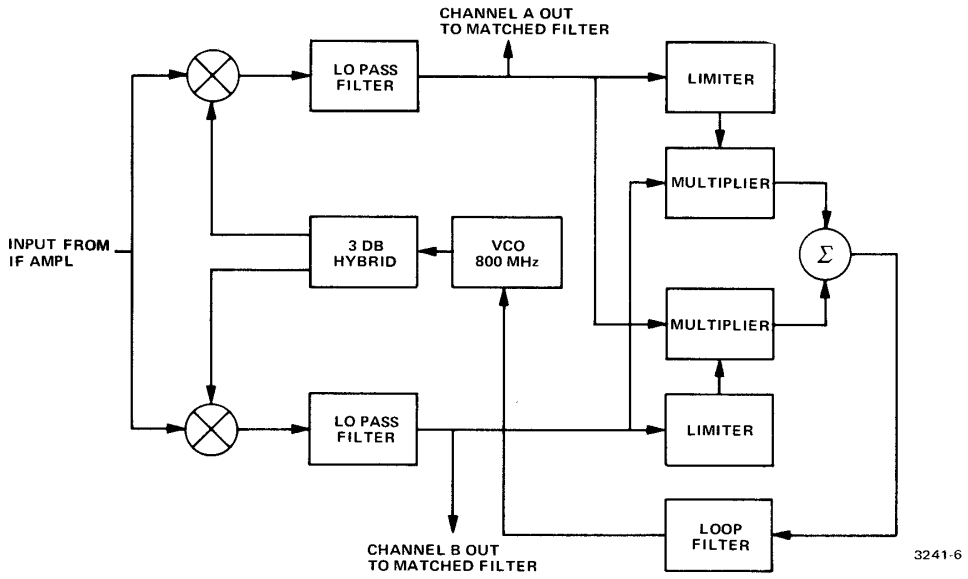


Figure 13. 4-Phase Demodulator and IQ Loop

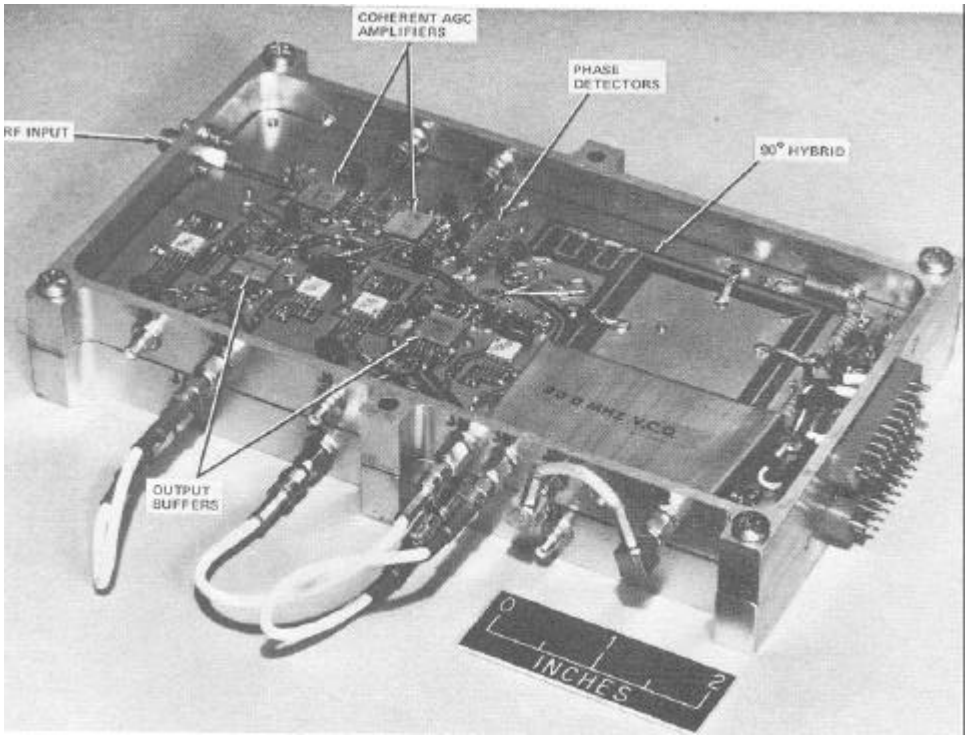


Figure 14. 4-Phase Demodulator and Phase Detector

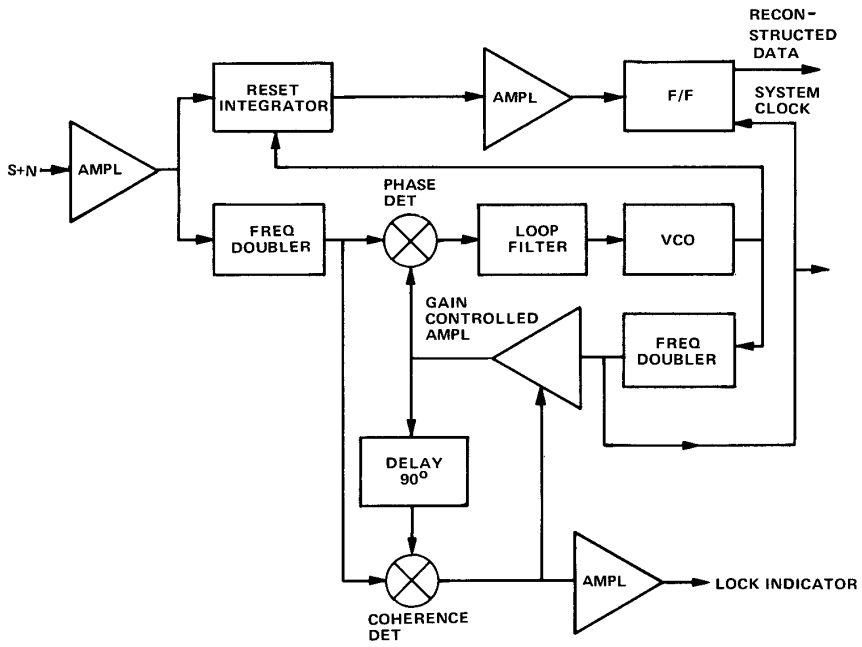


Figure 15. Bit Synchronizer and Matched Filter Block Diagram

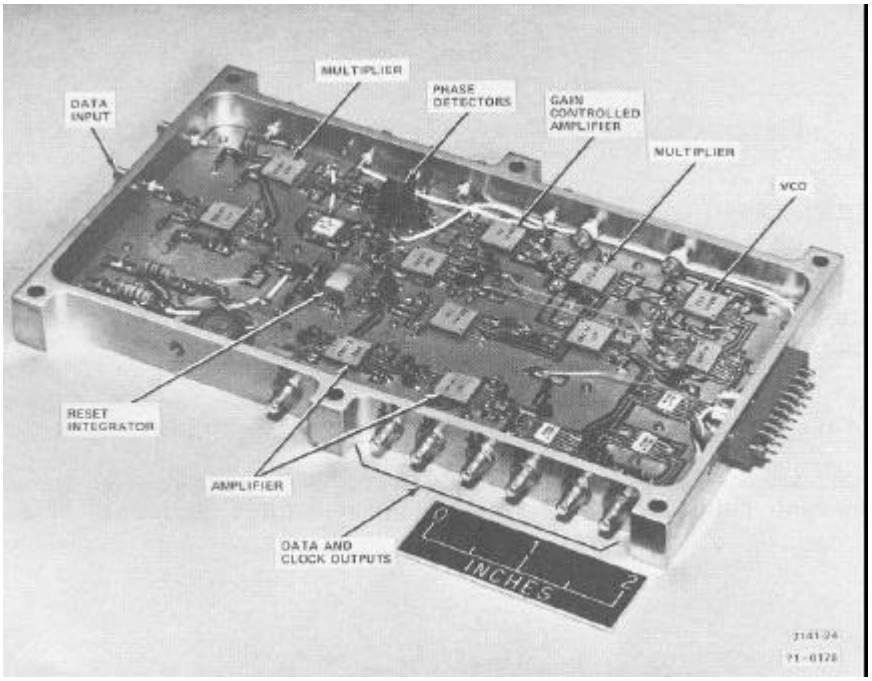


Figure 16. 200 MB/S Bit Synchronizer and Matched Filter

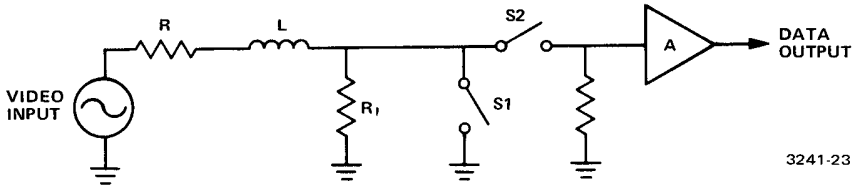


Figure 17. Simplified Diagram of the Reset Integrator