A DESIGN FOR A 10.4 GIGABIT/SECOND SOLID-STATE DATA RECORDER

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ABSTRACT

A need has been identified in the Test and Evaluation (T&E) and tactical aircraft communities for a ruggedized high-speed instrumentation data recorder to complement the ever-increasing number of high frame-rate digital cameras and sensors. High-speed digital camera manufacturers are entering this market in order to provide adequate recording capability for their own cameras. This paper discusses a Solid-State Data Recorder (SSDR) for use in Imaging and High-Speed Sensor Data Aquisition applications. The SSDR is capable of a 10.4 Gb/sec sustained, 16Gb/sec burst, input data rate via a proprietary 32-channel-by-10-bit generic high-speed parallel interface, a massively-parallel 256-bit bus architecture, and unique memory packaging design. A 32-bit PCIbus control/archive and dedicated DCRsi™ interface are also employed, allowing data archiving to standard high-speed interfaces (SCSI, Fiber-Channel, USB, etc.) and DCRsi™-compatible tape recorders.

KEYWORDS

Solid-State Data Recorder, High-Speed Video Imaging, Digital Sensor Processing, and Data Archiving.

INTRODUCTION

Current and future aircraft, space, and autonomous missile applications have limited space remaining to install the large tape recorders needed to acquire test flight and mission data. As the complexity of the guidance and avionics systems of these platforms increases, the need for high-capacity data recording equipment becomes apparent. Additionally, current airborne reconnaissance platforms' use of analog sensors is gradually transitioning to digital devices in order to accommodate the tremendous volume of high-resolution imagery and sensor data. For example, Silicon Mountain Designs is developing a Charge-Coupled Device (CCD) high-speed color imaging camera capable of 4000 frames/second with a 512 X 512-pixel resolution; when digitized into 10-bit pixel information, this frame rate converts to a 10.486 gigabit/second data rate!

Tape storage devices are not capable of handling the data rates and storage capacity requirements of the digital sensors (most are only capable of a maximum 240 megabit/second data rate) and are prone to poor reliability and communication/processing errors, mainly due to their mechanical tape transport mechanism. Current non-volatile SSDRs, having mainly been designed as higher-performance "drop-in" replacements for the tape devices, are only capable of storing data at a maximum of 1gigabit/second.

The subject design accommodates the high data rate, high storage capacity requirements of these digital sensors in a compact, high-performance form factor, with medium power requirements. The design was developed by Systems & Processes Engineering Corporation (SPEC) at their Austin, Texas laboratories under the trade name Tornado 10™.

OVERVIEW OF THE DESIGN

The prototype of the design is housed in an ARINC-standard 1ATR Long enclosed chassis and is cooled by conduction of heat to the chassis exterior walls and bottom plate. Figure 1 illustrates the block diagram of the design, which is divided into two (2) modules interconnected by a Backplane/Power Supply module.

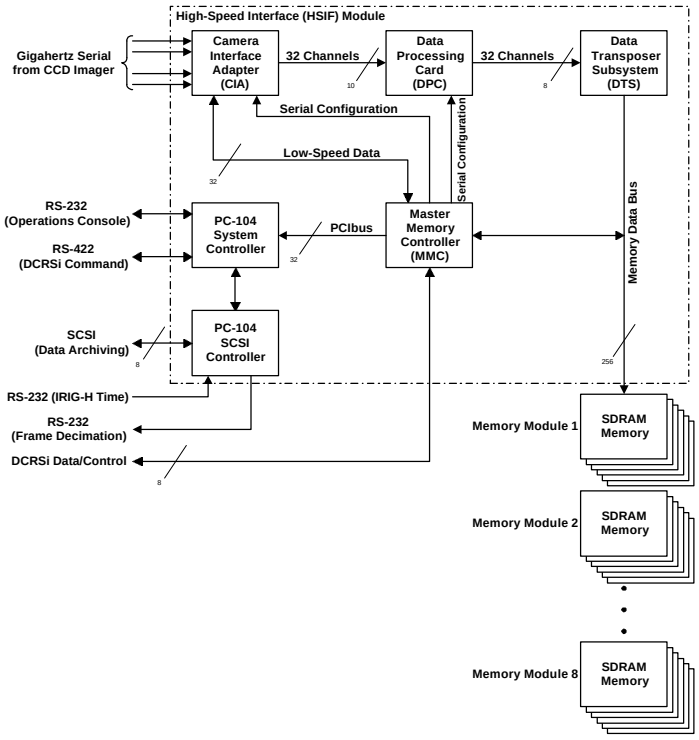

Figure 1: SSDR Design Block Diagram

The High-Speed Interface Module (HSIM) consists of the Interface Adapter, Data Processing Card, Data Transposer, and Master Memory Controller sub-modules. The primary functions of the HSIM are to accept data from a wide-bandwith source (a CCD imager, digital sensor, etc.), coordinate the transfer of data into the memory components of the Memory Modules, and coordinate the downloading of data from the memory components to the user via a selected interface port (SCSI, DCRsi™, etc.).

All the memory components of the design are contained in up to eight (8) identical Memory Modules. Each memory module consists of six (6) Memory Cards, designed in such a way that the total memory capacity of the design is limited only by available electrical power capacity and space.

CAMERA INTERFACE ADAPTER (CIA)

The CIA provides the design's specific interface to the selected imager or sensor source; this sub-module is custom-designed to interface the high-speed data source to the design's generic high-speed data port described below. The adapter for the prototype implementation of the design interfaces a 4000 frame/second, 512 X 512-pixel resolution CCD Video Imager, being developed by Silicon Mountain Designs.

As shown in Figure 1, data from the source arrives as four (4) 1.0 Gigahertz serial fiber-optic streams. The CIA converts these streams to sixteen (16) 10-bit parallel data streams, each operating at a 20 Megahertz rate. Additionally, the CIA uses the buffering capacity of the Decimation FIFOs to capture frames of data and transfer them to an external monitoring device for camera aiming or monitoring purposes.

DATA PROCESSING CARD (DPC)

The DPC sub-module provides a generic front-end to the design. This generic front-end is configured as two (2) sets of single-ended TTL channels:

- The primary input set is thirty-two (32) independent channels of 10-bit data, a Data Ready signal, and a Data Clock signal for providing high-speed (maximum 57 Megahertz burst) input of imagery or sensor data.
- The secondary input set is four (4) channels of 8-bit data, a Data Ready signal, and a Data Clock signal, providing low-speed (maximum 33 Megahertz) alternate data to the first four (4) primary channels.

Each primary channel employs one Data Processing ASIC (DPA) for processing of the associated incoming data stream; Figure 2 shows the block diagram of the DPA. The DPA

implements data compression, data blocking, and error correction encoding operations to ensure maximum density and integrity of data stored to memory.

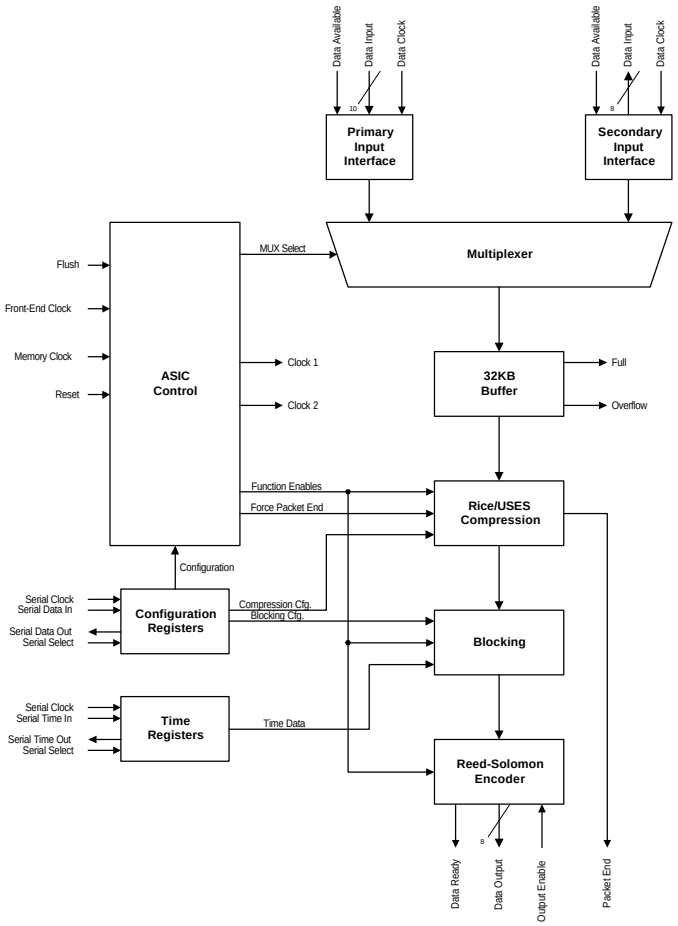

Figure 2: Data Processing ASIC Block Diagram

The DPA design employs the lossless Rice/USES compression engine. The Rice algorithm, named after its author, Robert Rice of Jet Propulsion Laboratories, was designed for NASA to compress image data from space. The code, now renamed Universal Source Encoder for Space (USES), has been greatly improved from its original form by Dr. Pen-Shu Yeh of NASA Goddard.

DATA TRANSPOSER SUBSYSTEM (DTS)

The DTS, shown in Figure 3, accepts the 32 channel data streams (with associated control signals), buffers each channel data stream, arbitrates channel buffer access to the 256-bit memory bus to the memory modules, and outputs the arbiter-selected channel buffer onto the memory bus; all these functions occur at the memory bus clock rate of 66 Megahertz.

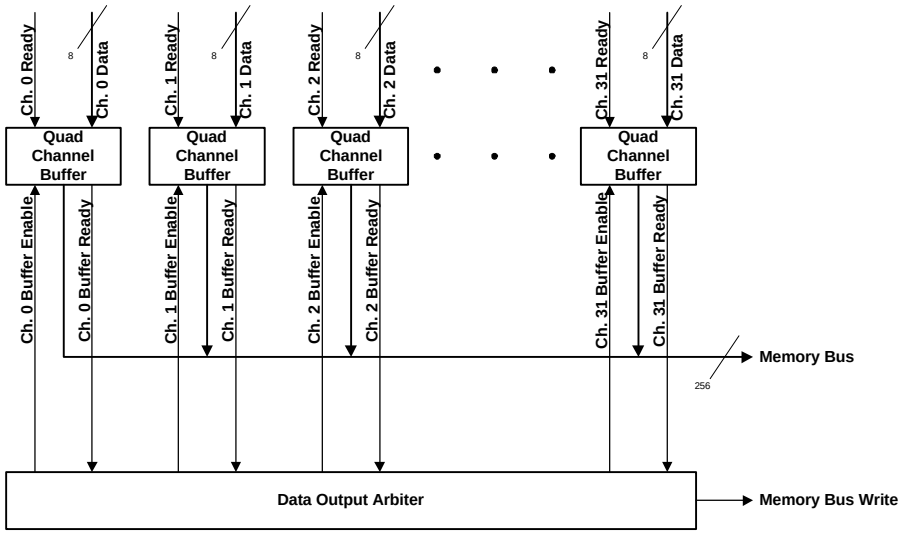

Figure 3: Data Transposer Subsystem Block Diagram

MASTER MEMORY CONTROLLER (MMC)

The MMC, a block diagram of which is shown in Figure 4, provides the low-level interface between the HSIM, Memory Module, DCRsi™, PCIbus, and error correction decoding functions. The following data flows are controlled by the MMC:

- DCRsi™-to-DPC (Low-Speed Recording) - Data input from the DCRSi™ port is routed to the four (4) Low-Speed Data ports of the DPC, where data compression, error correction encoding, or blocking information can be optionally appended before being forwarded to the memory module via the memory bus.
- Memory-to-PCIbus (Playback) - Data previously stored in the memory module is routed, via the memory bus, to the PCIbus port (with optional error correction decoding), where the System Controller may further route the data stream to PCIbus-compatible interfaces (SCSI, Fibre-Channel, etc.).
- Memory-to-DCRsi™ (Alternate Playback) - Data previously stored in the memory module is routed, via the memory bus, to the DCRsi™ port (with optional error correction decoding).
- HSIM Configuration - Data input from the PCIbus is routed to the CIA or DPC Configuration Registers for programmable selection of interface or data processing options.

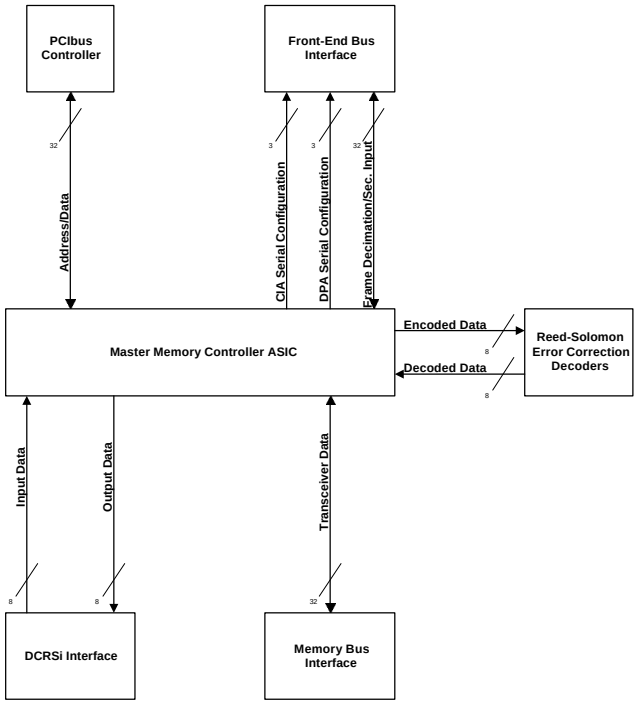

Figure 4: Master Memory Controller Block Diagram

The MMC interfaces to the 256-bit memory bus via a bank of 32-bit transceiver components. Data is clocked into or out of the transceiver bank as 256-bit data directly onto the memory bus and as 32-bit data internal to the MMC.

An interface is provided for marker data insertion into the data streams from the DPC by a serial time transfer from the MMC to the DPAs. The MMC keeps a free-running time-tag with a 10^{-4} second, synchronized with a one pulse-per-second IRIG signal from external time-code generation equipment. This marker data is serially transferred to the DPAs ten thousand times per second.

The MMC uses two AHA4011 Error Correction Encoder/Decoders, manufactured by Advanced Hardware Architectures, to facilitate error correction decoding. When error correction decoding is enabled, the MMC directs byte-wide data from the memory bus tranceivers to one of the devices. When this device becomes full and begins its' decoding cycle, data is redirected to the second device; when both devices are full and executing their decoding cycle, the MMC pauses memory data transfer until one of the devices completes its' decoding cycle and indicates ready to accept additional data. As each device becomes ready for output of corrected data, the MMC controls data flow to the destination port.

The 66 Megahertz memory bus master clock and 33 Megahertz HSIM master clock are generated by the MMC and routed through zero-latency clock distribution networks to supply one memory bus master clock for each memory sub-module and one HSIM master

clock for each of the CIA, DPC, and DTS sub-modules. Using this design, a maximum skew between distributed clock outputs of one nanosecond is achieved.

SYSTEM CONTROLLER

Overall control of the SSDR design is accomplished by a COTS 133 Megahertz Pentium™ core module in a PC-104 ***PLUS*** form factor. This module controls serial ports for Programming/Control, Frame Decimation, and DCRsi™ command control, as well as a SCSI data archiving port.

MEMORY MODULE

Synchronous DRAM (SDRAM) memory for the design is contained within the Memory Module. The module is partitioned into up to eight (8) sub-modules of six (6) memory cards each. All data and SDRAM control signals are redriven between memory cards to minimize signal skew through the module.

Figure 5 shows the packaging arrangement of memory cards into sub-modules. A sub-module is constructed by stacking memory cards using elastomeric conductive polymer interconnects (ECPI) to provide interconnect between cards. A metallic frame is placed between memory cards to provide a thermal path from the memory card components to the chassis side wall. Finally, connector cards are placed on either side of the resulting memory card stack to provide the mechanical connections to the memory bus and the entire stack is compressed together using standard hardware to bring the ECPIs into solid contact with the memory card etch.

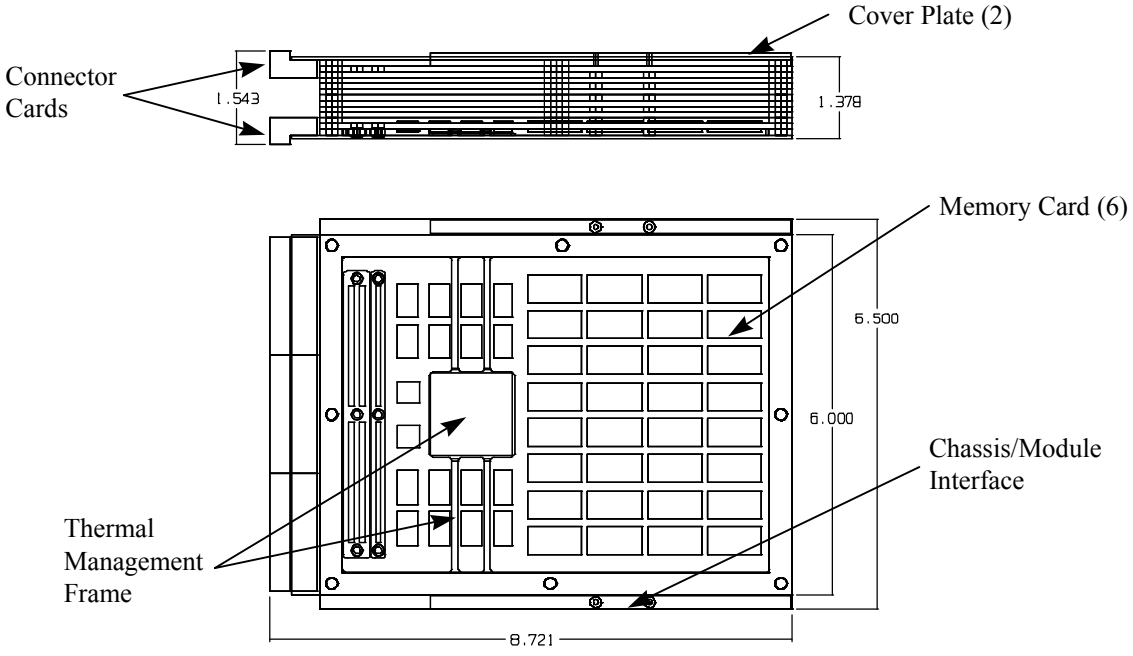

Figure 5: Memory Module Packaging

MEMORY CARD

Each memory card contains sixty-four (64) 64 Megabit SDRAM components, for a total of 4 Gigabits (0.5 Gigabyte) of storage capacity per card, 24 Gigabits (3 Gigabytes) per module, and a total capacity of 192 Gigabits (24 Gigabytes) for the entire Memory Module. Assuming a 2:1 compression ratio using the RICE/USES compression engine, this translates to a maximum theoretical storage capacity of 384 Gigabits (48 Gigabytes). Only one memory card is fully active at a time to reduce power consumption.

Memory fills or empties from the back (last memory card of the last memory sub-module) forward in response to memory read/write operations. As each memory card fills or empties, its' transceiver bank places all outputs onto the memory bus in the high-impedance state and the next memory card forward enables its' transceiver bank onto the memory bus. Memory cards are capable of both single read/write or multiple burst read/write operations. SDRAM refresh is accomplished between read/write cycles under the control of the Memory Controller ASIC.

Memory card clock distribution of the 66 Megahertz memory bus clock is accomplished using a zero-latency clock distribution network similar to the ones in the MMC design. This clock network isolates the memory card internal clocking from the memory bus clock, thus presenting a one-unit load to the master clock from the MMC per memory sub-module.

POWER DISTRIBUTION

Power for the design is supplied by eight (8) DC/DC Converters, mounted between the backplane and chassis bottom plate, as shown in Figure 8. Two of the converters supply +5.0 VDC to the HSIM, while the other six supply +3.3 VDC to the HSIM and Memory Module. Heat generated by the converters is transferred to the chassis bottom by heat sinks integrated into the bottom of each converter, satisfying the requirement of heat transfer via conduction only. The design requires +28VDC power at 34.5 Amps maximum.

FUTURE WORK

At the writing of this paper, SPEC has initiated a contract to develop a non-volatile version of the design capable of a 2 Gigabit/second data rate. The High-Density Recorder (HDR), code named Tornado 2™, will replace the Tornado 10™'s 256-bit parallel memory bus with a gigabit-rate serial token-ring data link. Memory Modules will consist of banks of 256 Megabit EEPROM components arranged so that pages of data may be written and programmed into the EEPROMs without interruption to data flow. The HSIM and each Memory Module will be housed in ARINC-standard ¼ ATR Long chassis, each providing

its' own power. A high-speed memory bus interface will also be designed into the HDR to enable data recorded by the Tornado 10™ to be offloaded or backed-up to the Tornado 2™.

CONCLUSION

The SSDR discussed in this paper satisfies the need for a ruggedized, high-bandwidth solid-state data recorder. Full configurability allows for independent application of lossless data compression, forward error correction, and data blocking without impeding the 10.4 Gigabit/second sustained data rate. SDRAM components provide up to 24 Gigabytes (uncompressed) of data storage capacity.

ACKNOWLEDGEMENTS

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BIOGRAPHY

Mr. Richard J. Wise, Jr. holds a Bachelor of Science degree in Electrical Engineering from Louisiana State University in Baton Rouge, La. and joined SPEC in January, 1997 as a Senior Electrical Design Engineer, specializing in PLC and FPGA design. Mr. Wise has over 25 years experience in Electrical Engineering and 16 years experience in tactical data link design.

Since coming to SPEC, Mr. Wise has designed the Data Transposer Subsystem (DTS) and the Master Controller for the Solid-State Data Recorder (SSDR) program. The DTS is a single-board subsystem designed to multiplex 32 independent byte-wide channels onto a 256-bit-wide memory bus at a 66MHz rate. The Master Controller, also a single-board subsystem, is designed to control the operation of the SSDR unit and interface SSDR memory data to DCRsi™ Tape Transport units.

Mr.Wise served as a Design Specialist on the PLSS, Aquila RPV, and L245 programs for Lockheed Missiles & Space Co., Inc. He has designed a high-speed VME interface, which has been used in unmodified form on numerous Lockheed tactical data link modules and

served as the baseline for the VXI interface designed for SPEC's DRFM module. While in Lockheed's employ, Mr. Wise developed and designed a multi-function, 256-word Specific-Application Sorter/Histogrammer (SASH) hardware coprocessor for VME-based applications, as well as the digital hardware and software for a Radio Frequency Calibration System for the U.S. Air Force.

Prior to joining Lockheed, Mr. Wise was employed by International Paper Co. as a Project Engineer. His accomplishments were the development, design, integration, test, installation, and operator training of Direct Digital Control (DDC) systems for various papermaking processes (Batch/Continuous Digesters, Recovery Boilers, Bleach Plants, and high-speed Paper Machines).