An IF Sampling Digital Receiver Implementation for Space-based Command and Telemetry Applications

Bruce W. Maples, MSEE
Keith A. Fix, MSEE
CMC Electronics Cincinnati
Mason, OH 45040

ABSTRACT

This paper describes an approach to the implementation of an IF sampling digital receiver for low data rate command and telemetry applications in the NASA Goddard Spaceflight Tracking and Data Network (STDN) and Air Force Space-Ground Link System (SGLS). The digital design is targeted for an FPGA-based implementation and was written entirely in VHDL. Several size and clock reduction techniques are described which were utilized due to limited gate-array resources and power. The system-level design architecture is described followed by a discussion of algorithms and performance of critical stages in the receiver chain. Bit error performance of the prototype receiver is also presented. Finally, although this design is specifically targeted for a narrowband command and telemetry application, the methodology forms the basis of a configurable receiver for higher data rate applications.

KEY WORDS

IF Sampling, Digital Receiver, Spaceflight Tracking and Data Network (STDN), FPGA, VHDL.

INTRODUCTION

The receiver described in this paper was designed for low data rate (2 kbps) command and telemetry STDN applications at S-band frequencies (2025-2110 MHz). The modulation format of the STDN waveform may be described as a BPSK modulated 16 kHz subcarrier linear phase modulated (PM) onto a main carrier with a modulation index of 1.0 radian.

The receiver is divided into four major assemblies; the S-Band downconverter assembly, IF assembly, digital demodulator assembly and the power supply assembly. It is partitioned along logical functional boundaries to provide isolation of RF, digital and power segments as well as providing manufacturability and testability necessary for a product that is cost effective to produce. Mechanically, each of the four major assemblies represent a separate slice which together comprise the complete receiver unit. A system-level functional block diagram of the STDN receiver is shown in Figure 1.

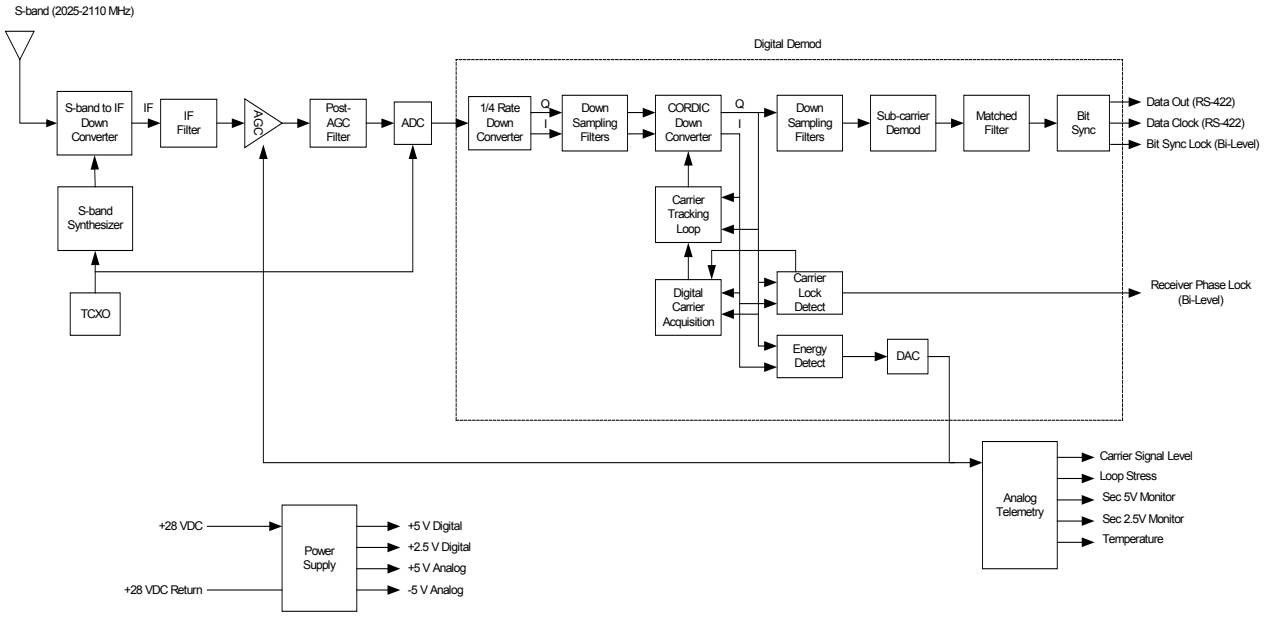

Figure 1. STDN Digital Receiver System-level Block Diagram

The digital portion of the receiver, which is the primary focus of this paper, consists of the functional blocks within the dashed outline. The RF/IF section, prior to the A/D converter, is analog and performs the functions of bandlimiting, gain, and downconversion to a suitable input frequency for the A/D converter.

RF/IF FRONT END

The RF front-end utilizes a single conversion superheterodyne architecture to produce the IF input frequency to the A/D converter and digital demodulator. A detailed functional block diagram of the RF/IF strip is shown in Figure 2.

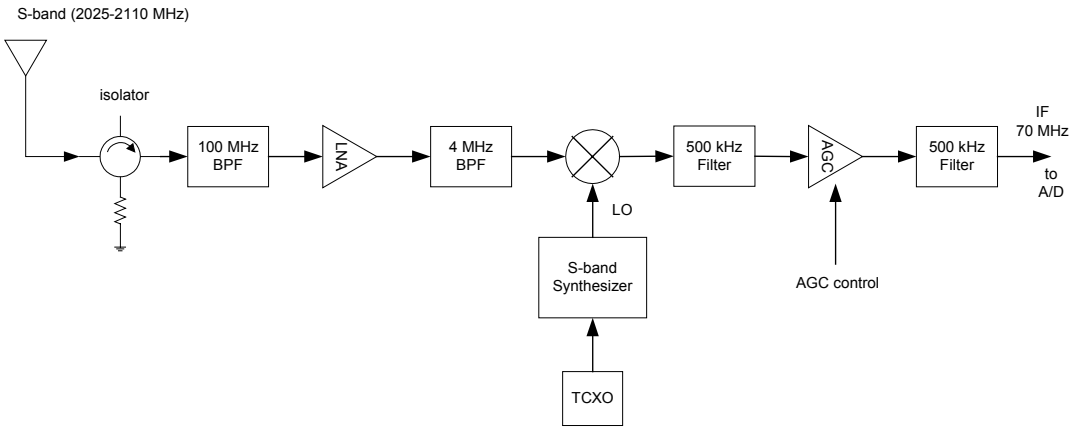

Figure 2. RF/IF Functional Block Diagram

The S-Band downconverter accepts RF input signals in the frequency range from 2025-2110 MHz and performs a fixed downconversion to an IF of 70 MHz. For flexibility, the local oscillator (LO) is synthesized allowing the input signal frequency to be preset in 80 kHz steps within the 2025-2110 MHz range. Out-of-band interfering signals are suppressed a minimum of 60 dB by two bandpass filters prior to the mixer. In practice, a user defined nominal operating input frequency is specified to allow the custom selection of the narrower of these two filters (post-LNA). The center frequency and bandwidth are chosen carefully with respect to the desired operating data rate for the purpose of maximally reducing the total noise power and interference into the front-end mixer. For this particular design, a nominal input frequency of 2042 MHz was selected along with a 4 MHz wide post-LNA bandpass filter.

Following the mixer, the IF signal is further bandlimited to remove mixing and intermodulation products as well as reduce total noise power. In addition, these post-mixing filters serve the critical function of providing anti-alias filtering for the digital demodulator. The anti-alias filter is crucial to the performance of an IF sampling digital receiver and must be carefully selected to provide sufficient out-of-band rejection to achieve the desired sensitivity design goal. For this application, a cascade arrangement of 500 kHz filters was used to obtain greater than 100 dB of stopband rejection. The design goal for receiver sensitivity was –130 dBm.

A multi-stage AGC maintains the IF signal at a fixed level to the input of the A/D converter. The output of the A/D converter is then applied to the digital demodulator. The AGC allows the receiver to have sufficient linear dynamic range in the presence of varying input signal levels as well as to avoid overdriving the input to the A/D, thus causing distortion resulting in poor receiver performance. The gain of the AGC is varied via an analog control voltage generated by the digital receiver driving a D/A converter. For this design, the AGC provides a total of 80 dB of dynamic range.

DIGITAL DEMODULATOR

The digital demodulator translates the STDN waveform from the 70 MHz IF to baseband and produces a demodulated output data stream and clock. A detailed functional block diagram of the digital demodulator is shown in Figure 3.

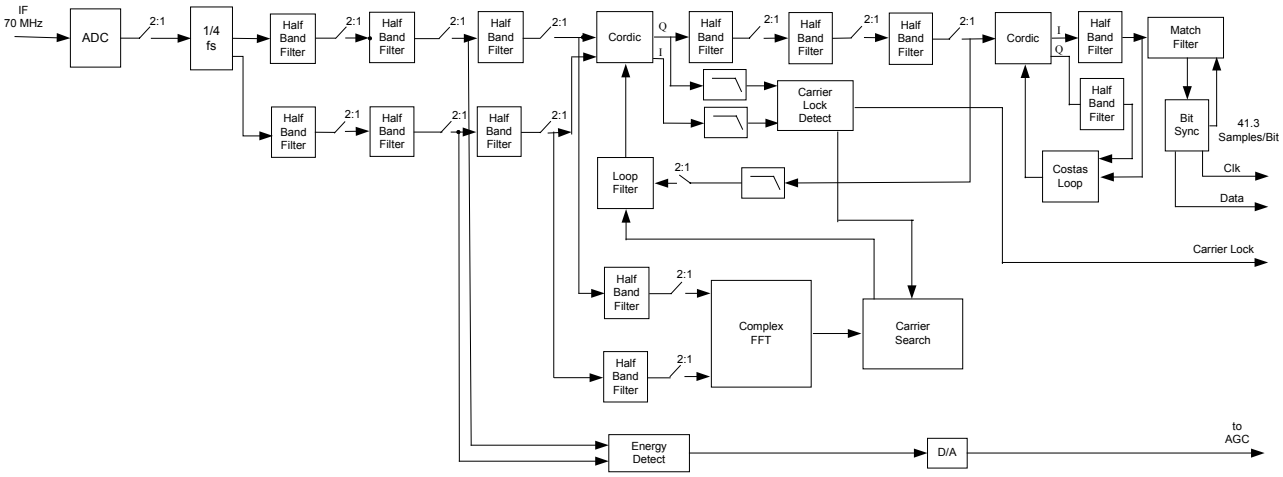

Figure 3. Digital Demodulator Functional Block Diagram

The bandlimited 70 MHz IF is undersampled by an A/D converter and decimated by a factor of 2 to produce an image of the desired signal at a convenient lower frequency[1]. This image is an exact copy of the desired waveform, resulting from the sampling process, which may then be processed at a significantly reduced clock rate compared to that required for direct baseband sampling of the 70 MHz input waveform. The Nyquist criteria states that a signal must be sampled at a rate equal to or greater than twice its bandwidth in order to preserve all the signal information. The absolute location in frequency of a band of signals is only constrained to lie completely within a single Nyquist zone, each of which is defined as a multiple of half the sample rate. This concept is illustrated in Figure 4 which shows the desired 70 MHz waveform located in the 27th Nyquist zone and the resulting lowest image located at approximately 1.321 MHz (0.25fs).

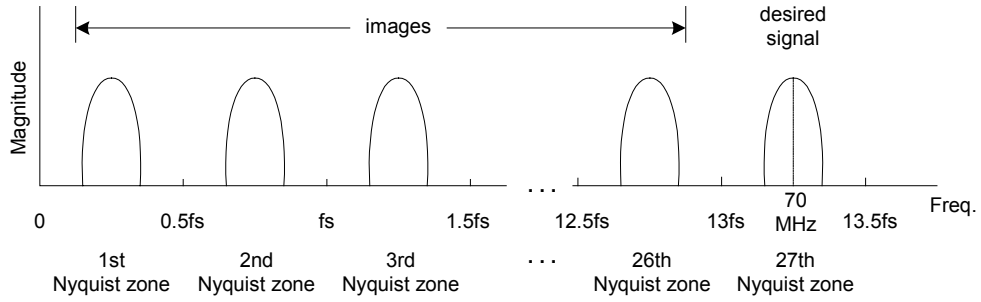

Figure 4. Spectral Images Resulting from Undersampling of Analog Waveform

A convenient formula relating the sampling frequency f_s to the desired signal center frequency f_c and the Nyquist zone N is given by,

$$f_s = 4f_c /(2N-1) \text{ (Hz)} \quad \text{where, integer } N \geq 1 \qquad \text{(eq. 1)}$$

[1] The 2:1 decimation is permitted at this point due to the band limiting provided by the anti-aliasing filters prior to the A/D. The higher sample rate is used to optimize the operation of the A/D converter.

Equation 1 determines a sampling frequency which ensures the desired signal center frequency f_c is located in the center of a Nyquist zone. In addition, the Nyquist criterion must of course be satisfied for the bandwidth of the waveform of interest. Signals which cross Nyquist zone boundaries will result in undesirable aliasing across the entire spectrum. This becomes an important consideration in the tradeoff of selecting a sampling frequency which is high enough to spread the images sufficiently to permit the use of simpler anti-alias filters and low enough to serve as a convenient clocking frequency for the hardware devices. Ultimately, the total stopband rejection of the anti-alias filter is a critical design factor in determining receiver sensitivity, dynamic range and overall performance.

It can be seen from Figure 4 that sampling of signals above the first Nyquist zone is equivalent to analog downconversion by producing an exact image of the desired signal in the first Nyquist zone. This image may then be further translated to baseband by complex mixing with its center frequency; in this case 1.321 MHz (0.25fs). The 1st Nyquist zone image centered at one-quarter f_s permits the use of a convenient frequency translation technique known as "quarter rate translation" which does not require the use of multiplication. From a digital hardware synthesis consideration, especially with limited FPGA gate resources, multipliers are generally to be avoided if possible due to their size and complexity. Quarter rate translation is performed by applying in-phase and quadrature mixing sequences to the input samples as follows,

In-phase sequence:	1, 0, -1, 0, ...
Quadrature sequence:	0, 1, 0, -1, ...

It can be seen that the two sequences are shifted by one sample relative to each other to produce phase quadrature. For each incoming sample we either apply a change of sign, zero the sample or no change to generate the in-phase and quadrature data streams. No multiplication has occurred and the 1st Nyquist zone image has been translated to baseband. Digital low pass filtering is subsequently performed to eliminate the higher frequency images. Referring to the functional block diagram of Figure 3, the quarter rate downconversion block and subsequent filtering are shown following the A/D converter.

Another digital resource saving structure is the half-band filter so called due to the nature of its frequency response. The half-band filter has the advantage of requiring no multipliers and delivering a frequency response whose 3 dB cutoff is at half the folding frequency (i.e. $f_s/4$) with a total stopband rejection of approximately 20 dB per stage. A block diagram of a single stage half-band filter architecture is shown in Figure 5.

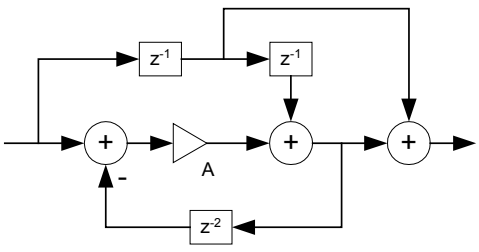

Figure 5. Single-stage Half Band Filter Structure

The transfer function of the half-band filter is given by,

$$H(z) = (A+z^{-1}+z^{-2}+Az^{-3}) / (1+Az^{-2}) \qquad \text{(eq. 2)}$$

The transfer function coefficient A may be selected to be powers of two ($1/2^n$) requiring only a bit shift to implement in hardware. Once again, multipliers have been avoided resulting in considerable savings in logic resources. For this design, a series of three dual-stage half-band filters in both the in-phase and quadrature channels were implemented. Each dual-stage filter was followed by a decimation-by-2 to reduce the total clock rate required for subsequent processing.

In practice, the desired signal may experience frequency shifts from the nominal carrier frequency due to Doppler, oscillator error, temperature drift, etc. The down conversion process to this point has, in reality, only produced a near baseband complex output that is offset by the uplink Doppler, transmitter and receiver frequency errors. Following the string of half-band filters and decimation is a complex CORDIC[2] downconverter for the purpose of resolving the remaining frequency offset. The CORDIC algorithm provides phase angle estimation via an iterative process. This algorithm requires no sine/cosine look-up table and only requires a single tangent value for each stage of the CORDIC. For this design, a ten stage CORDIC was implemented which provided sufficient phase angle resolution to meet specified requirements. This algorithm requires no multiplications and no PROM resulting in a significant reduction in implementation complexity. A block diagram of the complex CORDIC digital downconverter is shown in Figure 6.

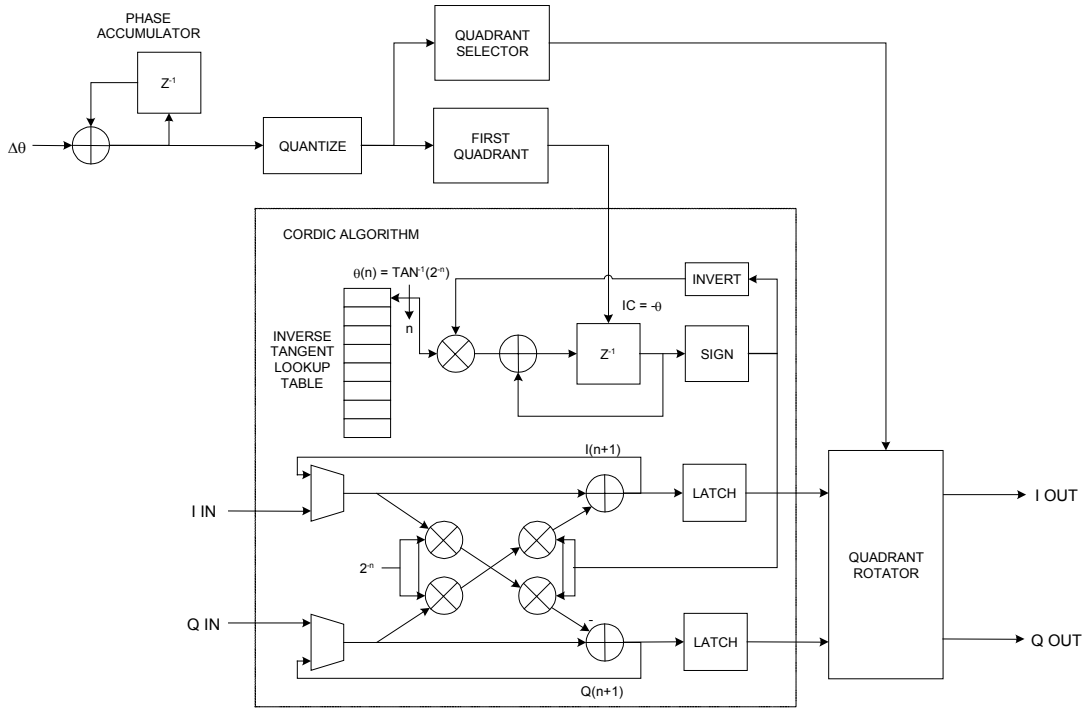

Figure 6. Complex CORDIC Downconverter

[2] CORDIC is an acronym for COordinate Rotation DIgital Computer. It is a method for calculating trigonometric functions, such as sine and cosine, which was described by Jack E. Volder in 1957.

The $\Delta\theta$ (phase error adjustment) feeds the phase accumulator which generates the phase angle for the CORDIC algorithm. This implementation of the CORDIC uses a ten stage iterative process to reduce the phase angle input to zero. An inverse tangent lookup table, related by powers of two, is used for this calculation. This process rotates the in-phase (I) and quadrature (Q) vectors to match the phase angle input. Since this implementation of the CORDIC only operates in one quadrant, the two MSBs of the phase angle must be used to perform a quadrant rotation. The output of the quadrant rotator provides the down converted I, Q outputs.

Referring once again to Figure 3, the output of the three stages of half band filters (I and Q) also feed a single half-band filter stage and decimator prior to the complex FFT. The I and Q outputs of the CORDIC are fed to low pass filters (digital single-pole RC) and then to carrier detect integrators. The Q channel output of the CORDIC is used as the phase detector of the carrier phase lock loop (PLL). When the loop is locked, the Q channel will have an average value of zero and the I channel will have an average DC value. The Q channel is digitally filtered and decimated prior to the proportional/integrator loop filter. The loop filter phase error output provides the step adjustment ($\Delta\theta$) of the phase accumulator clocked at the input sample rate of the complex CORDIC downconverter. The output of the phase angle accumulator becomes the differential phase angle input to the CORDIC.

A complex FFT was implemented to perform an energy search within the sample bandwidth (+/-165 kHz) to estimate the carrier offset of the desired signal. This estimated carrier offset is used to drive the digital PLL which controls the complex CORDIC to remove the remaining frequency offset. The advantage of this approach is the ability to move the CORDIC directly to the desired signal location in one clock cycle rather than a sweep method requiring multiple cycles. In this design, a 256-point decimation-in-frequency FFT was implemented providing a resolution bin width of approximately 1.3 kHz. A single multiplier was used in the FFT implementation.

Carrier acquisition begins by performing a complex FFT on the filtered I and Q samples. To achieve the desired sensitivity goal of –130 dBm RF input level, multiple FFT's are performed and integrated to provide sufficient noise filtering to accurately estimate carrier offset. The estimated carrier offset drives the digital PLL.

Carrier lock is determined by comparing the integrated I channel samples with the scaled integrated absolute value of the Q channel samples as given by,

$$\Sigma I > k \Sigma |Q| \quad \text{where, k is a constant} \qquad \text{(eq. 3)}$$

The scale factor k represents the lock threshold and the integration interval is determined based on probability of acquisition and probability of false lock requirements. When carrier lock is detected, the acquisition mode is suspended and tracking mode begins. The PLL bandwidth is selected to allow the loop to track Doppler induced carrier frequency variations. For this design, a loop bandwidth of greater than 30 Hz is required to track a worst case Doppler rate of 750 Hz/sec.

For the STDN waveform, the 2 kbps command and telemetry information signal is located on a 16 kHz subcarrier relative to the main carrier. The Q channel output of the complex CORDIC downconverter contains the modulated subcarrier energy. The 16 kHz subcarrier requires another

down conversion, which is performed by a second digital CORDIC downconverter. Prior to the second CORDIC, the signal is again processed through three stages of half-band filters and decimators to further reduce the sample rate. The second CORDIC downconverter utilizes a decision directed Costas loop to acquire and track the 16 kHz subcarrier. Figure 7 shows a block diagram of the decision directed Costas loop with complex CORDIC.

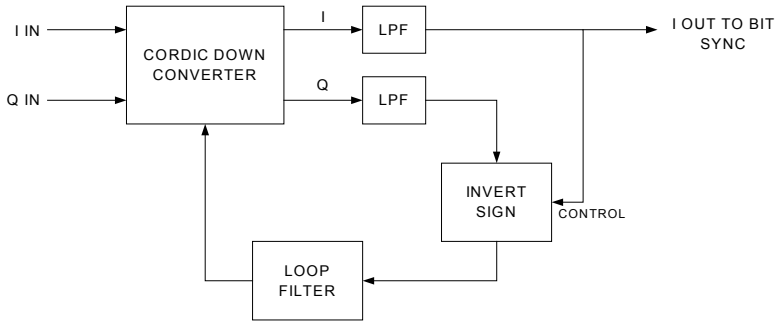

Figure 7. Decision Directed Costas Loop with Complex CORDIC Downconverter

The loop filter parameters are adjusted to meet the particular specifications of the 16 kHz subcarrier. The loop filters' phase error output provides the step adjustment to a phase accumulator whose output then becomes the differential phase angle input to the second CORDIC. The phase accumulator is clocked at the input sample rate of the CORDIC.

The I channel output of the second CORDIC downconverter contains the baseband 2 kbps data. This data is half-band filtered (LPF) to remove the double frequency mixing product (present in this case since the Q input is zero) and passed along to an integrate and dump (I&D) filter and early-late gate bit synchronizer which provides clock and data recovery of the received 2 kbps data stream.

MEASURED PERFORMANCE

The S-band digital receiver architecture described in this paper has been constructed as an engineering brassboard and performance measurements taken. Several key measurements are listed in Table 1 relative to their specification goal.

Table 1. Specification Goal vs. Brassboard Measured Performance

Specification Description	Specification	Measured Performance
Threshold at BER 1E-6	-117 dBm	-123 dBm (1,2)
Acquisition Threshold	-122 dBm	-138 dBm (1)
Acquisition Range	± 94 kHz	> ± 110 kHz

Notes:
1. Measured without S-Band front end filter; additional loss < 1 dB
2. Measured without NRZ-L to M conversion; additional loss < 1 dB

In addition, bit-error-rate (BER) performance was measured on the brassboard configuration. Figure 8 shows the error probability curve for the S-band receiver brassboard compared to BPSK after adjusting for noise figure and cable losses of the front-end (3.7 dB) and modulation loss due to the modulation format (4.1 dB). The remaining difference in performance relative to BPSK theoretical is approximately 0.6 dB representing the digital implementation loss.

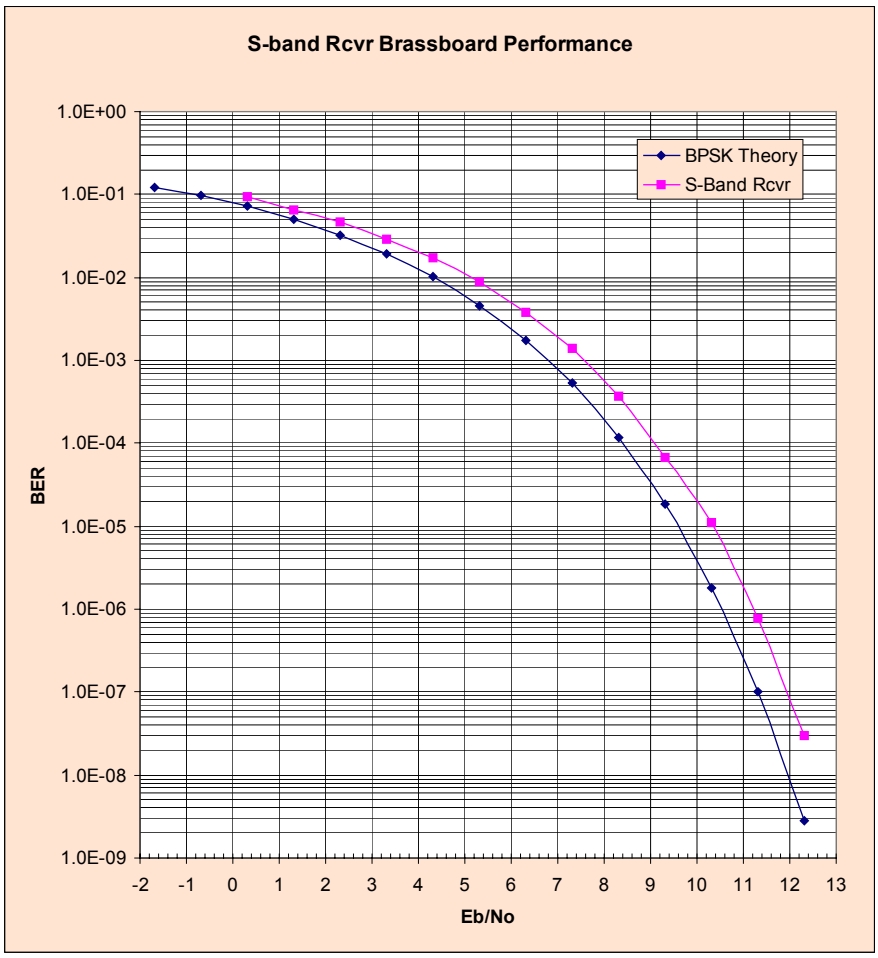

Figure 8. S-band Receiver Brassboard Error Probability vs. Eb/No

CONCLUSIONS

This paper presented several digital receiver design techniques which are important in reducing size and power requirements for resource limited FPGA-based implementations. The digital demodulator portion of this design was implemented entirely in VHDL and targeted for two radiation hardened Actel FPGA's suitable for spacecraft applications. Finally, the use of VHDL and the reprogrammability of the target hardware allows the relatively easy addition of other waveforms or modes such as SGLS, TDRSS, etc. as requirements dictate.

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Biography of Bruce Maples

Bruce Maples graduated from the University of Toledo in 1978 with a Bachelors of Science in Electrical Engineering. Following graduation he worked for Motorola Corporation as a design engineer. He later returned to the University of Toledo on a research assistantship through NASA and graduated in 1984 with a Masters of Science in Electrical Engineering. Since then he has worked for Space Communications Co., M/A-Comm Governments Systems, Inc. and CMC Electronics Cincinnati. He has been with CMC Electronics since 1988 as a member technical staff and most recently manager of internal research and development for the space communications group. His experience includes digital/analog communication system design, satellite communications, coding and information theory, digital signal processing, embedded system design and systems engineering.

Biography of Keith Fix

Keith Fix graduated from Purdue University in 1982 with a Bachelors of Science in Electrical Engineering and in 1984 with a Masters of Science in Electrical Engineering. After graduation he went to work for S.E.A. Corporation designing digital hardware for industrial control bus products. He began work for CMC Electronics Cincinnati in December 1985 as a member of technical staff and is now a Senior Design Engineer. His background includes hardware and software design and development of embedded DOD communications equipment in his earlier years with CMCEC. More recent experience involves communications system design, DSP algorithm design, VHDL design, digital and analog hardware design, and limited application software design for space communications products.