200 MBPS TO 1 GBPS DATA ACQUISITION & CAPTURE USING RACEWAY

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ABSTRACT

For many years VME has been the platform of choice for high-performance, real-time data acquisition systems. VME's longevity has been made possible in part by timely enhancements which have expanded system bandwidth and allowed systems to support ever increasing throughput. One of the most recent ANSI-standard extensions of the VME specification defines RACEway, a system of dynamically switched, 160 Mbyte/second board-to-board interconnects. In typical systems RACEway increases the internal bandwidth of a VME system by an order of magnitude. Since this bandwidth is both scaleable and deterministic, it is particularly well suited to high-performance, real-time systems.

The potential of RACEway for very high-performance (200 Mbps to 1 Gbps) real-time systems has been recognized by both the VME industry and a growing number of system integrators. This recognition has yielded many new RACEway-ready VME products from more than a dozen vendors. In fact many significant real-time data acquisition systems that consist entirely of commercial-off-the-shelf (COTS) RACEway products are being developed and fielded today.

This paper provides an overview of RACEway technology, identifies the types of RACEway equipment currently available, discusses how RACEway can be applied in high-performance data acquisition systems, and briefly describes two systems that acquiring and capturing real-time data streams at rates from 200 Mbps to 1 Gbps using RACEway.

KEYWORDS

Data Acquisition, VME (Versa Module Eurocard), VSB (VME Subsystem Bus), HIPPI (High Performance Parallel Interface), RACEway, Instrumentation Recorders, ID-1 Recorders, DCRsi, High-performance real-time systems, Fibre Channel RAIDs.

INTRODUCTION

RACEway expands the internal bandwidth of standard VME systems by allowing each RACEway-ready board to establish a 160 Mbyte/second point-to-point connection to another RACEway-ready board. An active backplane overlay known as the RACEway Interlink dynamically manages these connections, allowing multiple independent 160 Mbyte/second channels to operate simultaneously in the same VME chassis. In this architecture, internal bandwidth scales with the number of boards in the system, a significant advantage over a multi-board shared bus architecture. Additionally, the system designer can guarantee that bandwidth will be available between two critical real-time functions, which is not always the case in systems that rely on system buses (VME or PCI) for data transfer. These features make RACEway particularly well adapted to high-rate data acquisition applications where a deterministic data flow can be pipelined through one or more functional elements.

The recent advent of a wide variety of COTS RACEway products has propelled RACEway from being simply an interesting technology into a really useful technology that can be applied to solve difficult real-time data acquisition problems. In fact, many RACEway-based acquisition systems have been developed and fielded. These systems are performing at throughput levels not attainable using other standards-based COTS equipment.

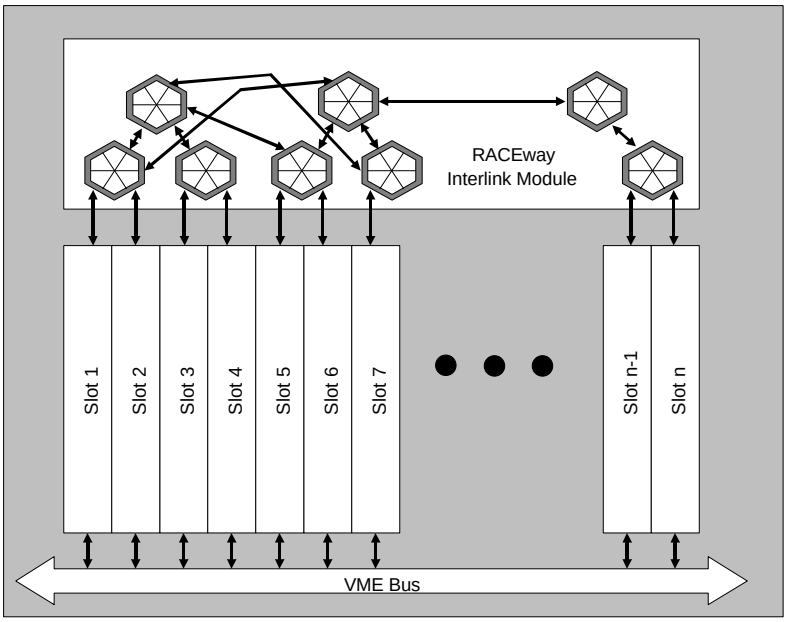
This paper discusses how COTS RACEway equipment can be used to acquire, record, and communicate real-time data streams ranging from 200 Mbps to 1 Gbps. First, an overview of RACEway technology is provided, including a review of the functionality that can be implemented with commercially available RACEway equipment. Then, specific examples of high-throughput real-time systems that incorporate RACEway and high-performance instrumentation recorders (ID-1 and DCRsi) are discussed.

RACEWAY - A SWITCHED FABRIC INTERCONNECT FOR VME ENVIRONMENTS

The RACEway specification (ANSI/VITA 5-1994, see references) defines a standard usage of the VME P2 connector’s A and C rows (“User Defined” pins in the VME

specification) to provide an additional high-speed mechanism for transferring large volumes of data between boards. RACEway uses these pins to implement a dynamically switched, point-to-point interconnect system, also known as a switched fabric (figure 1). Since RACEway uses only P2 rows A and C, it can operate concurrently with VME or VME64 operations. In fact, since all RACEway connections are point-to-point, RACEway operates more reliably with VME64 than other standard P2 interconnects that are bused and can create cross-talk problems (such as the VME Subsystem Bus, VSB).

Figure 1 - The RACEway Switched Fabric in a VME Environment



The central element of a RACEway interconnect system is the Interlink. The Interlink is a network of six-port crossbar switches that establishes point-to-point connections between boards in a VME/RACEway environment. Physically, the Interlink is an active P2 overlay that mates to the rear of a VME backplane (similar to VSB overlays). The slots encompassed by the overlay determine the boards that may participate in RACEway connections. Interlinks can encompass a variable number of slots; for example 4, 8, and 16 slot RACEway Interlink modules are commercially available.

Data transfers across RACEway are initiated when a master board writes a “routing word” and slave address to the Interlink. The Interlink module receives this information and establishes a connection to the requested slave board. The slave board determines whether a read or write operation has been requested and signals when it is ready to accomplish the data transfer. The Interlink manages actual data transfer on a 2 kbyte burst basis. When both the sender and receiver are able to accomplish a 2 kbyte burst, the Interlink allows the burst to occur. RACEway bursts always occur at 160 Mbytes/second (32 bit

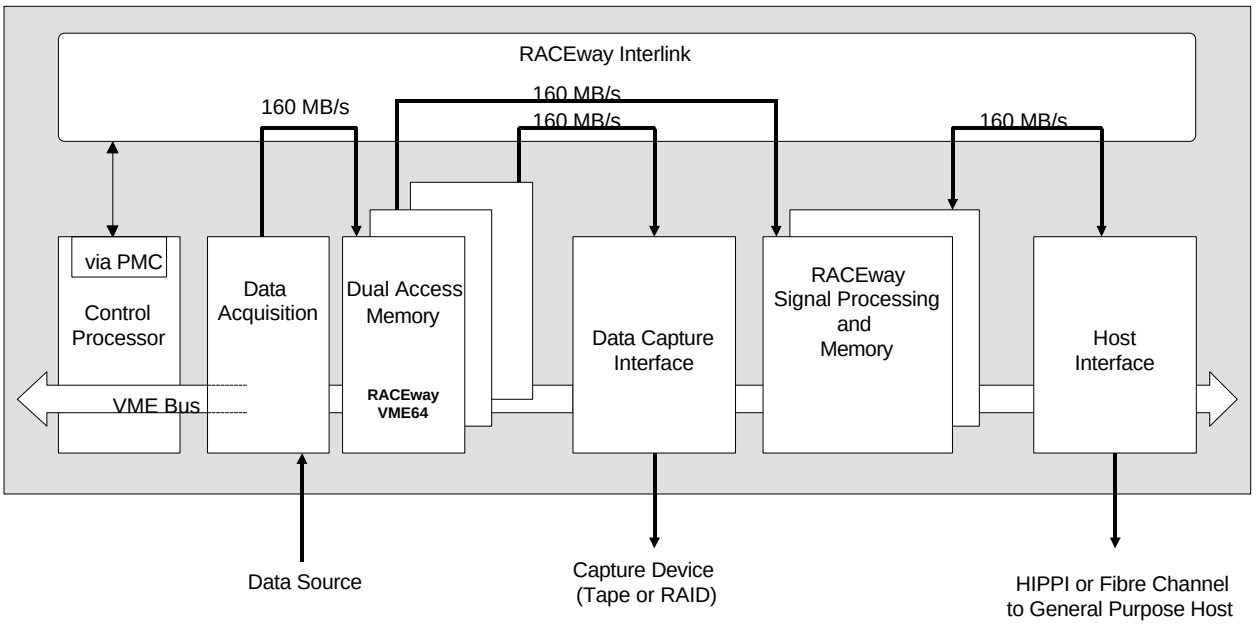
synchronous transfers at 40 MHz). The Interlink is also capable of interleaving bursts from several RACEway masters to a single RACEway slave.

The RACEway specification also allows for adaptive routing, split reads, broadcasts, and multicasts. Although these features may be interesting, they are not central to the use of RACEway as a real-time architecture. Additionally, all RACEway-ready equipment is not required to support these features, so it may not be prudent to design a system assuming these features will be available.

RACEWAY APPLIED TO REAL-TIME SYSTEMS

The real-time system designer can take advantage of RACEway's multiple data paths by pipelining the data flow through the system. Figure 2 illustrates a typical RACEway-based data acquisition system. In this example, a rotating set of three RACEway memory boards is used to buffer high-rate, real-time data. As data are acquired, they are written to one memory board. When that memory is filled, the acquisition switches to the second memory, while a data capture board extracts data from the first memory for recording on high-rate tape or Fibre Channel RAIDs. When the second memory is full, acquisition switches to the third memory, data capture switches to the second memory, and signal processors begin operating on data in the first memory. The signal processors can also use RACEway to pass data to additional signal processing boards or a high-performance workstation/supercomputer via ANSI-standard HIPPI or Fibre Channel communication channels. In this example, the VME bus is used for control only.

Figure 2 - Real-Time RACEway System Provides Multiple 160 Mbyte/second Channels



The above example illustrates a nine-board system with an internal bandwidth of 640 Mbytes/second (via RACEway) and 80 Mbytes/second (via VME64). This internal bandwidth is considerably higher than can be achieved with industry-standard bus systems (133 and 266 Mbytes/second for 32 and 64 bit PCI, for example).

While internal bandwidth provided is high, it is the scalability and determinism of RACEway channels that are the major advantage in real-time systems. In systems where data are passed from one element to the next (such as the example above), scalability is vital in achieving high throughput. In RACEway's switched architecture individual communication channels are available between each functional element (board), in a bused system all functional elements compete for use of a single bus. This distinction allows a RACEway-based system that include multiple functional element to support input streams up to 1 Gpbs where conventional bus architectures cannot.

Deterministic performance is the second major feature of RACEway important to real-time systems. Individual RACEway links can be dedicated to real-time data paths, insuring that the required bandwidth will be available when needed. In a bused system a time-critical data transfer may be delayed when the single data pathway is occupied with non-critical data or by relatively slow control messages.

RACEWAY BUILDING BLOCKS

Widespread industry support has been one of the keys to the success of VME. A large community of vendors offers a wide spectrum of products, many of which are tailored to real-time systems. Since RACEway is fully compatible with VME, it benefits from the great variety of VME products. More importantly, since the adoption of RACEway as an ANSI standard in June 1994, a growing number of manufacturers are supporting RACEway-ready versions of their VME products. COTS RACEway board-level products are available for data acquisition, digital signal processing, recorder interfaces, high-speed communication channels, and a variety of other functions (table 1). There are also chip-level products and foundation boards available to assist in the development of application-specific RACEway boards.

The variety of RACEway-ready products currently available coupled with the ability to integrate these products with standard VME equipment enables the system designer to configure a complex, high-performance real-time system using off-the-shelf products. In fact, the range of VME/RACEway off-the-shelf products is broader than other technologies.

Table 1 - RACEway Products

Type	Description
Analog & Digital Input/Output	Analog I/O to 400 Mhz, Digital Receivers, Serial I/O
Memory Boards	128 Mbyte to 2 Gbyte per board
Digital Signal Processors	Intel I860, Power PC, SHARC, TI320C40, TI320C80, Custom
Single Board Computers (SBC)	Various via PMC sites on SBC
Communication Channels	HIPPI (100 Mbyte/sec) Serial HIPPI (fiber optic, 100 Mbyte/sec) Fibre Channel Custom fiber optic (500 Mbaud)
Storage Connections	Fibre Channel RAID SCSI2/Ultra SCSI RAID ID-1 Recorders Ampex DCRsi
Foundation Boards	PMC Carrier General I/O Motherboard
Interlink Modules	4, 8, 16 slot
Chip-sets, Bridges	RACEway/PCI FIFO to RACEway chipsets PMC modules

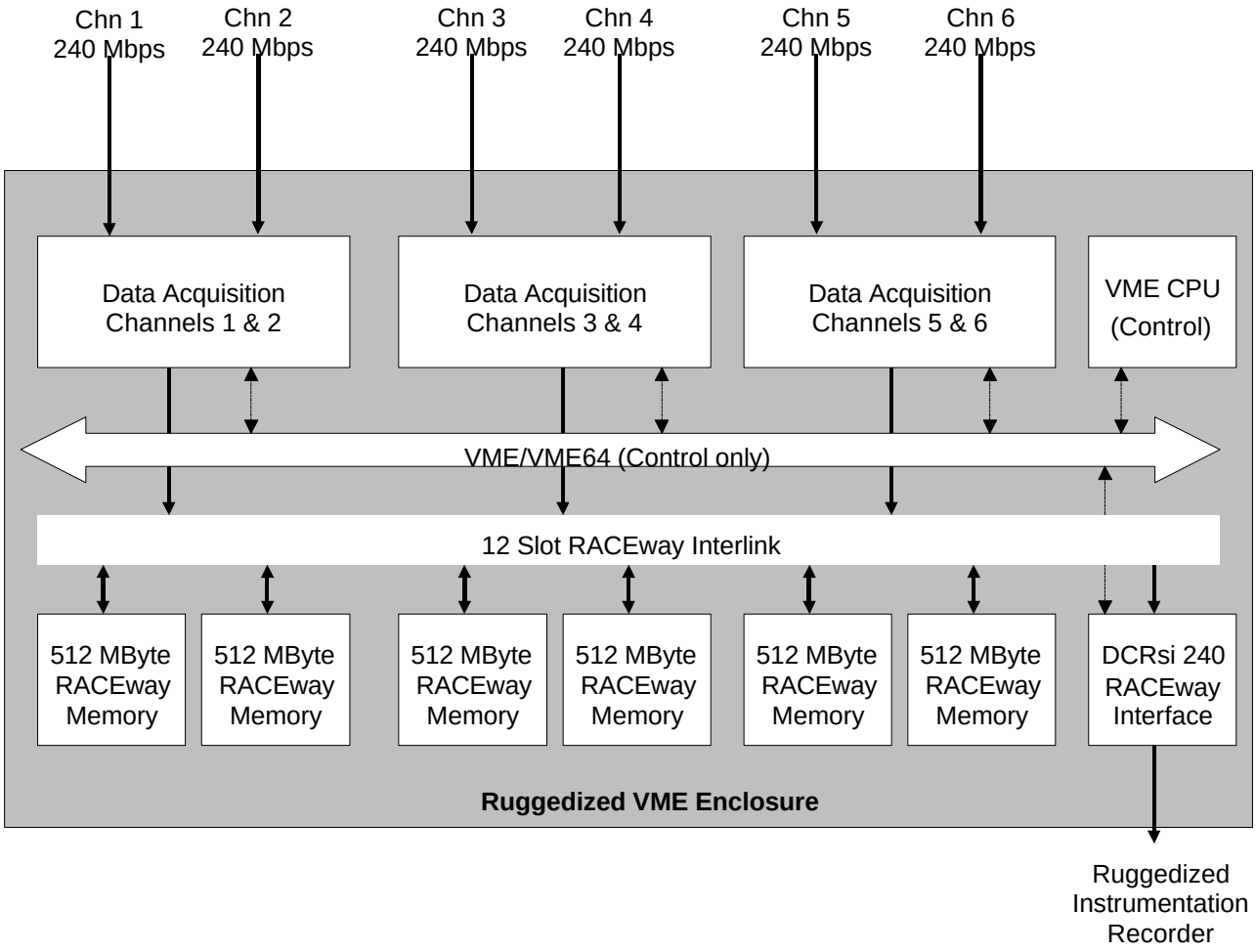
DATA ACQUISITION AND CAPTURE - 200 MBPS TO 1 GBPS

The scalability of RACEway makes it an ideal architecture for handling multiple high-rate data streams. Two examples of such systems are a high-speed data acquisition system, and a Common Data Link front-end system.

High-speed Data Acquisition System

The High-speed data acquisition system (Figure 3) is an airborne configuration that acquires data from six concurrent 30 Mbyte/second data streams, storing the data in COTS VME/RACEway memory boards. Selected portions of the data are read from the memories and recorded on a ruggedized instrumentation recorder. The system uses six 512 Mbyte memory boards (using six slots), for a total of 3 Gbytes of solid-state buffering. By using available 2 Gbyte memory boards, the total buffering can be easily expanded to 12 Gbytes. Furthermore, up to 8 more memory boards can be included in the system, taking the total buffering capacity to 28 Gbytes. The system makes use of existing ruggedized enclosures to provide the shock, vibration, and EMI/EMC protection required for airborne applications.

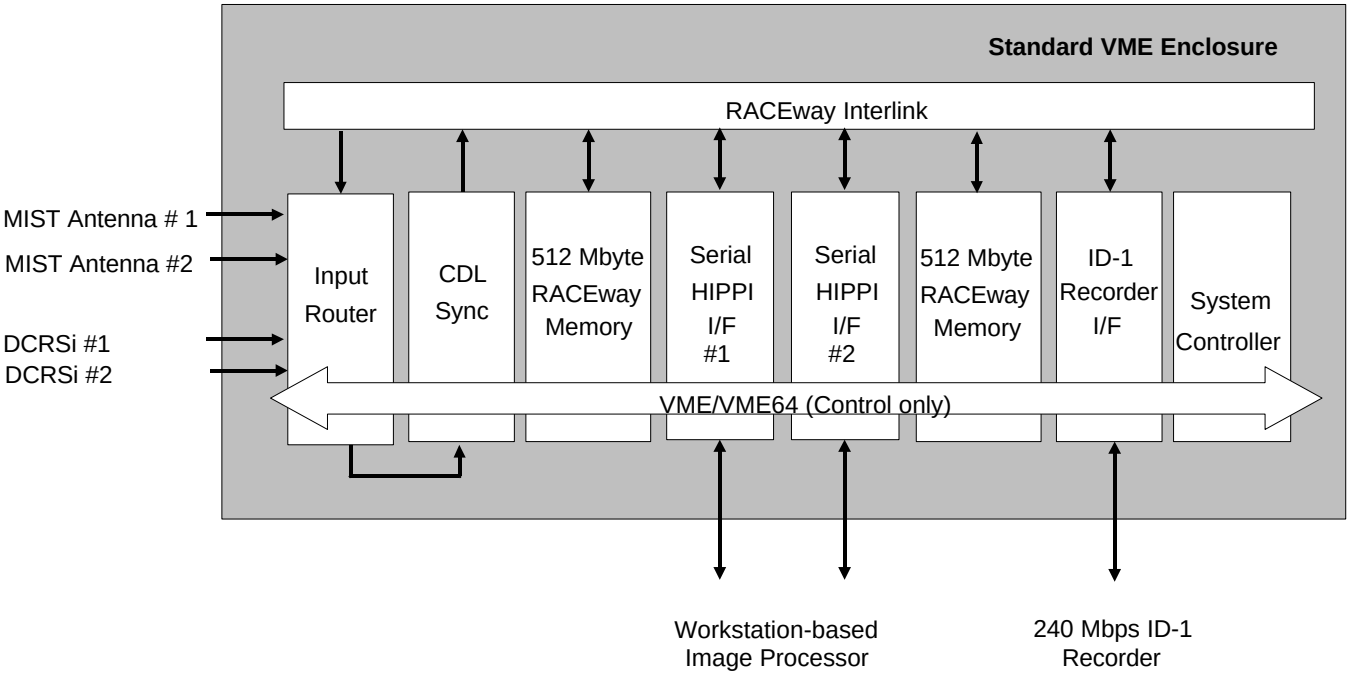
Figure 3 - RACEway System that Acquires Data at 180 Mbytes/second



Common Data Link Front End System

The Common Data Link (CDL) front end processor (figure 4) is a flexible system capable of handling two data 274 Mbps streams of data from MIST antennas. The first data stream is received, synchronized and stored in a VME/RACEway memory board. From the memory board the data is output to an image processing workstation (via Serial HIPPI). The second stream is received, stored in memory, and output to an ID-1 recorder and/or another workstation (via a second Serial HIPPI channel). The system controller (a standard VME single board computer) is responsible for controlling both operations simultaneously. The system controller is also responsible for examining header and support data in the dual access memories and making real-time decisions regarding what processing is appropriate for the input data.

Figure 4 - RACEway-Front End Handles Two 274 Mbps CDL Data Streams



CONCLUSIONS

RACEway architectures are well suited to high-performance, real-time data acquisition systems offering:

1. High throughput. Since internal bandwidth is scalable, it increases with the number of functional elements in the system. This is a large advantage over bus systems in which internal bandwidth decreases with the number of functional elements.

2. Deterministic Performance. The system designer can allocate separate data paths for critical real-time functions, ensuring data overruns will not occur.

3. Availability of Products. A wide range of off-the-shelf, high-performance products are available greatly reducing the amount of custom hardware typically required in high-performance real-time systems.

4. Compatibility with VME. Standard VME products -- including ruggedized enclosures, standard single-board computers, and auxiliary function equipment -- integrate easily with RACEway.