# IRIG-106: A Design Exercise for Digital Communications

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## ABSTRACT

This paper describes a design project which combines the simulation capabilities of the Communications Tool Box in SIMULINK® with the IRIG-106 standard. The design project is part of a senior level digital communications course offered in the Department of Electrical & Computer Engineering at Brigham Young University and functions as an introduction to the Telemetering Program at BYU which is funded by the International Foundation for Telemetering.

## INTRODUCTION

The senior level digital communications course offered in the Department of Electrical & Computer Engineering at Brigham Young University covers some practical aspects of digital communications systems including modulation, pulse shaping, matched filters, symbol decisions, carrier phase recovery, symbol timing recovery, and frame synchronization. An important part of the course is a series of design exercises which require students to construct a receiving system, test and debug the subsystems, and analyze the performance of their design using the Communications Tool Box in SIMULINK.® The PCM/FM standard outlined in the Inter-Range Instrumentation Group (IRIG) 106 standard provides an ideal platform for introducing some of these key communications systems concepts of to senior electrical engineering students.

This paper describes a design exercise and illustrates the utility of the IRIG-106 standard.

## DESIGN EXERCISE

The design exercise requires students to construct (in SIMULINK®) a demodulator to recover data which has been formatted using IRIG-106 and modulated using PCM/FM. The system requirements for the simulation exercise are summarized in Table 1. The modulated signal is supplied to the students and is stored in the file irig.mat. This exercise requires the students to design a demodulator, bit synchronizer, de-scrambler, and framing module to recover the data. The details of the design methodology are described in the following sections.

Table 1: Design Requirements

| | |
|---|---|
| Sample rate | 100 samples/sec |
| Bit rate | 1 bit/sec |
| Carrier frequency | 25 Hz (this is the “apparent carrier” frequency) |
| Modulation | PCM/FM (binary FSK) |
| Frequency shift | 1 Hz |
| Pulse shape | low pass filtered NRZ-L |
| Number of sources | 2 |
| Multiplexing format | TDM |
| Framing | IRIG-106 |
| Input file | irig.mat |
| Input file length | 49056 sec. |

## Source

The data consists of two secret messages, represented in ASCII form, multiplexed together using three subframes per minor frame as illustrated in Figure 1. As illustrated, each minor frame consists of a synchronization field, a frame counter field, and two data fields which contain the ASCII code of a character in the source message.

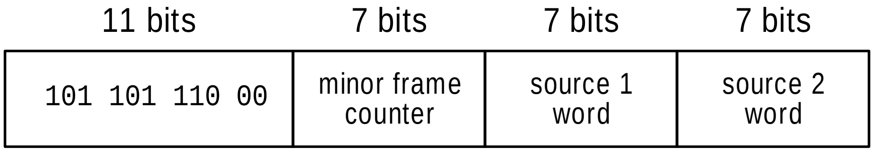

Figure 1: Minor Frame Structure

The source is assembled in software, randomized, and stored in the MATLAB® workspace. These data are then modulated using the SIMULINK® block diagram illustrated in Figure 2. The **Sampled Read from wksp** block outputs each bit of the composite source (which has a value either zero or one). The **Look-Up Table** block simply maps zero to -1 and one to +1 to create a bipolar signal suitable for frequency modulation using the voltage controlled oscillator (VCO) of the **Discrete-time VCO** block. The premodulation filter is a length 100 FIR low-pass filter with a cut-off frequency of 0.7 Hz which is represented by the **Classical FIR LP Filter** block. The effect of this filter on the power spectrum of the modulator output is easily observed using the powerful plotting capabilities of MATLAB®. The output of the modulator is stored in the file irig.mat using the **To File** block. The contents of this file serve as the source for the demodulator design.

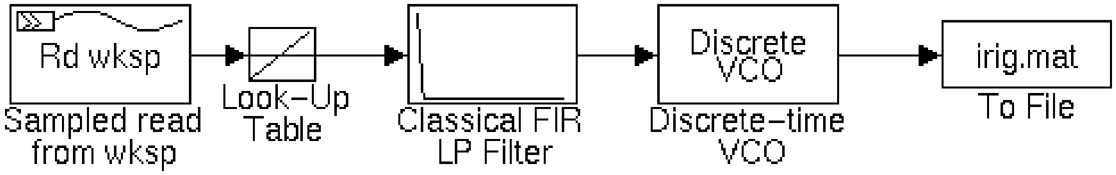

Figure 2: PCM/FM Modulation System

## Demodulator

The entire demodulator is illustrated in Figure 3 and consists of four major components: the source, the FM Demodulator, the Bit Synchronizer, and the Data Destination subsystems. The source for the demodulator is the file `irig.mat` which is input to the system using the **From File** block.

The FM demodulator is implemented using the delay-line technique which approximates the derivative of the phase of the input signal. The K-step delay is chosen to so that $\omega_0 K = \pi/2$. The low pass filter is a 3rd order Butterworth filter with cut-off frequency 10 Hz.

## Symbol Timing Recovery (Bit Synchronizer)

The bit synchronizer is composed of four main parts, the integrator, the symbol timing recovery subsystem, the sample-and-hold system, and the bit decision. The integrator is realized using the **Discrete Integrator w/edge triggered reset** block which sums the input samples until reset by a rising edge on the clock input. The integrator output is sampled (using the **edge triggered zero order hold** block) and a decision is made on the bit value using the **Fcn** block which tests the input to determine if it is greater than zero.

The **Discrete Integrator w/edge triggered** and **edge triggered zero order hold** blocks are edge-triggered devices which perform their functions when the rising edge of the clock input is detected. This clock is generated from the integrator output by the **Timing Recovery Subsystem** block which is expanded in Figure 4. This system is designed following the standard procedure of processing the matched filter output with a non-linearity to produce a harmonic at the bit frequency which is then isolated by a filter to produce a clock at the bit rate which is in phase with the bit transitions [2]. The non-linearity is produced by multiplying the integrator output by a delayed version of itself. The delay which produces the strongest Fourier component at the bit time is half the bit time

[3]. The product is filtered using a phase lock loop which uses the **Product 3** block and **Butterworth IIR LP Filter** block as a phase detector and **the Discrete-time Quadrature VCO** block as the oscillator (this block outputs two sinusoids in quadrature). The VCO output (a sinusoid) is then hard-limited by the **Sign** block to produce a square wave, with well defined edges, which functions as the clock for the **Discrete Integrator w/edge triggered reset** and **edge triggered zero order hold** blocks.

### Data Destination

The data are written to the MATLAB® workspace where the de-randomizer is implemented using a software function written in a MATLAB® script. Word synchronization and extraction is performed using a MATLAB® script also. Students are then able to reconstruct the messages and submit the result via email.

## CONCLUSION

The design project described in this paper serves two purposes:

1. Introduction to the principles of digital modulation, pulse shaping, symbol timing recovery, and frame synchronization. This is an extremely useful tool which provides students concrete examples which reinforce the theoretical aspects of these principles. In this way, the IRIG standard supports the educational goals of the senior level course.
2. Introduction to the IRIG-106 standard and the field of telemetering. This is an important component in support of the Telemetering Program at BYU which is funded by grants from the International Foundation for Telemetering.

The PCM/FM standard is well suited to reinforcing basic principles of digital communication systems design. The IRIG-106 is easy to implement and understand – thus students are not distracted from the principles by details which are not directly relevant to those principles. In addition, this project is representative of an actual system (rather than a contrived example for the class). The SIMULINK® design and simulation environment is also easy to use. It provides students with an easy to use method for demonstrating the functionality of the basic components in a communications system which reinforce the principles discussed in the classroom.

## REFERENCES

[1] Telemetry Group – Range Commanders Council, *IRIG Standard 106-93: Telemetry Standards*, White Sands Missile Range, New Mexico, 1993.

[2] R. Ziemer and W. Tranter, *Principles of Communications: Systems, Modultion, and Noise*, Houghton Mifflin, Boston, Fourth Edition, 1995.

[3] B. Sklar, Digital Communications: Fundamentals and Applications, Prentice-Hall, Englewood Cliffs, 1988.

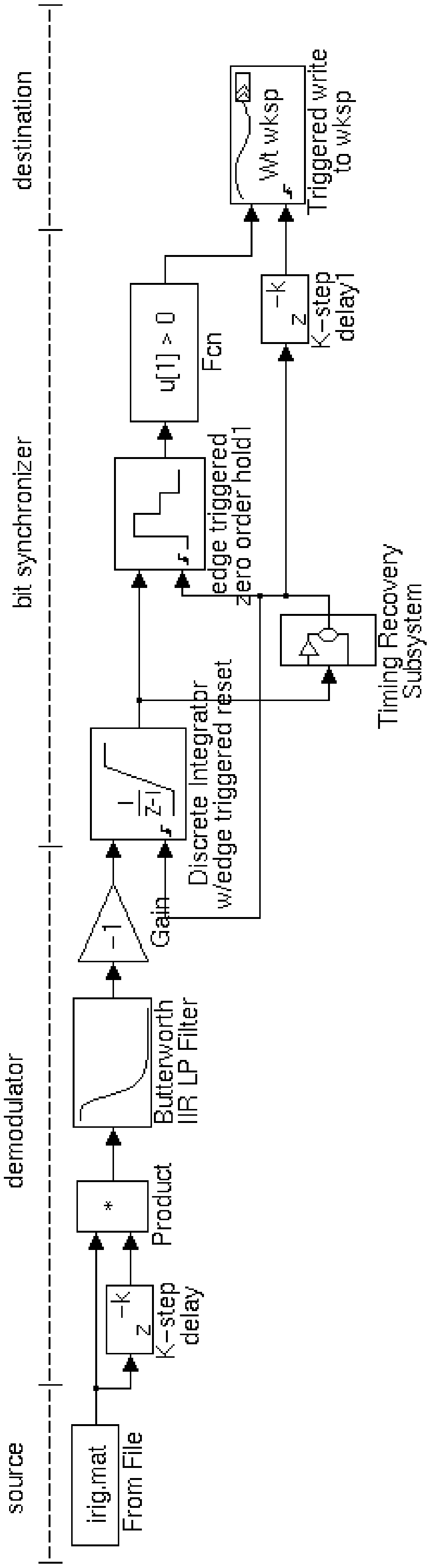

Figure 3: PCM/FM Demodulator

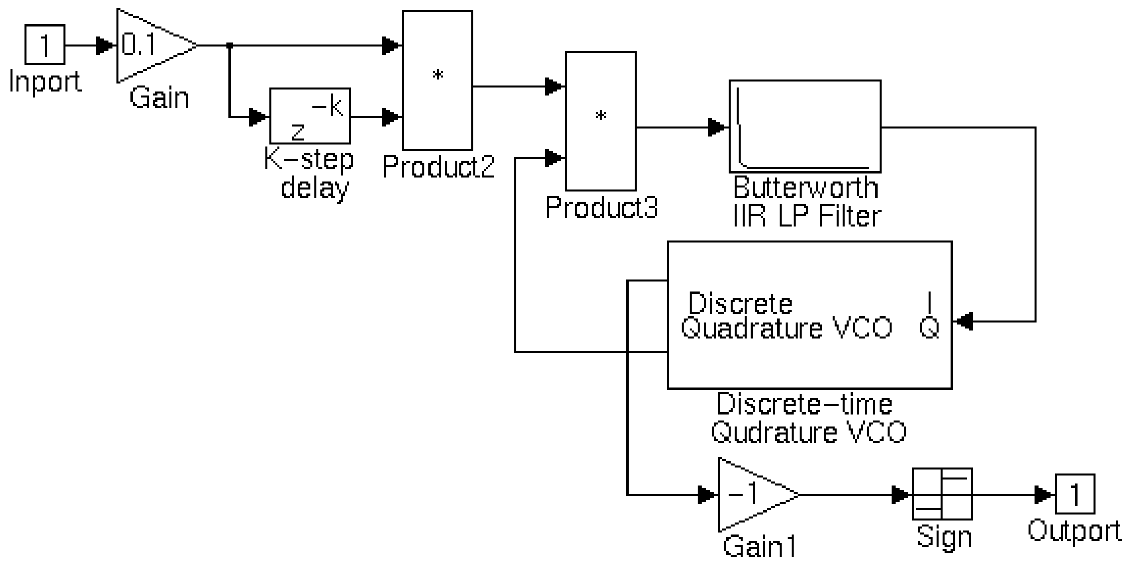

Figure 4: Symbol Timing Recovery Subsystem