ULTRA HIGH BIT RATE (UP TO 1GBIT/S) BANDWIDTH EFFICIENT FQPSK ALL-DIGITAL MODULATOR/DEMODULATOR ARCHITECTURES AND NASA IMPLEMENTATIONS

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ABSTRACT

The paper presents ongoing efforts at NASA's Goddard Space Flight Center and the Jet Propulsion Laboratory to develop ultra high bit rate bandwidth efficient FQPSK modulators and demodulators.

The ability to transmit and receive ever-increasing amounts of extremely high rate data is an enduring challenge in the arena of near-earth space borne science missions. Reliable and efficient transmission of information at these data rates requires the use of power and bandwidth efficient modulations that exhibit low transmitter, receiver, and decoder complexity. Conventional high rate approaches for achieving spectral limiting typically employ sharp post amplifier filtering at the transmitter to limit the interference to the adjacent bands. However, using analog filtering alone can produce substantial intersymbol interference and other distortions that substantially affect the detection performance of the signal. In contrast, various theoretical classes of modulation waveforms can be tailored to provide varying degrees of bandwidth and power efficiency or robustness to non-linear transmitter distortions while incurring little or no performance losses. In order to realize many of these signal types, precise amplitude and phase control over the synthesis of these signals is required, typically necessitating the use of digital signal processing.

INTRODUCTION: THE FQPSK WAVEFORM STRUCTURE

Feher-patented QPSK, or FQPSK, is a spectrally efficient form of offset QPSK modulation patented by Kamilo Feher in 1986 [1]. In 1998, a trellis-coded interpretation of FQPSK was discovered by Simon and Yan [2] that allowed for a simpler transmitter structure and a receiver with improved bit error performance when utilizing an optimal detector. Using this interpretation for both in-phase and quadrature channels, one of sixteen spectrally shaped waveforms (the eight unique waveforms shown in Figure 1 and their inverses) is transmitted based on a trellis-coded combination of present and previous

data bits. The generation of this waveform may also be viewed as a finite memory bit sequence mapping to select the transmitted, full response pulse shape from the eight possibilities shown in Figure 1 with the most recent bit determining the polarity of the signal.

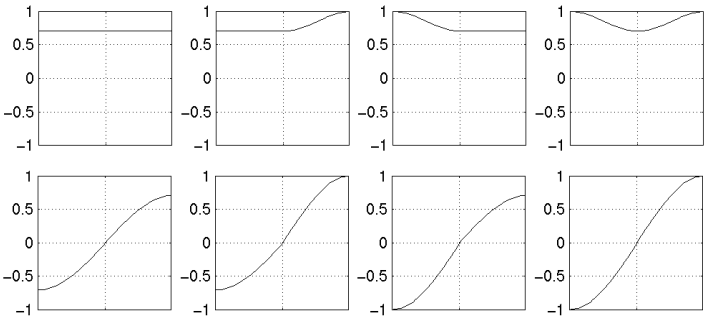


Figure 1. FQPSK waveforms

The FQPSK waveforms are designed to minimize spectral sidelobes and envelope fluctuation. Cross-correlation is introduced between the transmitted in-phase and quadrature waveforms to produce a quasi-constant envelope with less than 0.2 dB envelope fluctuation. Due to its quasi-constant envelope property, FQPSK can pass through a nonlinear power amplifier in full saturation with minimal spectral regrowth. Overall, the spectrum of FQPSK is substantially bandlimited with a 99% power containment bandwidth more than six times smaller than QPSK. Figure 2 shows a computer-generated plot of the FQPSK spectrum with the frequency axis normalized to the information data rate (twice the transmit symbol rate).

A baseband-filtered version of FQPSK, known as FQPSK-B, has an even narrower spectrum with sidelobe suppression of –70 dB at approximately 1.5 times the data rate away from the center frequency. FQPSK-B has been recommended by CCSDS and IRIG standards for use in systems that require high data rate, bandwidth efficient communications.

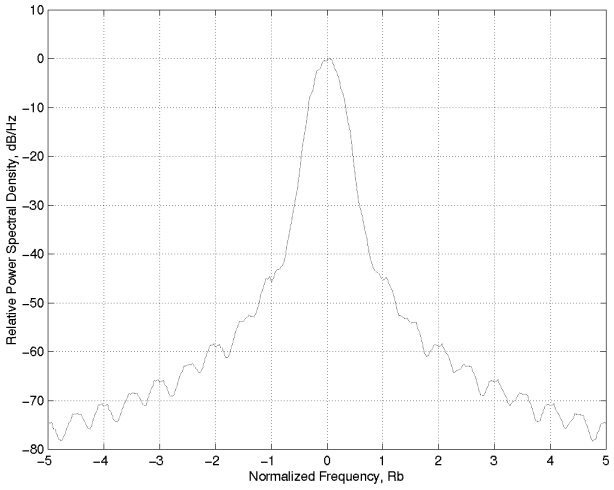


Figure 2. FQPSK Spectrum

NASA/GSFC FQPSK MODULATOR

NASA's Goddard Space Flight Center has developed a prototype digital FQPSK modulator capable of 300 Mbps. The design is based on an architecture described in [1] and [2] and is currently operating in the lab at full rate. A block diagram of the modulator and test configuration is illustrated in Figure 3. The design is implemented on a board consisting primarily of discrete components, although an integrated circuit (VLSI) implementation is possible with even higher performance possible. The following is a summary of the key modulator parameters:

- Data rate of up to 300 Mbps with FQPSK modulation
- 4 Samples per symbol

The prototype demonstrates the feasibility of implementing the architecture in [2] at high rates and proves numerous design methodologies. The design is to be tested with other NASA space telecommunications equipment, including the TDRS system. The knowledge gained through this design effort and results of these tests will be used extensively in future efforts to develop higher data rate modulators (exceeding one Gbps), which are currently ongoing at JPL and NASA. Figure 4 illustrates the eye diagram and spectrum of the modulator generating 300 Mbps FQPSK. Note the modulator meets the Space Frequency Coordination Group (SFCG) recommended spectral mask for high rate mission planned after 2001.

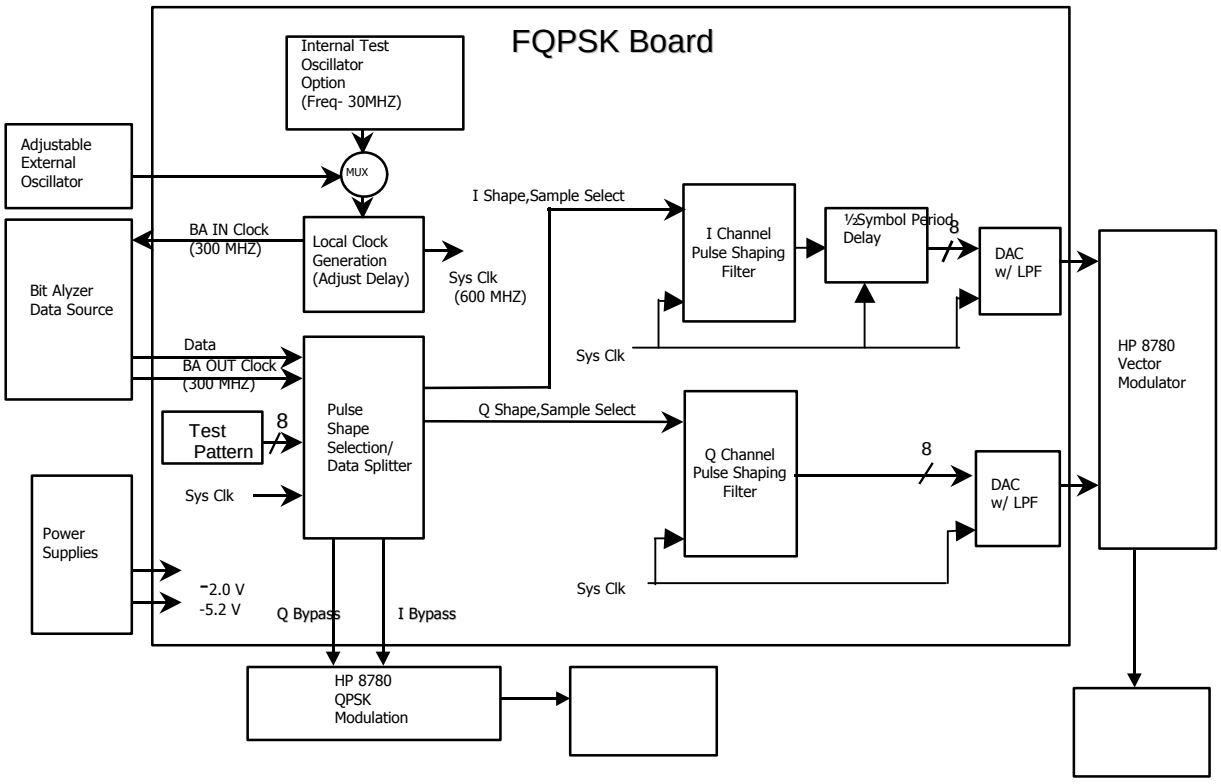
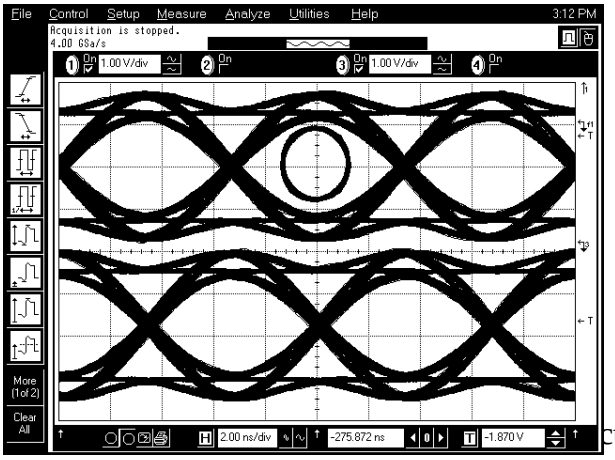
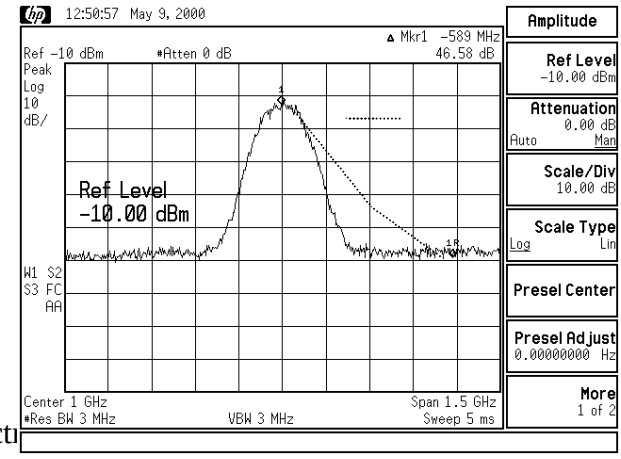


Figure 3. NASA/GSFC FQPSK Modulator





JPL/NASA BANDWIDTH EFFICIENT MODULATOR

Here we present an effort at JPL to develop a very high rate bandwidth efficient modulator, including FQPSK, based on parallel processing elements. The design approach described here replaces expensive, high power consumption analog or digital GaAs signal processing technology for very high rate applications with low power, high density and relatively inexpensive CMOS technology based on parallel processing methods. This effort is structured to result in hardware algorithms, designs and prototypes to generate different bandwidth efficient modulations for Gbps applications. The combination of parallel architectures and novel waveform generation is intended to provide a full measure of flexibility in performance and bandwidth efficiency in a cost-effective fashion.

The first target waveform considered is FQPSK. Here we discuss the design approach and its implementation and expansion to high rates in field programmable gate array (FPGA) logic as well as results of preliminary laboratory testing.

DIGITAL MODULATOR CIRCUIT ARCHITECTURE AND DESIGN

Due to their reconfigurability, constantly increasing capacities and availability of radiation tolerant components [3, 4], commercial FPGAs represent an ideal technology in which to validate the concept of low cost, parallel, high rate communications signal processing for potential space-based applications. In this section, we discuss the FPGA circuit architecture used to synthesize the FQPSK complex baseband waveform as synchronous digital samples. The initial effort produced a design for a single processing element whose core could be re-used in a parallel, time-multiplexed fashion to achieve high rate throughput. A high level view of the functional signal flow for the FPGA is shown in Figure 5. Serial input data is initially de-multiplexed into alternating data streams from which pulse shape lookup addresses are computed as depicted in Figure 6, according to the rules given in [2]. The state address and the value of the most recent information bit then provide the selection of the complex FQPSK pulse shape during that symbol interval. The state and bit information are then routed to identical lookup tables that store eight ten-bit samples for each pulse shape. These samples are synchronously read out over a symbol interval with a half symbol delay implemented between inphase and quadrature sample streams.

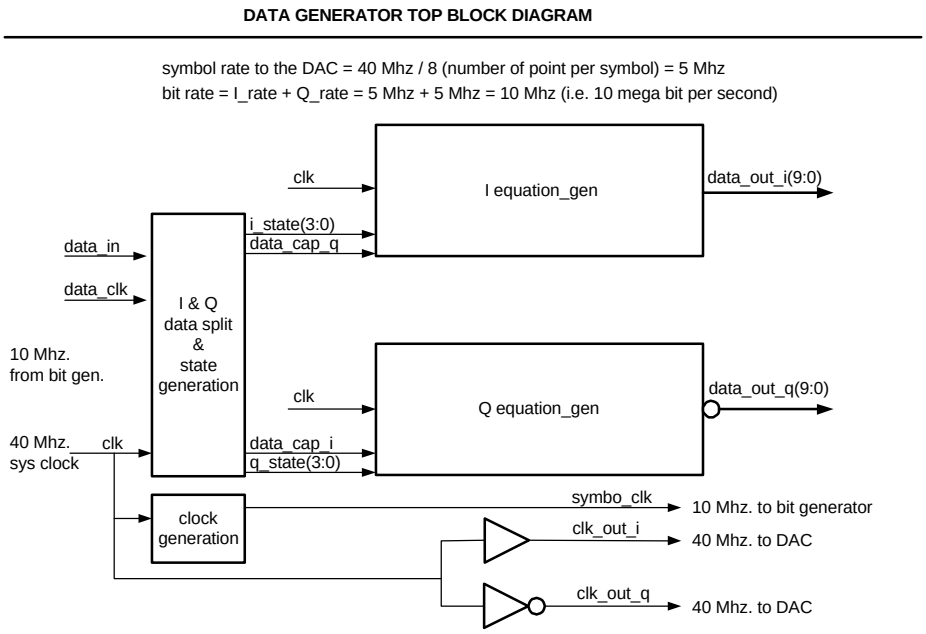


Figure 5. Single Processing Element Configuration

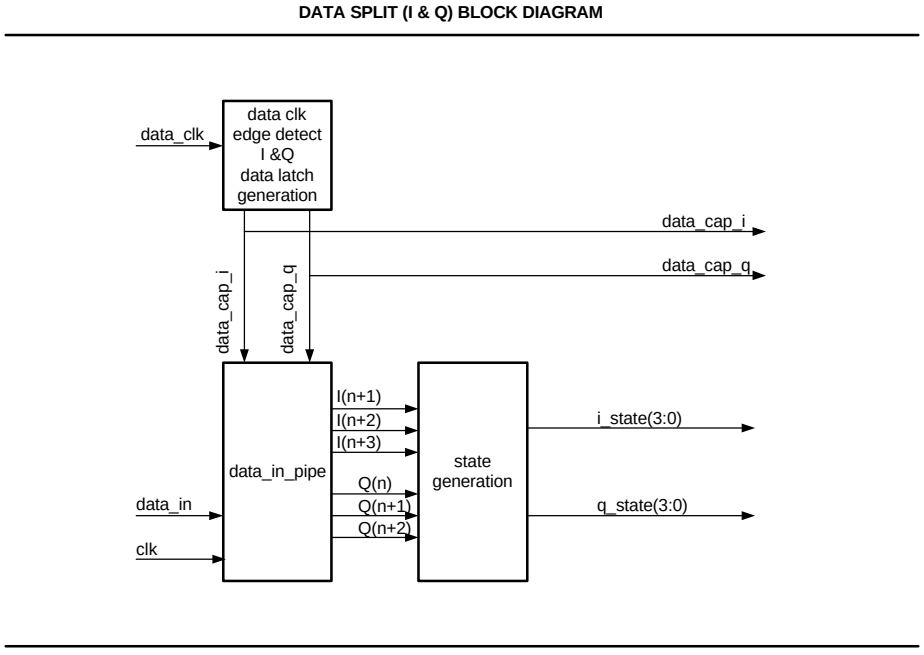


Figure 6. Serial Data Input and State Generation for Waveform Selection

In terms of implementation details, the modulator's digital design was realized in an Altera Flex 10K family FPGA (EPF10K100ARC240-3). This part is representative of a modest capacity device (approximately 100,000 equivalent gates, 189 user I/Os). A preliminary design for the Trellis-Offset QPSK (T-OQPSK) waveform was written and simulated in VHDL and tested with the digital-to-analog converter (DAC) evaluation board to verify basic system operation. As more sophisticated tools were made available, the subsequent design of FQPSK was done in Verilog for compatibility with related

projects and verified using a ModelTech simulation tool. Test inputs consisted of known input bit patterns and digital waveform outputs were compared to a discrete time MATLAB simulation. These inputs and outputs, in turn, respectively formed the test stimulus and response for verifying modulator operation when fully integrated into the test configuration described in the following section.

The migration of the single processing element design to multiple parallel processors is depicted in Figure 7 for a dual element configuration. Many aspects of the pulse shape lookup table and state generation

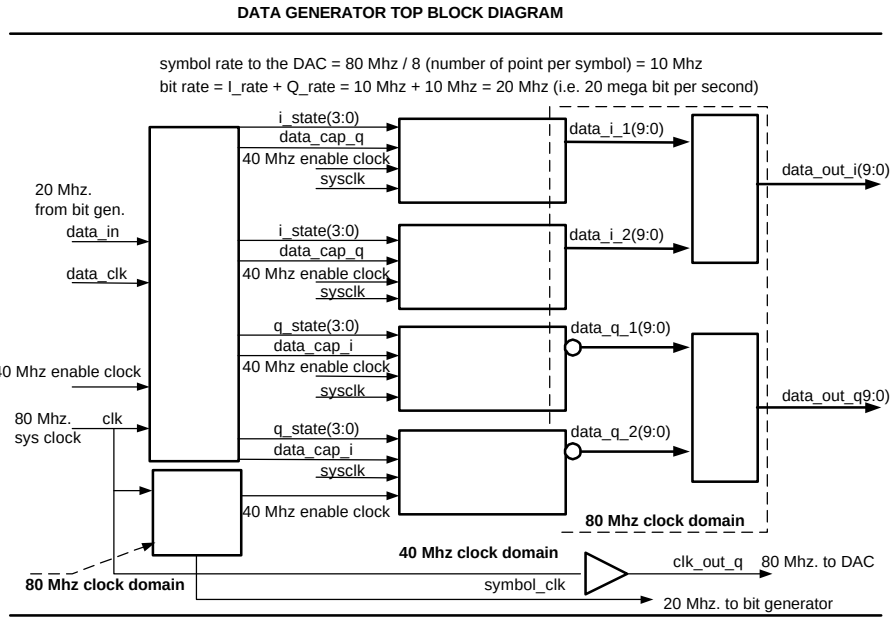


Figure 7. Dual Processing Element Configuration

remain identical to those present in the initial design. A high rate (80 MHz) 8x10 bit block register is added to the table lookup equation generator and a sample multiplexer is added to the modulator in order to select between the correct symbol output. This approach is sufficient to add low numbers of additional channels within the confines of the FPGA. However, it can quickly become limited when the high-speed portions of the design outstrip the maximum clock frequencies supported by a particular FPGA technology (typically in the 80 – 150 MHz range). At that point, the incorporation of additional parallel channels can be accommodated by expanding the width of the output words so that many parallel samples are simultaneously output from the FPGA at a lower frequency while retaining a high throughput sample rate.

Such configurations then rely on external high speed multiplexing circuitry that is typically rendered in GaAs for the serial sample stream generation. Preliminary analyses have indicated that the number of parallel elements supportable by the Altera FPGA is not circuit area limited but rather I/O pin limited. Depending upon the number of bits in the output samples to the DAC, between seven and nine parallel elements can be accommodated within this part. For substantially larger parts, up to 30 parallel processors can be implemented.

LABARORATORY CONFIGURATION AND MODULATOR PERFORMANCE

The initial prototyping effort focused on validating the complex baseband waveform generation of the FQPSK signal. In order to rapidly demonstrate this capability while retaining sufficient flexibility to implement simple parallel processing structures, stand-alone evaluation boards for the FPGA and the dual DACs were integrated into a single chassis and interconnected with test equipment in the configuration shown in Figure 7. A complex upconverter suitable for modulation at UHF carrier frequencies was also used to evaluate the spectral occupancy of the FQPSK signal. An external synthesizer provides a local oscillator input to the upconverter at a frequency of 437.1 MHz. User programmable serial data input into the FPGA was provided by a BitAlyzer 25 bit error rate tester (BERT). The FPGA was programmed to provide the input data clock to the BERT for purposes of maintaining coherent throughput from input data to output waveform samples. The data generator was used both in known data pattern and random PN sequence generation modes to verify the complex baseband output waveforms.

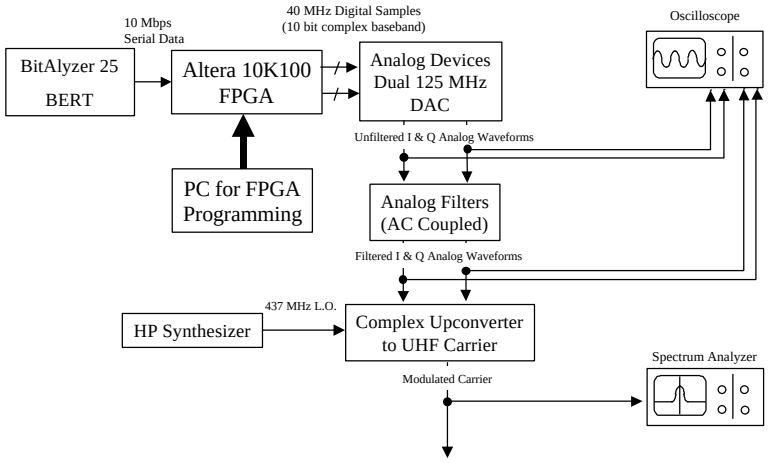


Figure 8. Laboratory test configuration

The modulated signal spectra shown in Figure 9 respectively correspond to the upconverted FQPSK waveform with and without analog filtering following the baseband DAC outputs. The unmodulated carrier due to the DAC DC offsets is clearly evident in the first spectral plot. With AC coupling and nominal lowpass filtering, the carrier component is removed in the second spectrum analyzer display. In both figures, the spectral containment of the signal agrees very well with the computer-simulated plot of Figure 2 up through the first nulls (-45 dB down from the signal peak), which occur at +/- 10 MHz from the carrier frequency. The remainder of the out of band spectral roll-off is not as pronounced as that observed in the simulated performance and is likely the result of reaching the dynamic range of the 10-bit digital-to-analog converters to accurately reproduce an un-quantized waveform. For very high rate systems requiring substantial attenuation at frequency separations greater than one or two sidelobes beyond the main lobe, this is most likely achieved with the aid of relaxed analog filtering.

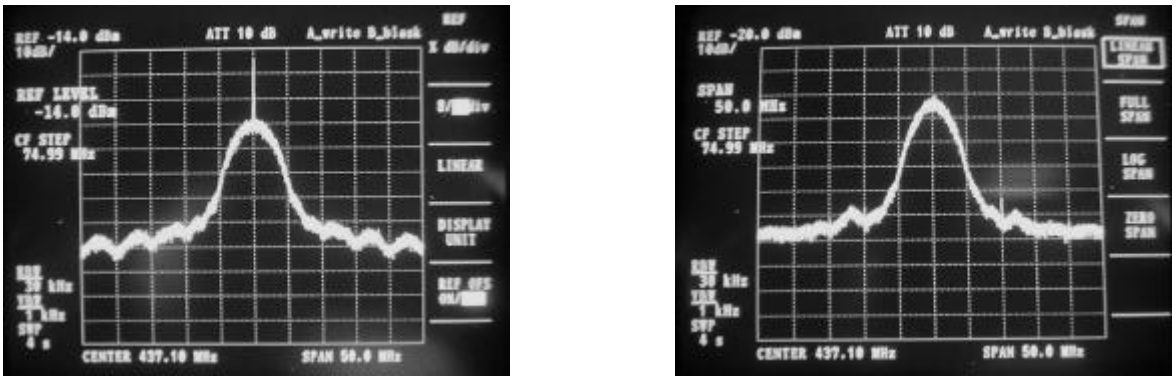


Figure 9. Spectra of 10 Mbps FQPSK UHF Carrier, with and without baseband lowpass filtering

A prototyping effort to implement a 10 Mbps FQPSK modulator using basic commercial FPGA technology was completed in a time period of approximately two months. The designs resulting from this effort help form the algorithmic foundation for the design and implementation of a parallel circuit, low cost, very high rate, space-based modulator capable of generating a variety of power and bandwidth efficient communications waveforms with data rates above one Gbps.

NASA/GSFC JPL VERY HIGH RATE ALL-DIGITAL PARALLEL RECEIVER

A very high rate all-digital receiver for satellite communications capable of demodulating a wide range of data rates and data formats has been developed by NASA's Goddard Space Flight Center and JPL [6,7]. The core of this receiver is a demodulator application specific integrated circuit (ASIC) which performs all the operations of a traditional receiver: downconverting to baseband, carrier recovery, detection filtering, symbol-timing recovery, and limited equalization. All filter coefficients and a host of other parameters are programmable. The all-digital receiver is capable of demodulating a host of bandwidth efficient modulations including FQPSK. The receiver is currently being tested in the lab at GSFC and is capable of data rates up to 600 Mbps.

The receiver will be tested together with the 300 Mbps FQPSK modulator in Q4 2000. Figure 10 illustrates the performance of the fixed-point software model of the receiver with FQPSK modulation. To date, QPSK demodulation test results with the receiver in the lab have yielded results on the order of 0.1 to 0.2 dB worse than the fixed-point software model of the receiver used for simulated demodulation. Similar results are expected for FQPSK modulation.

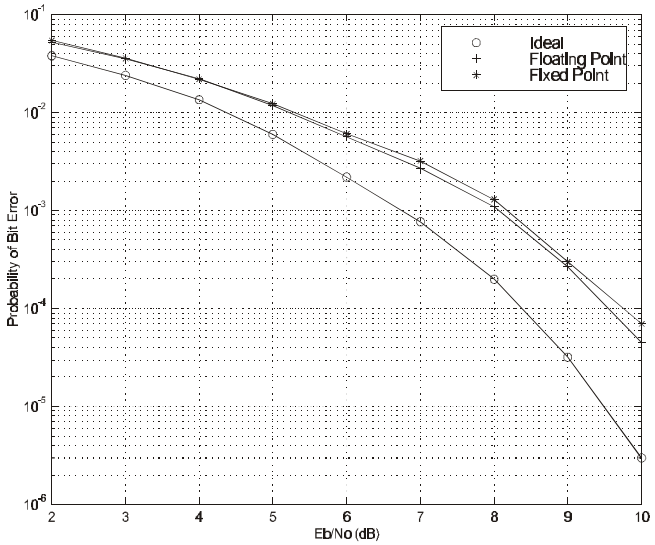


Figure 10. Demodulation Performance of the High Rate Parallel Receiver with FQPSK

The next generation parallel digital receiver is currently being developed by NASA/GSFC and JPL. Data rates in excess of 1.2 Gbps QPSK and 2.4 Gbps 16-QAM will be possible with the next generation. The demodulator will be implemented in a single CMOS ASIC solution with a core architecture identical to that currently implemented and described in [6,7]. Higher chip clock rates, improved parallel signal processing algorithms, and parallel equalization will also be incorporated in the next generation parallel digital receiver.

CONCLUSION

This paper presented an overview of ongoing efforts at NASA/GSFC and JPL to implement FQPSK modulators and demodulators at ultra high data rates. Currently hardware exists and is operating in the lab at GSFC that modulate FQPSK at rates up to 300 Mbps and demodulate at rates up to 600 Mbps. The next generation of these systems that are currently being developed at JPL and NASA/GSFC will modulate and demodulate at data rates well in excess of one Gbps.

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