A VERSATILE PROGRAMMABLE FUNCTION RF ASIC FOR SPACE-BASED RF SYSTEMS

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ABSTRACT

A programmable RF ASIC is described which provides most of the RF functions within a next generation S-band transponder for space applications. The unique 18-contact LCC device can be programmed to perform a variety of RF and analog functions. This single space qualified high speed bipolar "function toolbox" is used in 39 locations throughout the transponder to provide a flexible radio architecture. The ASIC design process, internal electrical design, circuit application, space environment performance, and RF testing of the RF ASIC are described. This proprietary part provides a space-qualified solution for RF circuitry that can be applied to a variety of space application products.

KEY WORDS

RF ASIC, transponder, QuickChip, radiation hardened.

TOOLBOX ASIC APPROACH FOR SPACE ENVIRONMENT

In 1996, L-3 Conic selected a novel custom RF ASIC “function toolbox” approach to meet the rigorous demands of a new space-environment S-band transponder. To minimize component qualification and screening cost, one single chip design provides 13 RF and analog circuit functions available as either bonding options or as pin-programmable functions. The single chip design, dubbed “Chameleon”, is used in 39 positions within the new transponder. In each position, the Chameleon takes on the function enabled by its circuit board connection.

While the “function toolbox” approach may seem inefficient from the standpoint of chip count and silicon usage, it is highly effective in space applications where a larger number of a single part type can be qualified and screened to replace a myriad of miscellaneous discrete component types used in lower quantity. In addition, making changes to the lineup within the block diagram is simply a matter of rearranging the RF chips on the board. A commitment to a highly integrated ASIC with a dedicated internal block

diagram is avoided and total on-chip gain is held to less than 26 dB, easing S-band stability and crosstalk risks. The general purpose building block, being uncommitted to a particular block diagram, will be useful on other future space products.

The packaged part meets the many unique requirements of space applications, including screening to MIL-STD-883 Class S, low outgassing, hermeticity, 1 Mrad radiation tolerance, excellent tolerance to single event upset, and absence of single event latchup. The small ceramic surface mount package provides a low cost alternative to hybrid construction while retaining small size, low cost, and the ability to withstand the mechanical rigors of long term thermal cycling. Part obsolescence, always a concern in space hardware, is now under direct internal control. The custom RF ASIC was developed with first-pass success after a 5 month development program. Transponders using this unique part are now in production.

For this S-band space application, analog signal processing (ASP) using this custom ASIC was chosen over digital signal processing (DSP) because of its lower power, smaller size, and lower cost. The cost of an S-level Chameleon is less than 4 % of the cost of a similar radiation level FPGA.

APPLYING CHAMELEON TO THE S-BAND SPACE TRANSPONDER

The block diagram for the new transponder followed the previous heritage design, with modifications to make maximum use of the custom RF ASIC capability, including the replacement of previous multiplier-based local oscillator (LO) generation with a phase lock loop approach. Figure 1 shows the block diagram of the upgraded transponder.

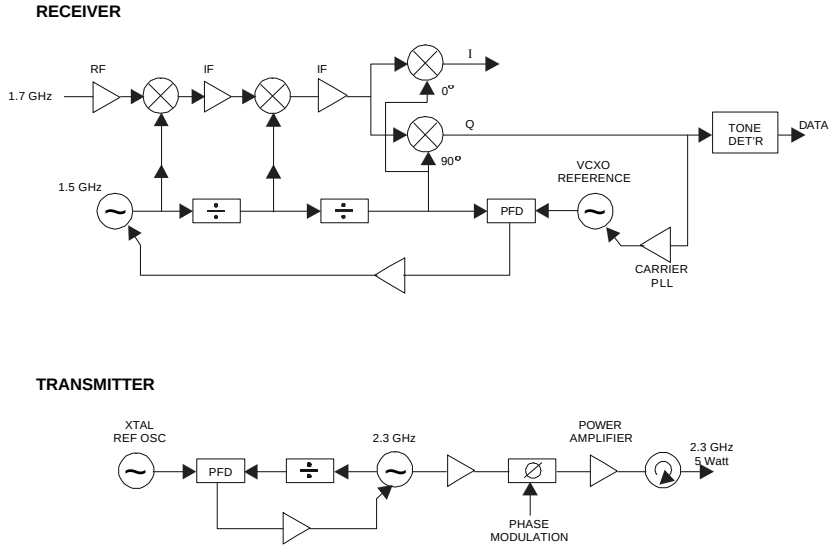

Figure 1. Next Generation Space Transponder Block Diagram

The 13 functions designed onto the Chameleon chip are separated into two independent blocks of circuits, each with 18 on-chip bonding pads. These are available in an 18 contact LCC package as two separate bonding options, creating two part types from the single chip design. In the case of the Dash 1 bonding option, the seven RF functions are selected via six programming lines. When installed on circuit boards, Chameleon takes on the function dictated by the voltages and currents provided on the programming lines. The Dash 2 tone detector has all its functions accessible on external contacts. During operation, the transistors in the unused functions are powered down.

The Dash 1 bonding option of Chameleon is shown in Figure 2. This configuration includes the variable gain amplifier (VGA), mixer, phase/frequency detector (PFD), divide by 2, 3, 4, and 5 prescalers, and the 6-input function selector circuit.

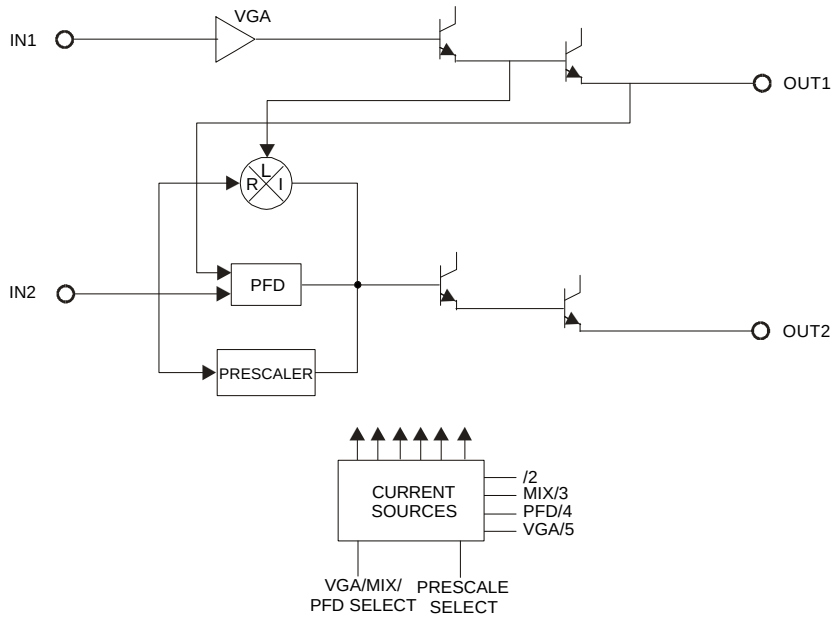

Figure 2. Dash 1 Selectable RF Functions Block Diagram

The Dash 2 bonding option uses the other half of the Chameleon die and is shown in Figure 3. All its functions are available directly on the 18 package contacts without programmable selection. In practice, the tone detector function depends on external op-amps to drive the RMS summer. The linear phase detector is used for demodulation of the phase modulated transponder ranging signal.

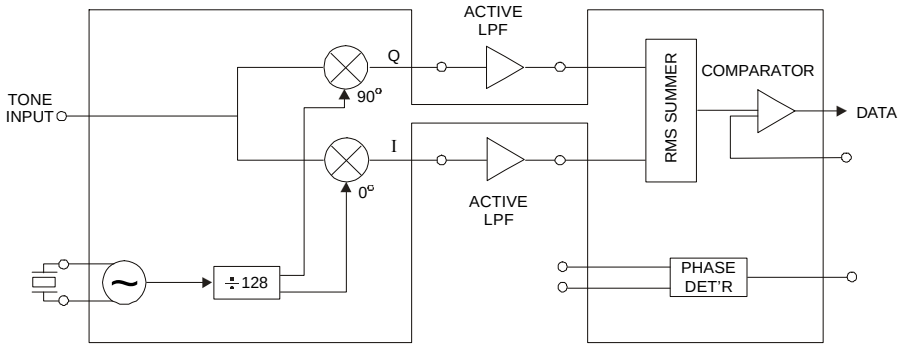

Figure 3. Dash 2 Tone Detector Block Diagram

SILICON BIPOLAR CIRCUIT DESIGN

Design of Chameleon used conventional silicon bipolar circuit design techniques. The SPICE-like analysis tool provided excellent modeling of non-linear effects, but required user-generated macros to extract frequency domain parameters such as s-parameters and waveform harmonics. Even at S-band, low on-chip parasitics allow useful signaling impedances within the chip of ohms to thousands of ohms. Some of the essential elements of the bipolar ASIC design are shown in the simplified schematic of Figure 4. Although on-board capacitors are available for RF applications, all circuits were designed to be DC-coupled for ease of DC testing. For lowest crosstalk and stability risk at s-band, differential signaling was used externally and internally.

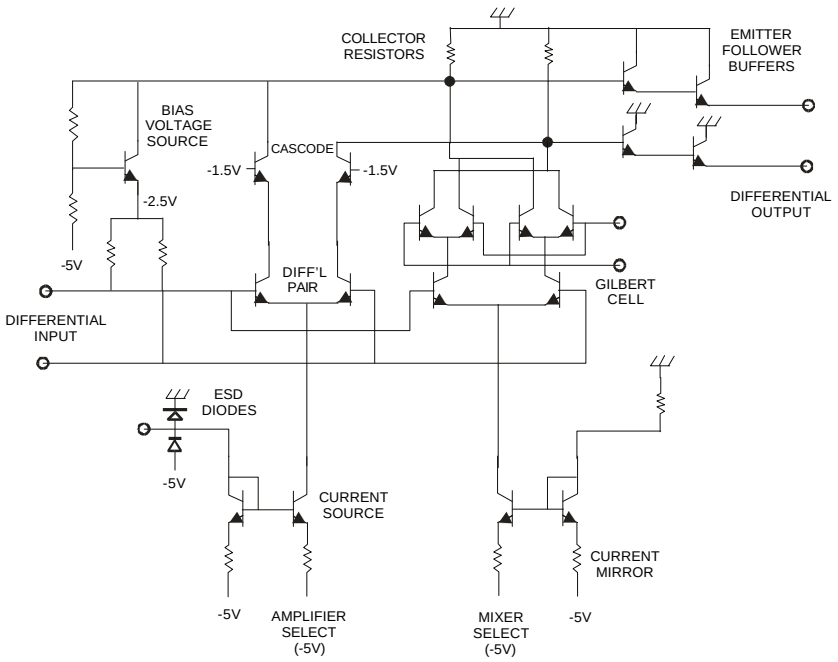

Figure 4. Elements of NPN Bipolar ASIC Circuitry

Because RF currents delivered to off-chip loads are supplied by the NPN emitter followers, RF return currents come from the positive supply rail, making it a clear choice for the ASIC ground. A negative supply voltage is applied to the negative rail. Because the negative rail powers only inherently high isolation active current sources, the negative supply exhibits little conducted RF emission or susceptibility. A power supply voltage of –5 V is used for the Dash 1 RF configuration to accommodate the higher voltage headroom requirements of flip-flops with sets and resets. The Dash 2 part is used at frequencies below 50 MHz and is usually powered between +5 V and ground.

Most transistors in the Chameleon design are .7 mA types with 27 GHz f_t , 0.002 pf collector to base capacitance, and a V_{be} of about 0.9V. A small number of large area devices are also used. Almost all resistors are polysilicon type with a +/- 30% tolerance and high temperature coefficient but excellent ratio tracking. The designer can also specify custom low drift nichrome resistors up to a thousand ohms. A few capacitors under 3 pf are available, as are Schottky diodes. Schottky diodes are available near each bonding pad for ESD protection of I/O.

Collector swings are on the order of a few hundred millivolts and devices are biased with low V_{ce}, most in the 0.6 to 1.5 volt range. To avoid current injection into the substrate, collector to emitter saturation is avoided. A few PNP's are available in the NPN process, but these are of lateral construction and were not used due to their low performance and susceptibility to radiation. Good complementary NPN/PNP processes are also available, but speed is lower.

Transistor devices on the chip are generally biased in the 0.2 to 0.5 mA range, while larger area emitter followers with 3 mA bias are used to drive external loads. The silicon substrate is conductive, so only a thin layer of glass separates the metal layers from ground, making interconnect capacitance as high as 0.3 pf for cross-chip runs. Emitter followers are used to drive s-band signals from one side of the chip to the other.

CHAMELEON FUNCTIONS

Electrical performance of the 13 circuit blocks within Chameleon makes it a good component base for many different space applications. The variable gain amplifier exhibits 26 dB insertion gain, with a 3 dB point of 500 MHz and a matched gain at 2.3 GHz of about 17 dB. The VGA is selected by supplying a bias current which doubles as a gain control port for receiver AGC applications. Figure 4 shows a VGA of similar design. Figure 4 also shows a Gilbert cell mixer similar to the one in Chameleon. Adding emitter degeneration to the mixer reduces conversion gain to 6 dB, but provides the linearity and analog accuracy needed within the transponder application. Note that the LO is fed to the mixer through the VGA. Mixer LO and RF inputs are designed for up to 2.5 GHz

operation, but the mixer output has a 3 dB point of 500 MHz, limiting the IF to below 1 GHz.

Figure 5 shows a simple latch circuit made from a Gilbert cell. The left differential pair acts as an amplifier feeding the shared collector resistors, while the right pair has the outputs tied back to its inputs in positive feedback fashion to provide the latching function. The bottom pair selects between the amplifier mode and latch mode. A pair of these latches can be cascaded to create a master/slave flip flop. Two master/slave flip flops are combined with a NAND gate to yield the phase/frequency detector which operates up to 700 MHz.

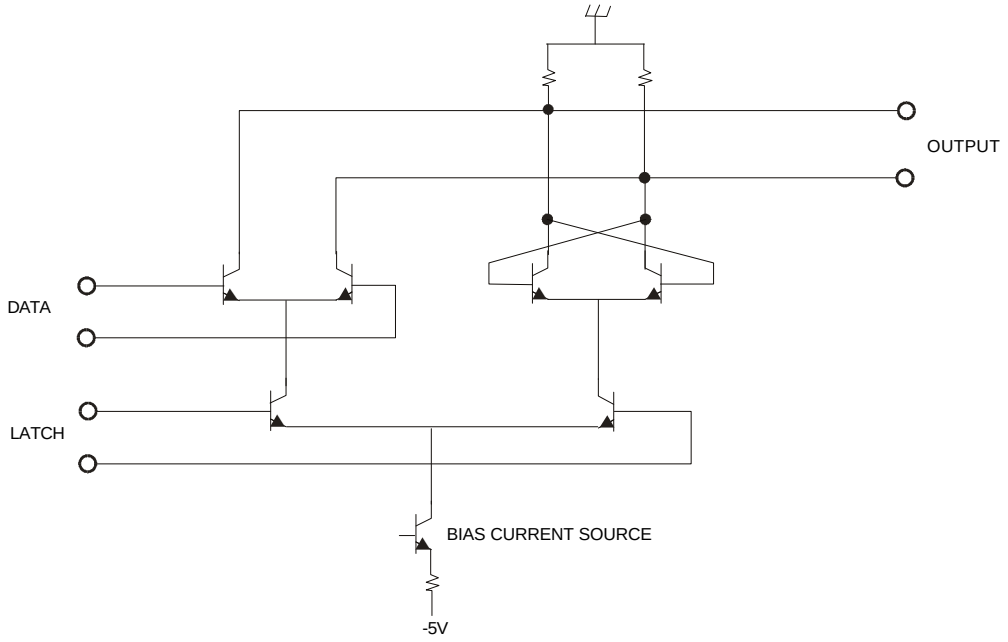

Figure 5. NPN Bipolar Latch

Master/slave D flip-flops are configured as shift registers with feedback as shown in Figure 6, to yield the divide by 2, 3, 4, and 5 prescaler functions. The divide-by-three prescaler of Figure 6 shows the shift register with its two flip flops can assume any of four possible states, with an incoming clock causing it to progress from one state to a predetermined following state due to the logical feedback to the shift register input. The feedback logic is selected to put the circuit in a 3-state loop with all possible states leading into the desired loop. Design of the other prescalers is similar. Maximum frequency of operation is around 4.5 GHz, but the 18 contact LCC package resonance limits actual performance to around 3 GHz.

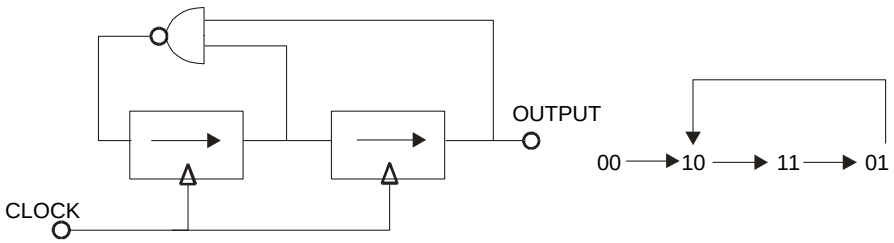

Figure 6. Divide-by-Three Prescaler

Three Dash 2 tone detectors (see Figure 3) demodulate the 3-tone SGLS command signals in the transponder. Gilbert cell mixers make up the in-phase (I) and quadrature (Q) mixers. A string of divide-by-two prescalers makes up the divide-by-128 function, with the last divide being done by two flip flops in parallel. One toggles on positive transitions and the other toggles on negative transitions, yielding quadrature outputs to drive the I/Q mixer. An external crystal is tied from the output of a differential pair amplifier to its input to form the oscillator function.

The RMS summer is an analog shaper circuit which provides an output voltage proportional to the RMS summation of the I and Q input voltages to indicate total RMS voltage in the tone. In the three-tone application, the comparator indicates whether this voltage is larger or smaller than the detected tone voltage of another tone detector. The accuracy of the tone detector system depends on close voltage matches between base/emitter junctions on the chip.

The Dash 2 Chameleon also includes a linear phase detector consisting of two master/slave flip/flops for ranging signal demodulation. The phase detector operates at frequencies up to 100 MHz.

RF INTERFACING

To ensure in-circuit performance of Chameleon prior to release of prototypes to the foundry, circuit operation was modeled to include external components and board parasitics associated with the actual circuit environment. Figure 7 shows the most common methods used to interface to the differential inputs and outputs of the RF ASIC. Differential signaling is used almost exclusively for its higher gain and lower crosstalk. Several differential filters, both discrete and printed, are used in the transponder design. Half wave lines are used above 1 GHz to adapt single ended sources and loads to a differential format. Output swings are on the order of 0.5 V p-p on each output. These levels are compatible with the ASIC inputs, making them cascadable.

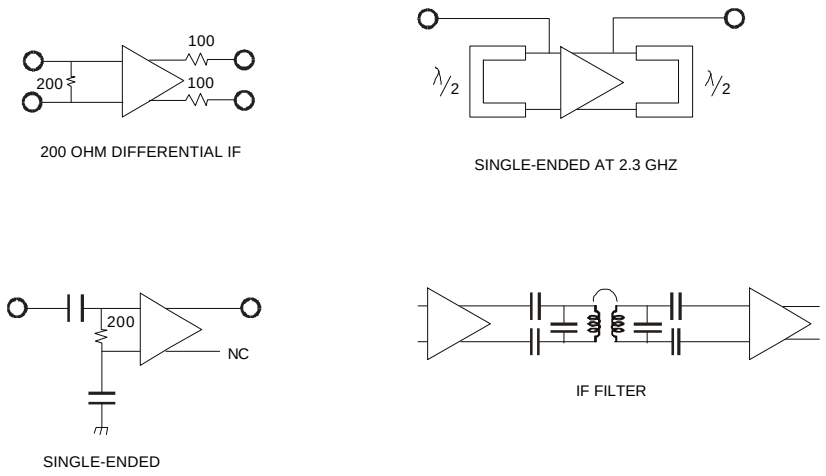

Figure 7. RF Interfacing Methods

SELECTION OF ASIC PROCESS

Silicon bipolar was chosen over GaAs FET technology because of the low frequency application (below 2.5 GHz) and because of the consistency of DC parameters such as V_{be} needed for analog signal processing. Radiation tolerance was known to be in the 1 Mrad area when trench isolation is used between devices. Single-event upset was not a concern in this application, but absence of single event latchup tendencies was of paramount importance. SiGe was also considered, but in 1996 was not available to the average user.

Conic selected MAXIM in Beaverton, Oregon for its track record of first-pass success, excellent full-feature proprietary development software, accurate electrical models, and foundry turnaround time of 14 weeks to first parts. A reasonable price provided the software, designer training, factory support, design reviews, and the first prototype parts. Design software is SPICE-based with a good user interface and capability for electrical design, chip layout, and electrical and layout rule checking. The Conic development system was UNIX-based, but current versions are now NT-based for PC's. Effective software and accurate electrical models were considered essential to minimizing risk with the considerable investment in the Conic in-house ASIC design task. For flight production parts, MAXIM provided wafer level DC test software and wafer probing services.

The MAXIM GST-2 high speed NPN process was chosen for its S-band capability and the availability of the GST-2 QuickChip. The commercial process was mature and processes were well-controlled. QuickChip provides wafers of chips with pre-fabricated devices laid out waiting for the last four metal layers to connect devices according to the custom application. Devices are conveniently located in tiles containing many transistors, diodes, capacitors, and Schottky diodes. Several digital tiles contain large numbers of

small devices ideal for the many flip-flops used in the design, minimizing routing compromises with the predetermined device layout. Of the 900 transistors available on the QuickChip, Chameleon used 800, a high usage factor. A few custom low drift nichrome resistors on one of the four metal layers were used in several locations where high analog accuracy was important.

PACKAGE SELECTION

Package selection is critical in any application, but even more so for space applications at S-band. To avoid cracking of solder joints in a wide temperature range thermal cycling environment, package size must be kept small. A .26 x .26 inch 18 pin leadless ceramic package was selected for its small size, hermeticity, and low lead inductance. Figure 8 shows the internal bonding of the .070 x .075 inch chip. An all-gold system is used for bonding and eutectic die attach. Part dissipation ranges from 60 to 130 mW depending on function selected. Junction to case temperature rise is less than 5° C.

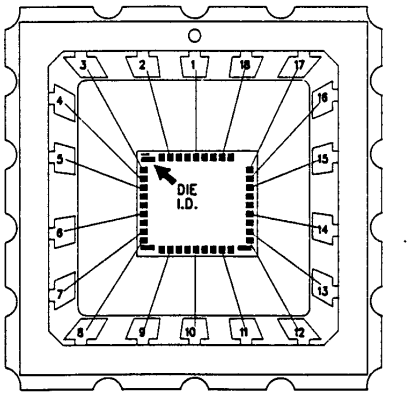

Figure 8. RF ASIC Package

Package lead inductance is about 0.6 nH, low enough to place its resonance with the VGA and mixer input capacitance beyond the maximum frequency of use. Package feedback from output to input is minimized by placing the inputs and outputs on opposite sides of the chip and package. Differential operation of inputs and outputs eliminates coupling via the ungrounded lid for applications above 1 GHz.

THE DESIGN PROGRAM

Conic found the custom RF ASIC design process quite different from circuit board based RF design. The design process lasted 5 months and yielded first-pass success with no changes for production masks. Key to success was commitment to a completely focused four person group which combined a mix of system and circuit synthesis capability, extensive practical bench experience, and computer RF design and software installation

support capability. The ability to work a wide range of highly interacting activities in parallel made the effort quite intense. Success depended heavily on specific focus activities partitioned into six development phases.

In the Setup Phase, computer hardware was installed, design software was brought up, familiarization with the design tools completed, and training at the foundry completed. The Synthesis Phase saw the transponder block diagram synthesized and analyzed and schematics for the ASIC circuit functions synthesized. A package was selected and pinouts defined early in the program.

All circuit blocks were modeled, analyzed, and optimized in the Modeling and Design Phase, which also included synthesis of the function selection method and integration of the ASIC circuit models into a complete chip model. The Layout Phase was concurrent with the last half of the Modeling and Design Phase and caused significant changes in interface designs as the high capacitive loading on lines crossing the chip became apparent.

With the completion of design synthesis, the Checkout Phase provided exhaustive model checks of chip performance over high and low temperature and high and low process variations. The ability of the MAXIM software tools and models to predict process variations was a key element in first-pass success. This phase also included definition of 100% DC testing for the foundry wafer probing activity and definition of functional testing and fixtures for flight part screening. After thorough design reviews provided by the foundry, the design was submitted for a 100 unit engineering run.

Parts were available 14 weeks after design release, initiating an intense Evaluation and Verification Phase using evaluation boards designed and fabricated to exercise each function. Parts were installed in prototype transponder boards and 6 weeks after receiving engineering parts the production run of 10,000 parts was started and completed. Qualified and screened ASIC's are being installed in production space transponder flight hardware.

TESTING AND SCREENING

Chameleon chips are wafer-probed for full DC parameters at the foundry and packaged by Space Electronics Incorporated (SEI) in San Diego, CA. A single package and chip type is used, but the separate Dash 1 and Dash 2 bonding options create two part types in the packaged state.

SEI performs part qualification and flight unit screening of Dash 1 and Dash 2 Chameleons to 883 Class S levels, doing both DC testing and functional testing of the Dash 1 and Dash 2 parts. Screening includes 100 hour burn-in and 100% DC and

functional testing at –55 and + 125 C. Test fixtures were developed by both SEI and Conic for automated testing of DC and functional parameters.

CONCLUSION

A custom silicon bipolar ASIC provided a highly effective single-chip solution for the Conic S-band transponder for space applications. The selection of a single-chip "function toolbox" approach simplified chip design so that first pass success was achieved. The design provides a universal building block for future space products. The emergence of higher capability modeling tools, foundry compatibility, and a growing number of engineers who can install and use CAD tools makes direct electrical design and chip layout by the designer an increasingly approachable solution for new analog, waveshaping, RF, and high speed digital applications. For many specialized communications applications, accurate analog signal processing using custom high speed ASIC's can yield significantly higher speed, smaller size, lower power, and better radiation tolerance than digital signal processing.

ACKNOWLEDGMENTS

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