DIGITAL FILTERING OF MULTIPLE ANALOG CHANNELS

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ABSTRACT

The traditional use of active RC-type filters to provide anti-aliasing filters in Pulse Code Modulation (PCM) systems is being replaced by the use of Digital Signal Processing (DSP). This is especially true when performance requirements are stringent and require operation over a wide environmental temperature range. This paper describes the design of a multi channel digital filtering card that incorporates up to 100 unique digitally implemented cutoff frequencies. Any combination of these frequencies can be independently assigned to any of the input channels.

KEY WORDS


INTRODUCTION

Anti-aliasing filtering of transducer inputs to a sampled data system have historically been implemented with analog filters. Typically a six pole butterworth filter with a cutoff frequency equal to the maximum signal frequency has been used. If the bandwidth of the system is limited, filters with more poles could be used to decrease the over-sampling ratio. Analog filters requiring high accuracy, over a range of temperatures and for long periods of time, are expensive and difficult to design.

As an alternative to analog filtering, a DSP device can be used to do the filtering by mathematical calculations. Digital filters are computers that process the data with formulas that do not change with time or temperature.Removing the analog filter from the system removes its fixed errors and environmental errors. However, a DSP filter requires an increased sample rate from the analog to digital converter (ADC). Since an ADC is already required in a system with analog filters, the only difference with using digital filters is the increased cost of a faster ADC. This design change usually has no effect on the system budget, since the cost of a DSP chip is now less than the cost of eight well built analog filters for eight channels.
DESIGN CONSIDERATIONS

SYNCHRONOUS VS ASYNCHRONOUS DATA TRANSMISSION
One of the first design decisions was whether to synchronize the sampling frequency to the PCM format sample rate. If the rates are not synchronized then the DSP will be sampled in the PCM format such that occasionally one DSP sample is sampled twice by the PCM format. Ideally each DSP sample is sampled one time by the PCM format. If the input signal is being well over sampled, or if the output analysis will be done by strip chart, there is not a significant problem. If, on the other hand, the input signal is a frequency close to the DSP filter cutoff, and a fast Fourier transform (FFT) type analysis is done, the analyzed data will contain energy spikes associated with the asynchronous sampling, which may be a problem.

If the DSP and PCM are synchronized, then there are constraints that must be imposed on the format to allow proper DSP operation, and each of the filter coefficient tables and decimation tables must be tailored for each PCM format. Asynchronous operation was chosen for maximum flexibility and minimum development cost for each application.

SAMPLE RATE
Because the DSP is a sampled input system, it still requires that something be done to prevent aliasing of the input signal components. If the signal energy spectrum is not known in advance (as in this case) then some type of analog filter is still required. In order to keep the analog anti-aliasing filter simple and of minimal effect to overall response, it is necessary to have the sampling rate much above the analog filter. We chose a 4 KHz two pole Butterworth analog filter, which gives about 40 dB of attenuation at the lowest DSP aliasing frequency (at 41.7 KHz - 1.3 KHz = 40.4 KHz). A problem with going above a 41.7 KHz sample rate is that the calculation time increases because more points are taken and this increases the coefficient table length, which increases processing time. Also the common gain stage of the signal amplifier and the ADC must work faster.

FIR FILTERS
The type of digital filter used for this design is the finite impulse response (FIR) filter. The FIR filter gets its name from the fact that it responds to an impulse input for only a finite amount of time. This is because the filter has no feedback of the output signal to be mixed with the input signal. The output is only a linear combination of present and past inputs (see Figure 1). There is no analog equivalent to this type of filter. One problem with this type of filter is that if the sampling frequency is much higher than the cutoff frequency, a very high order filter is required, resulting in a large number of clock cycles to calculate each output point. Since the output values do not rely on knowledge of previous output values, then decimation of the input sample frequency to get a lower rate output sample frequency can be achieved by calculating only those values desired. The result is a much
faster filter. Another option is multistage FIR filters with the first stages acting as anti-
aliasing filters for later stages. The resulting sum of stages is faster than using only one
stage.

![FIR Filter Block Diagram](image)

**FIGURE 1**
**FIR FILTER BLOCK DIAGRAM**

Referring to Figure 1, the 99th order FIR filter works as follows. The 16 bit input signal is
multiplied by a0 and added to the previous input multiplied by a1. This sum is then added
to the input from two time periods ago (multiplied by a2) and so on until the sample from
98 periods ago is multiplied by a98 and added into the sum.[1, p68]

**DECIMATION**
Because the DSP filter is after the ADC converter, there can still be frequency fold back or
aliasing problems. If the sample rate of the ADC is the same as for the analog filter case,
then the same accurate analog anti-aliasing filter would be required. To get around this
problem, the input is sampled at a much higher rate than the output sample rate. This
allows a much simpler input anti-aliasing filter. However, for the output rate of the DSP
filter to be at the proper lower system rate, a process known as decimation is used. In this
process, only selected output values from the filter output calculations are used. If the
input sample rate is some integer multiple of the output rate, the process reduces to a very
simple procedure of only outputting every Nth output calculation, where N is the ratio of
input to output sample rates. Because the other output values are not used, they do not
need to be calculated, and the total amount of calculation time is reduced
proportionally.[1, pp87,93,126]

**FILTER STAGES**
With an FIR filter, the farther apart the sample rate is from the cutoff frequency of the DSP
filter, the longer the coefficient table (number of calculations per output data point). Given
the DSP chip used, it was decided to limit the coefficient table to 256 points as part of the
DSP memory allocation strategy. While the number of calculations is reduced by
decimation, the calculation length of 256 required that the filtering be done in multiple stages. It was found that with 256 points, the early stages could decimate up to 20 times, while the last stage, with its sharper cutoff is limited to a decimation of eight. Available memory and processing time limited the design to four stages maximum.

With an input rate of 41667 SPS, three stages of 20 decimation and one stage of 8 decimation, the result $41667/(20 \times 20 \times 20 \times 8) = 0.65$ SPS. For a sample rate to cutoff frequency ratio of four, 0.16 Hz is the lowest frequency filter that can be calculated.

**CUTOFF FILTER**
While the specification is +/-0.05 dB up to Fc, and -65 dB at 2 Fc, most filters are actually meeting +/-0.005 dB at Fc, ignoring any effects of the analog front end filter. At 2 Fc, most filters are in a null of at least 72 dB in the output stage. The analog filter adds 3.01 dB at 4000 Hz, 0.26 dB at 2000 Hz, and 0.02 dB at 1000 Hz. The filter coefficients were obtained using a DSP filter design program from Momentum Data Systems, and are Kaiser Window designs. A typical filter response is shown in figures 2 and 3. [2]

**GROUP DELAY**
Filters with the very sharp rolloff exhibit an associated large group delay. Basically group delay in DSP is due to each calculation and decimation. Because these are fixed for a particular filter, the filter delay is fixed, therefore the phase shift verses frequency is linear.

**ANALOG INPUT CIRCUITS**
The input stage has a preliminary gain programmability of 1, 10, 100, and 1000. There is a bridge balance DAC per channel, which can also be used for quick voltage calibration. There is internal input zero calibration. Each input amplifier is followed by a 4 KHz low pass filter and an 8:1 MUX. Next is a common gain stage of 1, 2, 4, or 8 followed by a programmable offset DAC.

**INTERNAL CALIBRATION**
Calibration takes 256 samples of input and averages them to get a level relatively free of noise. An error delta based upon the input signal verses the desired output as defined in a look up table is computed. Calibration attempts to correct any parasitic effects that would cause a deviation in the card's transfer function from its ideal value of $Y = G \times V + O$ where $Y$ is the output, $G$ is the gain, and $V$ is the input. Gain calibration is fully defined for all of the card's gain/channel combinations. The ideal set points can be set by the user. Gain calibration is performed after the final filter stage calculation. A subsequent offset calibration is performed. Since gain and offset calibration interact, successive iterations must be performed until the interaction error reduces to a value below the quantization level.
FIGURE 2
ROLLOFF BODE PLOT

FIGURE 3
ROLLOFF BODE PLOT
A percent tolerance (customer definable) for each gain/channel for both zero scale and full scale is available. This sets the limits on how far calibration will attempt a correction before the DSP assumes fault condition exists and halts subsequent computations.

Calibration can be performed with a precision reference input signal, or with the actual aircraft signal. Calibration can also be performed with an internal input short, or an internal input reference (via the bridge balance DAC). If the internal reference is used, a look-up table sets the DAC. During calibration the offset DAC is also set to a value from a calibration lookup table.

BOARD TEST
The board contains boundary scan logic for a digital Field Programmable Gate Array (FPGA) and an equivalent port on the DSP to ease board level test. All DSP firmware is located on a card mounted Electrically Erasable Programmable Read Only Memory (EEPROM) that can be reprogrammed without removing it from the PCB, allowing updates or reconfiguration without modifications of the hardware.

FILTER SELECTION
The card has pre-loaded filter coefficients with 0.1% accuracy every 10% value from 0.196 Hz to 1000 Hz. Due to the two pole 4 KHz analog filter used before the ADC, there is a slightly greater error above 1000 Hz.

For a 6 pole analog Butterworth filter, the -0.01 dB point is at 0.6 Fc and the -72 dB point is at 4 Fc giving a pass-band to cutoff ratio of 6.7:1. For the typical DSP filter in this design, the -0.01 dB to -72 dB cutoff ratio is 2:1, or only two times the Nyquist limit. An equivalent analog filter with regard to amplitude would be 13th order. This can be used to reduce the required bandwidth to 30% of that required for the same signal using 6 pole analog filters.

FINAL PRODUCT DESCRIPTION
The DSC-108 is an 8 Channel Differential Bridge Conditioning Card designed for use in Aydin Vector's PCU-8XX Series II family of data acquisition systems. See Figures 4 and 5 for the DSC-108 block diagram. Each channel consists of an instrumentation amplifier with 16 software programmable gains followed by a digital filter with up to 100 software programmable cutoff frequencies from 0.215 Hz to 2.15 KHz, plus an unfiltered mode. The offset can be adjusted on a per channel basis in the DSC-108 overhead. This will allow an input of 10 Volts/Gain between +10V and -10V (i.e. for a gain of one, the input could be set for -10 V to 0 V, -7.5V to +2.5 V, -2.5V to +7.5V, 0V to 10V, etc.). The digitized ADC output has a full scale range of 48 to 4048 counts. There is also a hardware
FIGURE 4
INPUT STAGE BLOCK DIAGRAM

FIGURE 5
OVERALL BLOCK DIAGRAM
programmable unipolar constant voltage excitation source provided on the card. Bridge excitation voltage is fixed at 2.5, 5, or 7.5 volts with a strap option that affects excitation outputs on a channel-pair basis.

The DSC-108 also supports zero calibration ("CAL1" disconnects external inputs and shorts the amplifier inputs to ground) and shunt calibration ("CAL2" connects a user installed resistor in parallel with one leg of the bridge). These modes can be asserted through the PCU-8XX overhead via external switches. The DSC-108 provides a bridge balance circuit per channel. Each balance circuit is designed to provide up to 10V of correction voltage to balance a bridge. Bridge balance scaling resistors are provided on the card for each channel. A resistor is connected to the negative input on each channel and is mounted on terminals so they can easily be changed by the user. An input voltage calibration mode can be utilized by connecting the bridge balance circuit directly to the channel input. The open circuit deflection voltage available is 0 to 10 volts.

The eight channels of the DSC-108 can be randomly accessed and output into the PCM stream through the PCU-8XX overhead. If the system is running at less than 16 bits per word, the LSBs of the words will be truncated. The truncated bits can be recovered in the following word by performing an "extended read" command. Note that, although the input ADC is 12 bits, if the input noise is random and at a higher frequency then the DSP filter, more then 12 bits of resolution are available. This is due to the phenomena of dithering.

CONCLUSION

The use of DSP in signal acquisition filters will substantially increase accuracy over existing analog filters without the increase in cost that would be associated with better analog filters. However, the use of asynchronous sampling must be weighed against the increased accuracy of the filters and the sharper roll off. The use of DSP also allows the changing of filter parameters with remotely controlled software changes as opposed to the changing of physical parts in an analog filter.

REFERENCES
