MULTI CHANNEL AC POWER MONITOR USING DIGITAL SIGNAL PROCESSING

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ABSTRACT

The monitoring of multi phase 400 Hz aircraft power includes monitoring the phase voltages, currents, real powers, and frequency. This paper describes the design of a multi channel card that uses digital signal processing (DSP) to measure these parameters on a cycle by cycle basis. The card measures the average, peak, minimum cycle, and maximum cycle values of these parameters.

KEY WORDS

Power monitor, Digital signal processing(DSP), Alternating Current, Telemetry.

INTRODUCTION

Most aircraft have multiple sources of Alternating Current (AC) power. These are usually derived from generators running off of the aircraft's engines. While these generators produce a nominal constant frequency that is usually 400 Hz, it can vary considerably. This includes the DC to 400 Hz variation during engine turn on. Furthermore, the output of one generator is not normally synchronized to any other generator. Because of all the variables associated with AC power generation, it is often desirable to monitor the power distribution during aircraft testing. One method would be to treat the AC signals (voltage and current) as instantaneous signals to be recorded or transmitted. This method consumes a large amount of bandwidth, with little information content. Another method is to measure only certain parameters, or perhaps only the limits of certain parameters. This will substantially reduce the bandwidth required to store or transmit the information. The latter approach is what is used in this design.

REQUIREMENTS

The circuit card is required to monitor all three phases of a three phase generator. The parameters being measured by this circuit are listed in Table one. Note that the minimum and maximum cycle root mean square (RMS) values are available (voltage, current, and power), which is not the case in some systems.

	Average (RMS)	Peak	Minimum (RMS)	Maximum (RMS)
Voltage	yes	yes	yes	yes
Current	yes	yes	yes	yes
Power	yes	no	yes	yes
Frequency	yes	no	no	no
Number of Cycles	yes	no	no	no

TABLE 1
TABLE OF MEASUREMENT REQUIREMENTS

The AC input frequency can vary from 20 Hz to 1000 Hz. The sample period is also variable. It can be either a function of the AC input signal or the telemetry format sample rate.

DESIGN CONSIDERATIONS

SAMPLING

When the design was first considered, one approach was to sample at a fixed rate of 64 times the highest frequency (64 x 1000 Hz = 64 KSPS). This method would require that the number of samples per cycle be measured. A sum of squares calculation would then be made. Finally, the number of samples per cycle would be divided into the sum of squares. The DSP allows up to 256 sums without overflow, therefore the input frequency would be limited to 64/256 = 1/4 of the maximum rate of 1000 Hz, or 250 Hz, which was not acceptable. Consequently it was decided to add a phase lock loop (PLL) to give a 64 times clock from the input frequency to drive the Analog to Digital Converter (ADC).

The input AC signal applied to the first channel is conditioned to generate an interrupt to the DSP during its -/+ zero crossing. The interrupt initiates the processing of the previous 64 samples of each of the 8 input channels. The samples are stored in a circular buffer in the DSP. The DSP then performs a sum of squares calculation. The result is divided by 64 and then the square root is taken.

$$RMS = ((\sum X^2)/64)^{0.5}$$

For the purpose of calculating RMS values, the only sampling requirement is that a complete cycle of the input be captured. The absolute phase angle of the signal is

unimportant. However, the measurement must begin and end at the same phase angle. This technique allows voltage and current inputs from a multi phase generator to be measured using only one signal as a reference. The RMS power is calculated by taking the instantaneous voltage and current {RMS = (∑VxI)/64}. This takes into account any phase difference between the voltage and current, giving real power out.

SYNCHRONOUS SAMPLING

Voltage and current must be sampled at the same time in order for power calculations to be correct. Calculated power is then the instantaneous voltage times the instantaneous current. No regard need be given to the phase angles between the signals. To implement this method of sampling, at least two separate sample and hold amplifiers that can maintain accuracy over the wide sampling rate are needed. Alternatively, two ADC converters can be used. For this design an ADC per channel was chosen. The eight converters are all driven by the same control signals, so that they all sample at the same time. The outputs of the converters are digitally multiplexed to the DSP, where they are saved into a circular buffer. By using a circular buffer (as opposed to a linear buffer), only the buffer address pointer value at the time of calculation interrupt needs to be saved. The buffer (which is set to twice as long as the data needs) can continue to fill with new data as the old data is used for calculations.

DIGITAL PHASE LOCK LOOP

This circuit monitors the AC frequency coming into the unit and uses it to gate a counter that counts the number of system clocks (16 MHz) per AC cycle. The counter is constrained to limit its minimum and maximum values to meet the card requirements of 20 Hz to 1000 Hz input range. The output of the counter is divided by 64 and feeds another counter as its jam inputs. The second counter runs at 64 times the input frequency. Its output clocks the ADC to measure the input signal at 64 equally spaced points during one input cycle (see figure 1). Because the 64x clock can not be a perfect subdivision of the input clock, there will be up to 4 us of error, or 0.16% error at 400 Hz input. As a first order approximation, the error will cause a cycle RMS calculation to be in error by the same amount.

INPUT

The input is a differential instrumentation amplifier with over voltage protection. By using attenuation resistors on the printed circuit board (PCB) the input can be driven up to 100V. At levels above that point, or if the common mode voltage is above a few volts, an isolation transformer is needed on the input. The inputs can also be used at lower voltages or with a low output current transformer, by adding a gain resistor to the input amplifier. All calculations are done based on the amplifier output values being in the range of +/- 10 volts full scale. It was determined that most users would use isolation and current transformers to match the normal +/- 10 volt input range and would therefore not have to add resistors to the PCB.

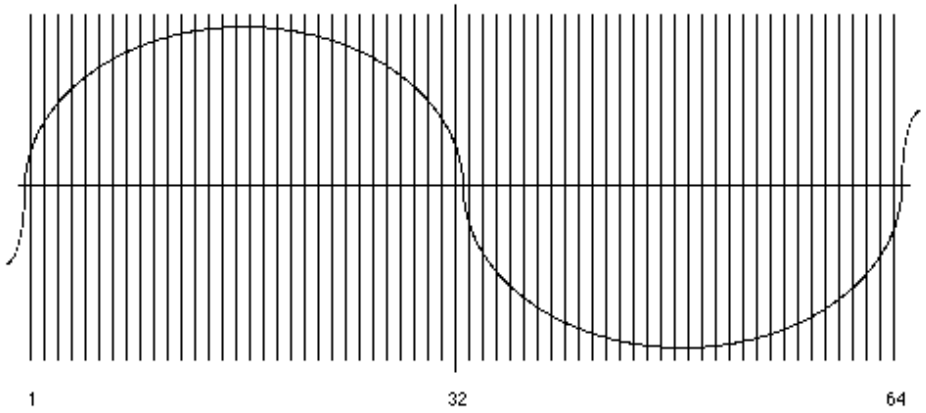

FIGURE 1
SAMPLED SINE WAVE

INTERNAL CALIBRATION

The card has the ability to automatically calibrate small gain and offset errors arising in either the PCB's components or external errors. Calibration takes 64 samples of the input and averages them to provide noise rejection. An error delta between the input signal and the full scale test voltage output (as defined in the DSP program) is calculated. Calibration is done with a precision DC reference input signal. The gain and zero calibration are not updated in the electrically erasable programmable read only memory (EEPROM) unless the signal values are within the tolerances set in the DSP program. This sets limits on how far calibration will work before the DSP assumes that an incorrect signal was applied and calibrating should not be done.

BOARD TEST

The board contains boundary scan logic for an on card digital field programmable gate array (FPGA) and an equivalent port on the DSP, to ease board level test. All DSP firmware resides in an EEPROM, that can be reprogrammed without removing it from the PCB. This allows updates or reconfiguration without modifications of the hardware.

FINAL PRODUCT DESCRIPTION

The ACP-108 is an eight channel power monitoring card for use in Aydin Vector's PCU-8XX family of data acquisition systems. See Figure 2 for the ACP-108 block diagram. Each channel consists of a resistor attenuator and high frequency filter, followed by a resistor programmable gain instrumentation amplifier (IA). With no attenuation and unity gain, the circuit gives an input of 20 volts peak to peak (Vpp) full scale. To increase the range, reduce the gain with the attenuator resistors. {R = l00 KΩ∗ (attenuation/(1-attenuation))}. To decrease the range, increase the gain with the gain

resistor {R = 50 KΩ/(G1)}. Next is a 4 KHz anti-aliasing filter. Each channel has a separate ADC. The ADCs convert simultaneously to give matching samples of voltage and current for power calculations. Four channels are designated as voltage input and four channels are designated as current input. The assignment is arbitrary except that the first channel must maintain adequate signal level to operate the zero crossing detector used to measure cycle length. Also, if using the power calculations, the corresponding Voltage (V) & Current (I) pairs must be maintained. Frequency measurements are based on channel #VA only. Also the sampling of all eight channels is based on channel #VA. For correct calculations, all channels must be at the same frequency as channel #VA, however the phases may be different. In this way the card can be used to monitor the outputs of a three phase generator, with one spare pair of inputs. The card can also be used to monitor eight voltages related to the same generator. Calculations are done by taking 64 samples of each cycle. The card can lock on to frequencies between 20 Hz and 1000 Hz. Each cycle sample timing is based on the previous cycles time. Therefore if the input frequency shifts, there will be an error in the calculation due to sampling at the wrong rate and including (or excluding) a portion of a cycle. This error is proportional to the cycle by cycle frequency shift. For input frequencies outside of these ranges the sample rate will free run at about 16 SPS, with calculations on groups of 64 samples. In this way DC power can be monitored.

There are four types of measurements performed on each of the eight inputs. Peak signal sample (absolute value), the highest cycle average, the lowest cycle average, and the average of all cycles since the last reset. Averages are all RMS. The amount of cycles averaged and monitored before a reset (called a block of data) is a function of the PCU-8XX sample format. The reset point can be set as a function of the format. Reset occurs each time the reset bit is present (normally once per major frame) or once every 4th, 16th, or 64th time the reset bit is present. There is a limit of 256 maximum cycles per block of data before data is overwritten. There is an output available that gives the number of cycles used in the last data block calculation. The card can also be set to reset after each 16th, 64th, or 256th input frequency cycle, without regard to the PCU-8XX frame words. Reset pulses may also be set to occur as often as every ACP-108 card output to the PCU-8XX bus. Power calculations are done based on an instantaneous calculation of VxI, with an RMS average per cycle and per block. There are also minimum and maximum cycle values saved per block.

The frequency output is the block mean of each cycle time in that block, measured using a one microsecond crystal clock time base. The output is a period measure in binary counts of microseconds (16 bits maximum). If the input frequency drops below 20 Hz, the signal output loses correlation to the input frequency. The card may be auto calibrated for zero scale and full scale (7800/7FFF)x(+10 volts) = 9.375 VDC. The offset correction is done on a sample point by point basis, while the gain correction is done to the final result of each calculation.

The card outputs in a 16 bit per word format, however the MSBs can be read in a reduced word length if desired. There is also a special "no response" code to allow the reading of extended words in a reduced word format.

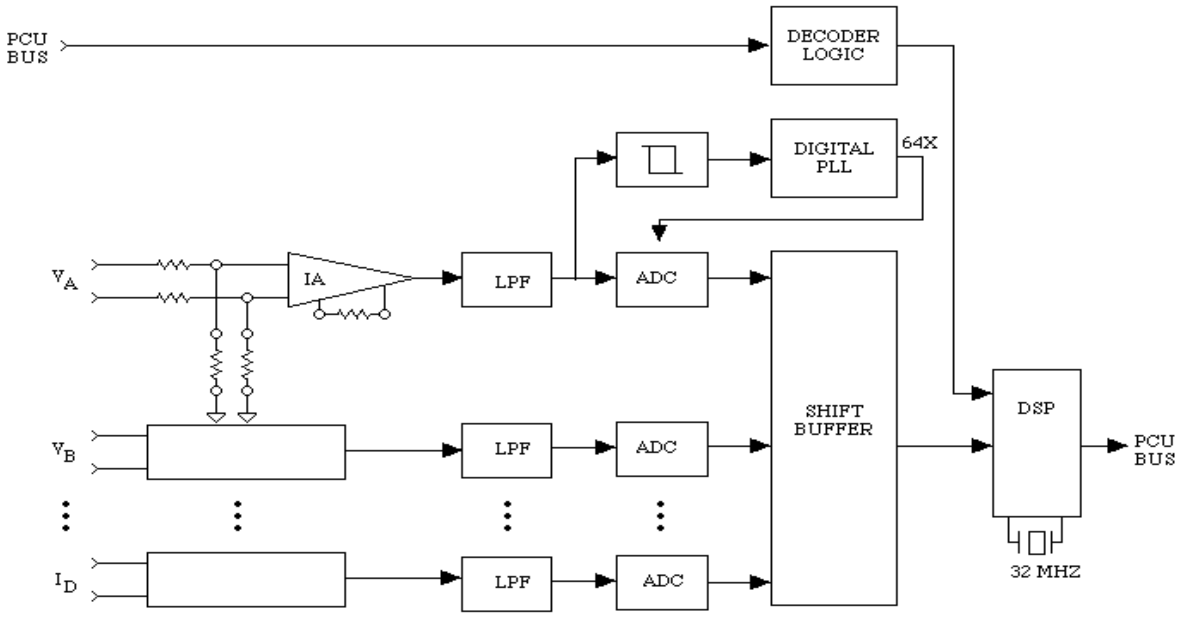

FIGURE 2
BLOCK DIAGRAM

CONCLUSION

The ACP-108 can be used to monitor 4 sets of voltage and current, eight voltages, one voltage and seven currents, or any combination that has at least 1 voltage to drive the zero crossing detector reliably. For power calculations, voltage and current must be paired. The unit will work from 1000 Hz down to DC. However, below 16 Hz the card will no longer synchronize to the AC signal, and should only be used for scalar measurements bellow 20 Hz. The eight inputs should be all be at exactly the same frequency, otherwise the calculations will be in error.

Using traditional sampling of the 400 Hz signal for a pair of voltage and current results in 614 KB/Sec. (2Ch x 400Hz x 64SPCycle x 12BPW = 614,400BPS).
Using the ACP-108 card with processing on the card and 256 samples per average gives only 225 B/Sec. (1Ch x 12readingsPCh x 400Hz x 12BPW/256CyPAv=225BPS). This results in a bandwidth reduction of 2731:1, with very little loss of information.

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