DESIGN OF A DIGITAL VOICE ENCODER CIRCUIT

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ABSTRACT

This paper describes the design and characteristics of a digital voice encoding circuit that uses the continuously variable slope delta (CVSD) modulation/demodulation method. With digital voice encoding, the audio signal can be placed into the pulse code modulation (PCM) data stream. Some methods of digitizing voice can require a large amount of bandwidth. Using the CVSD method, an acceptable quality of audio signal is obtained with a minimum of bandwidth. Presently, there is a CVSD microchip commercially available; however, this paper will describe the design of a circuit based on individual components that apply the CVSD method.

With the advances in data acquisition technology, increased bit rates, and introduction of a corresponding MIL-STD, CVSD modulated voice will become more utilized in the flight test programs and a good knowledge of CVSD will become increasingly important. This paper will present CVSD theory, supported by graphical investigations of a working circuit under different conditions. Finally, several subjects for further study into CVSD will be addressed.

KEYWORDS

Continuously Variable Slope Delta Modulation, A/D Conversion, Voice Encoding

INTRODUCTION

There are a variety of methods available to incorporate voice into pulse code modulation (PCM) data streams. One disadvantage of these methods is that they use a large percentage of the bandwidth available in the relatively low bit rate systems of

the past. If the voice data with a 3 Khz bandwidth was treated as a regular analog signal converted into a 12 bit PCM word, it would require 72 Kbs to send using the nyquist criteria.

Delta modulation tracks the audio signal in a series of timed steps and delivers a serial data stream of one's or zero's which corresponds to an increase or decrease of the input frequency. For example, if the sample tracked by the encoder detects that the audio signal is rising, it will output a one and if it detects a decrease in the signal it outputs a zero. This is known as linear delta modulation. The step size is a fixed value and this can result in slope overload conditions unless a very high sampling rate is used. What is needed is a circuit that can change the step size between samples when a large change in the input is detected.

The method used to design the encoding circuit in this paper is known as continuously variable slope delta (CVSD) Modulation/Demodulation. CVSD circuits have the ability to change the slope size when the serial data indicates a large change in the input signal. The bandwidth requirements for CVSD are much lower than that required of PCM or linear delta modulation for the same quality signal. This paper will describe the design of a circuit based on individual components that apply the CVSD method.

ENCODING METHOD

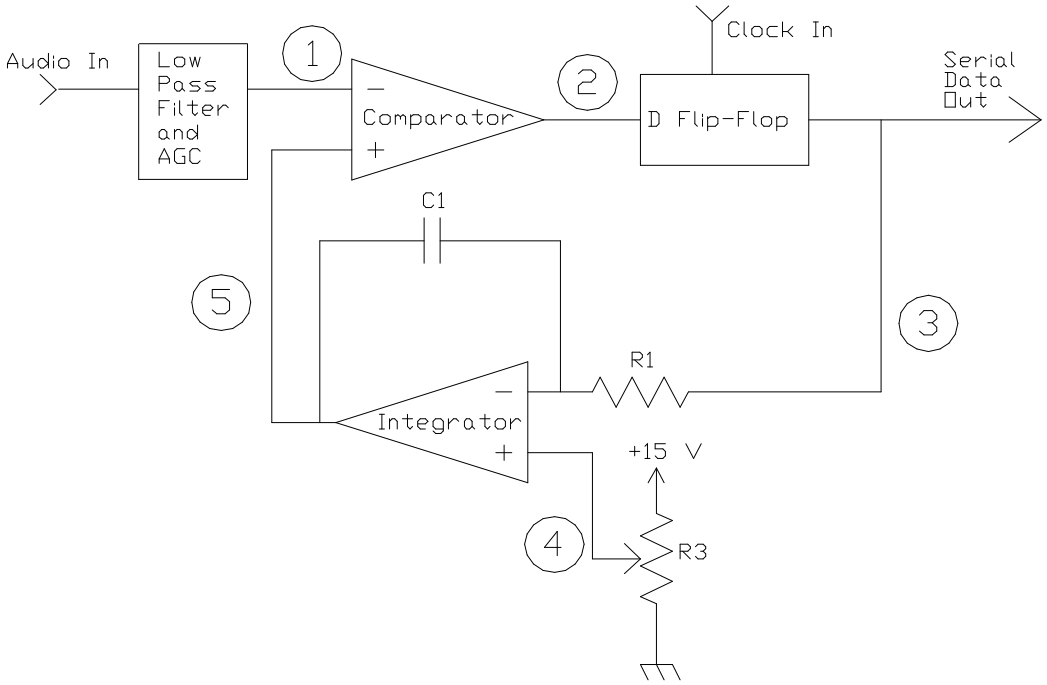
Since a CVSD circuit is a modification of a linear delta modulation circuit, the delta circuit will be explained first to gain a basic understanding of the fundamentals of digital encoding.

Linear Delta Modulation

An explanation of the linear delta modulation circuit will be shown by following the block diagram in Figure 1.

The process starts with the input of the audio signal. Proper operation of the circuit is dependent on the voltage levels of the signal being within certain voltage and frequency limits to avoid an overdrive condition. This is accomplished with an automatic gain control (AGC) and low pass filter. The filter is designed to pass audio tones which are generally between 50 to 3,000 Hz. After filtering and level adjustment, the signal is present at point 1.

Figure 1: Delta Modulation Block Diagram



To start this example, the non-inverting input of the comparator will be at ground. The audio signal will be considered to be above ground. With these conditions, the comparator output is a negative voltage at point 2. The D flip-flop will respond with a TTL low signal (zero volts) at point 3 with the new clock pulse. This low signal makes the first bit in the serial data out a zero. The clock for the circuit will generally run between 10 and 64 kHz. Above these frequencies, the quality of the audio shows little improvement with an increased sampling rate.

The integrator is biased at approximately 1 volt at the non-inverting input at point 4. With this bias, the integrator responds to the low voltage at the inverting input with a high output. An integrator circuit converts the output into a ramping up voltage signal. The slope of the ramp is calculated with the equation:

$$SRckt = Vm/(2*R*C) \qquad (1)$$

SRckt = slew rate of the circuit in volts per second (V/s)
Vm = is the peak to peak voltage of the square wave input.
R = Resistor between input signal and inverting input
C = Capacitor between inverting input and output

Example 1: The capacitor value is .1uF and the resistor value is 2,000 ohms with an input pulse of 3.15 volts. The resulting circuit slew rate is 7.88 volts per millisecond (V/ms). This increasing voltage is seen at point 5.

The comparator now sees an audio signal at point 1 and the ramping voltage at point 5. One of two conditions can now exist. If the audio signal has a high frequency and is increasing rapidly, the voltage at point 1 will have increased faster than the voltage of the integrator ramp at point 5 and the comparator output will remain at the negative voltage level. This will repeat the process just described, sending another zero into the serial data stream (point 3) and leaving the integrator to continue its increasing voltage ramp.

If however, the audio signal does not increase faster than the integrator voltage ramp, the comparator will see a greater voltage on the non-inverting input and will instead change the output to a positive voltage. The flip-flop now responds to the high voltage at point 2 by outputting a TTL positive voltage representing a one with the next clock pulse. This voltage (approximately 3 volts) is the next bit in the serial data stream and the integrator responds with a voltage output sloping down.
The downward sloping voltage is seen at the comparator at point 5 and the process of comparing the audio input level and the integrator's ramp voltage continues with each clock pulse.

CALCULATIONS

The limitations of the delta modulation circuit are realized when the slew rate of the input signal exceeds the adjusted slew rate of the circuit. When this happens, the full amplitude of the signal cannot be reached and distortion of the high frequency components of the signal occur.

The slew rate of a sine wave is calculated at the point of the maximum change on the curve; the point between an upper and lower peak. The slope at this point is calculated by the equation:

$$SRsig = Vm * pi * f \quad (2)$$

where SRsig = slew rate of th e signal in V/s
Vm = Peak-to-peak voltage of the signal
pi = 3.14
f = frequency of the signal in Hertz

Example 2: A 500 Hz, 5.0 volts peak-to-peak (Vp-p) signal would have an SRsig of (5.0*3.14*500)=7850 V/s or 7.85 V/ms. A signal with twice the frequency or twice the voltage would have an SRsig of 15.7 V/ms.

Slew rate limits of the circuit can be found by using equations 1 and 2. For example, an input signal of 3,000 Hz, 5 Vp-p is sent to a delta modulation circuit with a slew rate of 16.25 V/ms. The input signal has a period of 1/f or .333 ms. The time interval between a low-to-high or high-to-low peak is half the period or .167 ms. If the time interval is multiplied by the slew rate of the circuit, the maximum voltage swing for this circuit at this frequency is found to be:

.167 ms * 16.25 V/ms = 2.71 Vp-p

To determine the maximum slew rate that can be sent into this circuit without distortion, reverse the process using the maximum output voltage to find the slew rate.
Using equation 2 with Vm=2.71 and f=3,000, SRsig is found to be 25.53 V/ms. Dividing the rates results in:

SRsig / SRckt = SR ratio (3)

25.53 / 16.25=1.57

Therefore, multiplying the SRckt by the SR ratio results in the maximum slew rate that the circuit can handle without a reduction in the output amplitude.

SRmax=SRckt*1.57 (4)

This method can be applied to determine the output limitations for other frequencies.

Example 3: A 1,000 Hz, 10 Vp-p signal is applied to the circuit with a SRckt=16.25 V/ms. From equation 4, SRmax=25.5 V/ms. SRsig calculated from equation 2 is 31.4 V/ms. Since the slew rate of the signal is greater that the adjusted slew rate of the circuit, amplitude limiting will occur.

These limitations can be overcome by giving the circuit a large SR; however, this adversely affects the low-level signals sent to the encoder. Since the integrator ramp

will increase a set amount with each clock pulse, a signal with an amplitude less that the voltage rise of the integrator will not be encoded.

ILLUSTRATED EXAMPLES

To help illustrate the delta modulation process, a set of examples with o-scope displays are provided.

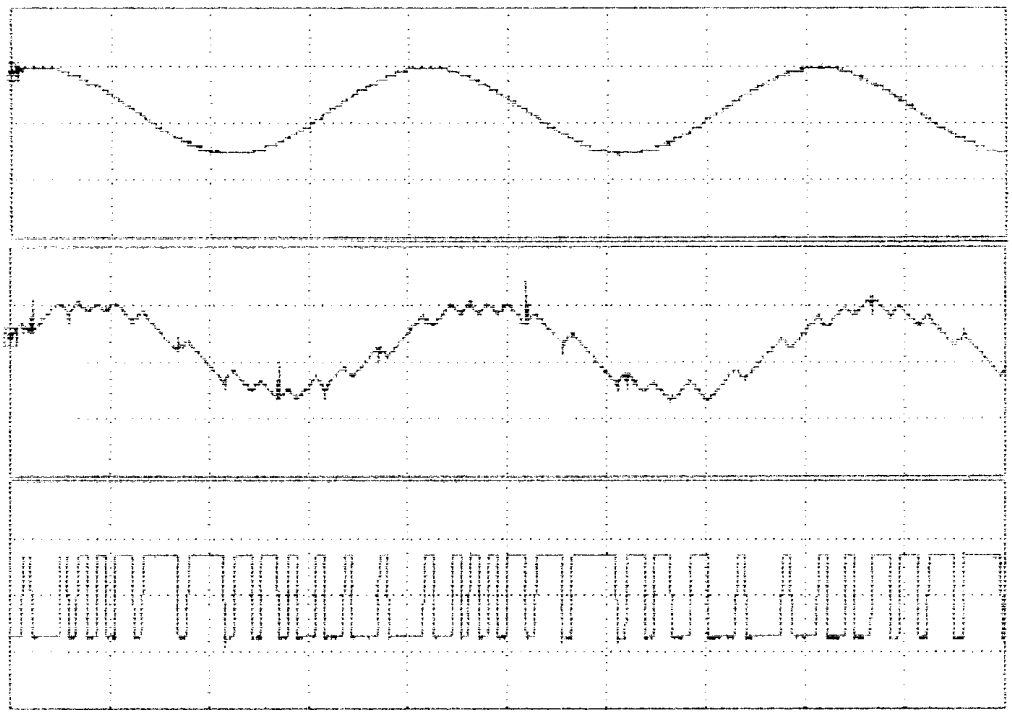
The first set of displays (Figure 2) shows the encoding of a 500 Hz sine wave at 3.0 Vp-p. The first display (2a) is the input signal taken from point 1. Figure 2b is the integrator ramping output voltage at point 5 with which the audio signal is compared. Figure 2c is the serial data output from the D flip-flop and the final display is the clock input. For this example, the clock is set at 20 Kbs. The integrator time constant is set at 200 microseconds (us) for the following 2 examples. With the input pulses from the D flip-flop of 0 to 3.15 volts, this results in a slew rate of 7.88 V/ms.

Figure 2: Delta Modulation Encoded Signal
Input signal: 500 Hz, 3.0 Vp-p, SRsig = 4.71 V/ms Circuit: SRmax = 12.4 V/ms, 20 kHz clock

Figure 2a: Point 1
Audio Input
2 V/div
500us/div

Figure 2b: Point 5
Feedback
2 V/div
500us/div

Figure 2c: Point 3
Serial data out
2 V/div
500us/div

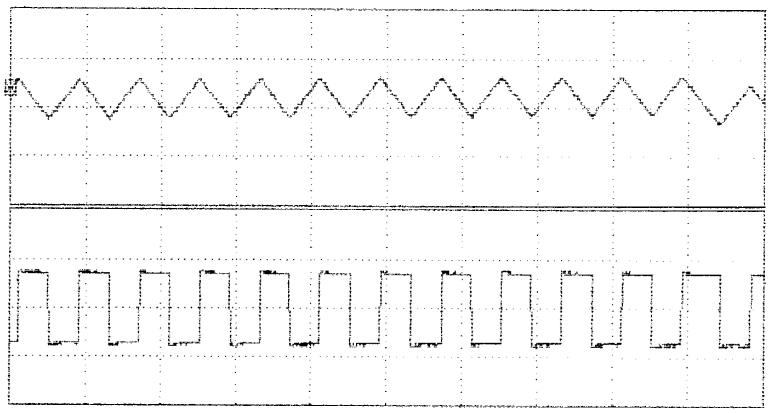


The second set of displays (Figure 3) shows the effects of an overdrive condition resulting from a higher input frequency. The input signal is 2,500 Hz at 3.0 Vp-p and the feedback waveform is only at 1.5 Vp-p.

Figure 3: Delta Modulation Encoded Signal; Frequency Overdrive Example
Input signal: 2500 Hz, 3.0 Vp-p, SRsig = 23.55 V/ms Circuit: SRmax = 12.4 V/ms, 20 kHz clock

Figure 3a: Point 5
Feedback
2 V/div
200us/div

Figure 3b: Point 3
Serial Data Out
2 V/div
200us/div



This frequency overdrive condition can be corrected by setting the resistor-capacitor (RC) constant of the integrator circuit to a higher level, resulting in a steeper slope. Doing this, however, causes an underdrive condition with the lower frequencies and smaller amplitude signals. This happens when the audio signal changes less than the height of the integrator ramp. The change in amplitude cannot be resolved and the dynamic range is associated with clock frequency.

What would be desirable is to have a variable slope circuit that increases the slope of the integrator feedback when a signal with a large amplitude or frequency was detected. This would preserve the quality of the lower frequencies and enable the higher frequencies to also be tracked. The continuously variable slope circuit provides this ability.

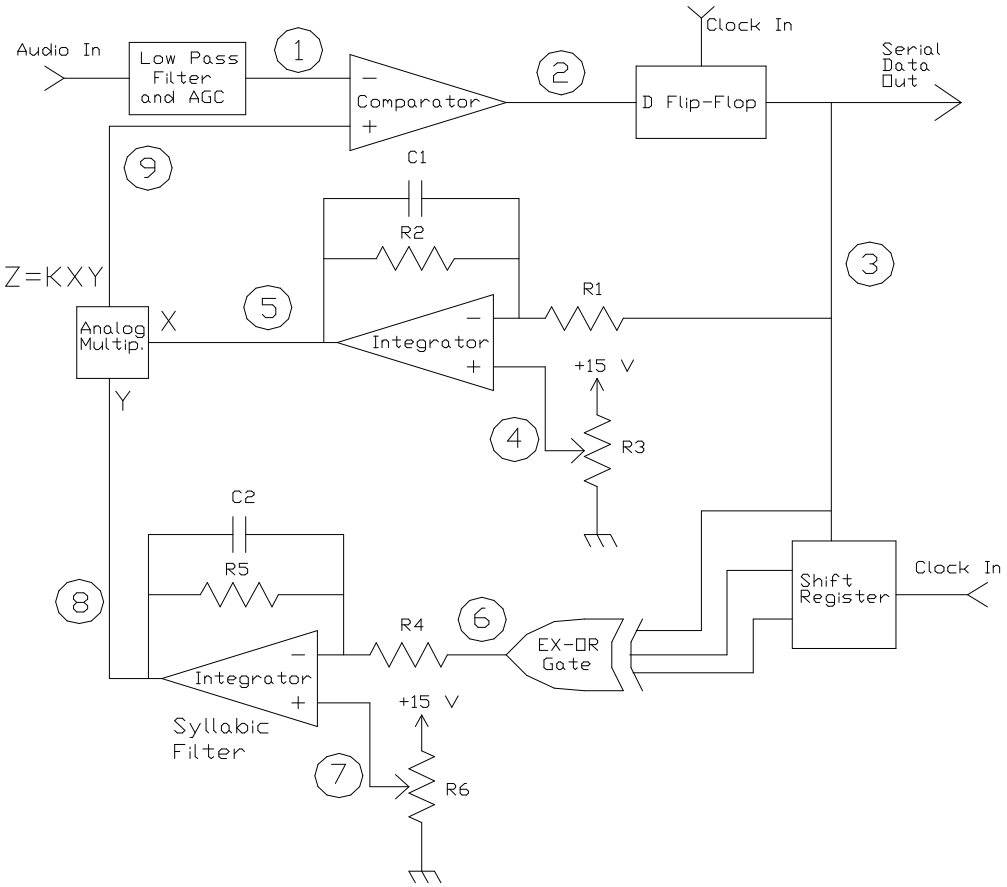
FUNCTION OF THE CVSD CIRCUIT

The CVSD circuit is the delta modulation circuit with an additional feedback circuit. This feedback monitors the serial data stream of the encoded audio. When the audio input is changing rapidly with steep voltage ramps, the serial data contains many ones or zeros in a row as the integrator output is failing to keep up with the audio

input. The additional feedback circuit receiving the serial data activates when 3 ones or 3 zeros in a row are seen. Once activated, this circuit increases the slope of the integrator feedback to the comparator.

An explanation of the CVSD circuit operation is shown by following the block diagram in Figure 4.

Figure 4: CVSD block diagram



The serial data at point 3 is sent into a shift register. Output from the register and the current data bit are sent to an Exclusive-Or gate. Output from the gate at point 6 is in a high state (3 volts) until 3 ones or 3 zeros in a row are sent to its inputs. When this occurs, the output goes low and the additional integrator know as a syllabic filter is activated. The RC time constant is proportional to the length of a typical syllable, therefore the term syllabic filter is used. The syllabic filter responds to the low input with an upward ramping voltage output at point 8.

The sylballic filter output is sent to one of the inputs of an analog multiplier. If the signal has not been slewing rapidly and the syllabic filter is not activated, the output at point 8 is at a level that will cause the analog multiplier to have a gain of one. The other input of the multiplier is the output from the integrator of the delta modulation circuit. In this configuration, the voltage ramp from the delta modulation integrator being sent to the comparator is increased (or decreased) more rapidly when the serial data indicates a rapid change. If the serial data continues to be ones or zeros for a period of time, the syllabic filter continues to ramp up and increase the multiplication factor, providing a better signal following ability.

ILLUSTRATED CVSD EXAMPLE

The graph shows the reconstructed signal at point 9 of the completed CVSD circuit. Although this frequency would be slew limited in the linear delta modulated circuit, it does not show the effects with the CVSD circuit. This waveform is comparable to Figure 3 where the same signal resulted in a frequency overdrive condition. Without the syllabic filter, the waveform would still follow the frequency but would have a reduced amplitude.

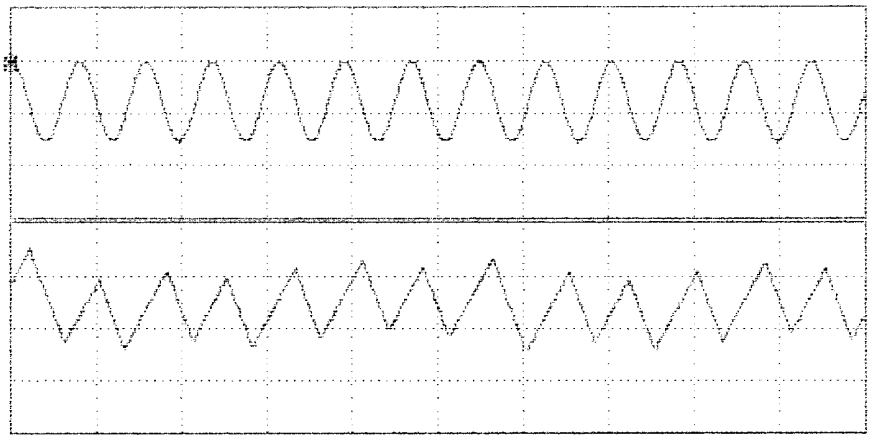
Serial Data Placement

Now that the encoding of the voice has been explained, the serial data are sent to the data acquisition system. The serial data stream is sent to a buffer where it is fed as a parallel word. The placement and removal of this data into and out of the PCM are beyond the scope of the paper.

Figure 5: CVSD Output for an input signal of 2500 Hz, 3.0 Vp-p Clock = 20 kHz

Figure 5a: Point 1
Signal input
2 V/div
500us/div

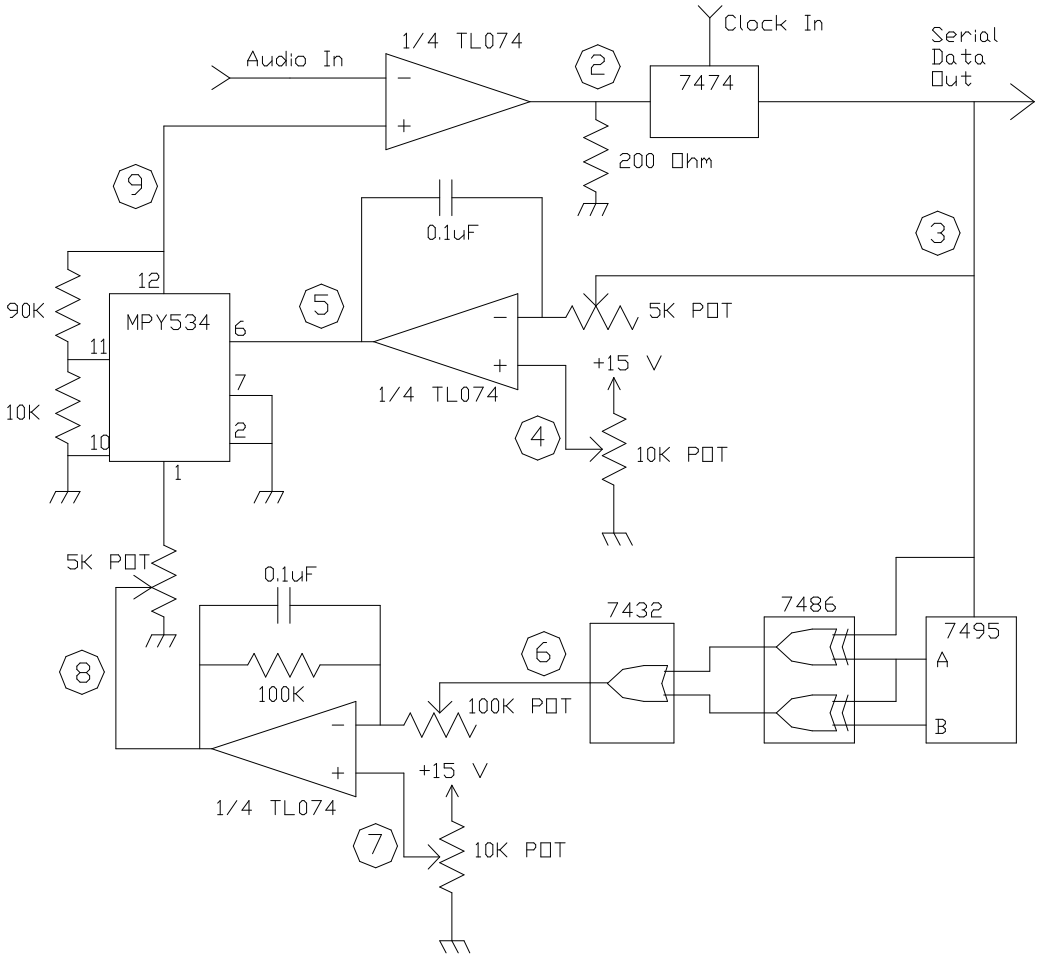
Figure 5b: Point 9
Feedback
2 V/div
500us/div



THE ACTUAL CVSD CIRCUIT

A circuit diagram for the functional CVSD circuit is show in Figure 6.

Figure 6: CVSD Circuit Diagram



With C1 = .1uf, the potentiometer allows the slew rate to be adjusted. For this paper, the rate was adjusted between 500 and 2,000 ohms. The voltage at point 4 is 1.4 volts and the voltage at point 7 is 1.2V.

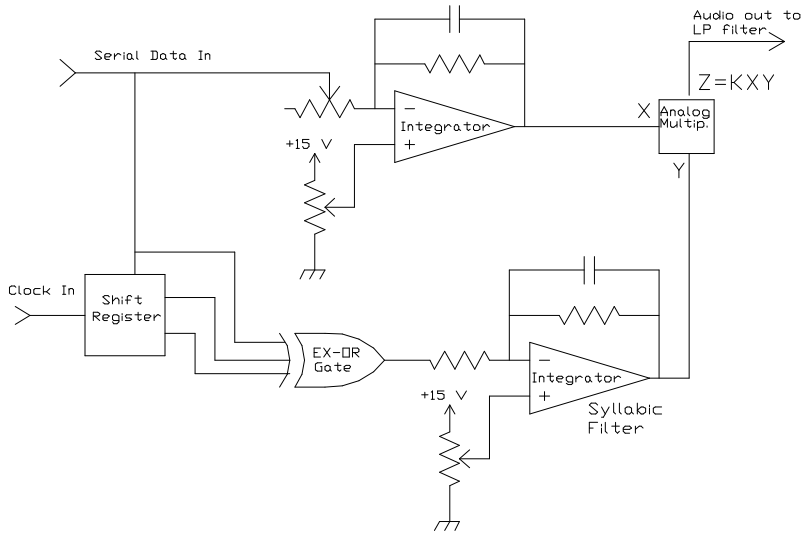
The Burr-Brown analog multiplier MPY534 is configured for an output of the pin 1 voltage times the pin 6 voltage with no additional gain and the TL074 op-amps are powered with positive and negative 15 volt supplies.

For the syllabic filter, the input resistance was adjusted to 50K Ohms and the output resistance to 2K Ohms. With these settings, the minimum voltage to the multiplier was 1 V and the maximum is around 3.5 V.

DECODING

Decoding the CVSD encoded voice is just a matter of sending the bits through a modified encoder circuit. The circuit functions like the encoder and the resulting jagged waveform is filtered and amplified. A block diagram of a decoder circuit is shown in Figure 7.

Figure 7: Decoding Circuit



SUMMARY

The CVSD encoding technique is an effective and simple way to place audio signals into a PCM data stream. The circuit can be built out of commercially available integrated circuits and the process uses a fraction of the bandwidth required by linear PCM encoding.

This paper started with an explanation of the linear delta modulation circuit. Through calculations and graphical analysis, the function and limitations of this encoder were investigated. It was determined that an additional feedback circuit would improve the performance at higher frequencies. With this modification, the encoder becomes the

CVSD circuit and the limitations of the linear delta modulation circuit are overcome. This is demonstrated with a signal that was distorted in the linear delta modulation circuit and is transferred with better resolution in the CVSD circuit.

Although straightforward, the actual designing and construction of the circuit can contain a number of different variables and settings which can produce a wide range of results. The circuit as designed here has a higher voltage requirement than the commercially available CVSD integrated circuit encoder. Further study could be done to build a circuit with a lower voltage requirement. Other areas of study could include a comparison of signal to noise ratios for different slew rates and clock frequencies. The technique of placing the data into a parallel word with different data acquisition systems can also be addressed.

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