IN FLIGHT DATA REDUCTION FOR REDUCED BANDWIDTH TRANSMISSION

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ABSTRACT

The desire to acquire large quantities of high speed vibration and acoustic data during aircraft testing is usually satisfied through on-board high speed recording methods. However there is often a need to have some of this data instantly available at the ground station for flight safety and other purposes.

A Data Processor (DP) has been developed allowing an airborne data acquisition system to acquire large amounts of wideband analog data, process the data in real-time, and develop reduced bandwidth information from high bandwidth channels. The reduced data can be inserted into a Pulse Code Modulation (PCM) stream and telemetered via a Radio Frequency (RF) link with a potential for a 2000:1 reduction in bandwidth.

This on-board processing capability also lends itself to additional tasks such as the generation of a reduced bandwidth marker channel which can flag critical time periods of data activity. This flagging technique can be used to facilitate ground station analysis of specific segments of data, resulting in significant cost and time savings.

KEYWORDS

Data reduction, Airborne telemetry, Real-time data reduction, Wideband Data.

INTRODUCTION

Wideband data gathering in aircraft testing has traditionally used Frequency Multiplexed (FM/FM) multiplexing techniques in conjunction with wideband FM analog recorders and the associated ground decomutation and display equipment. The recovered data was frequently digitized for subsequent computer analysis. Digital PCM data measurements have required two sets of ground support equipment (both FM and digital). Today, most aircraft test programs do all digitization on the aircraft

with high speed PCM systems, and FM/FM techniques are being used less and less. As a result, most of today's ground stations can utilize a single set of "digital" ground support equipment.

With the advent of "all digital data" in today's aircraft, the ability to perform airborne data reduction in real time, and to transmit the reduced bandwidth data to the ground station is a very real need. Aydin Vector Division has developed this capability for use on the Lockheed-Boeing Air Force F-22 aircraft. The design concept and general operating features of this design are described in this paper.

WIDEBAND DATA

On each F-22 vehicle, there are from 6 to 12 Wideband Data Acquisition Units (WBRU). Each WBRU is capable of generating up to 10 Megabits per second (Mbps) of digital data. The entire system is capable of generating up to 120 Mbps of data. However, the primary data acquisition system of the F-22 (Common Airborne Instrumentation System - CAIS) is only capable of handling a up to 15 Mbps of data, including the wideband data and all other signals. In addition, the F-22 RF ground link can only handle 2.5 Mbps of data. The requirement for the in flight data reduction system was to extract certain information from the total 120 Mbps of wideband data, and perform real-time processing on this data resulting in an output rate which is compatible with the CAIS system.

The major usage of these wideband channels is for vibro-acoustic data and piezoelectric accelerometers (for wing flutter). Other uses include monitoring high frequency avionics signals, such as sinusoidal weapons systems signals.

DATA PROCESSING

The DP operates on individual channels and calculates a true Root Mean Square (RMS) average of each channel for reduced bandwidth transmission. It was decided that the best reduction technique would provide only the average signal level at a bandwidth of 10 Hz. The ground station could then monitor this low bandwidth channel for an indication of average signal level. For example, the DP can process 30 channels of 30 Kilosamples per second (KSPS) data with a total unprocessed data rate of 9 Mbps and produce a total processed data rate of 4.5 Kilobits per second (Kbps) resulting in a bandwidth reduction of 2000:1.

Processed data can be monitored in real time to verify the integrity of transducer data, eliminating the need for redoing test flights. In addition, flight safety parameters such as flutter or flutter overload can also be monitored.

The processed data can also be used during post flight data reduction as a pointer for areas of activity by identifying time slices of data to be reduced. This results in significant cost and time savings due to reduced need for ground reduction.

DESIGN CONSIDERATIONS

One of the first considerations was the handling of the sign bit contained in the WBRU data. The WBRU data is formatted as a 16-bit word which includes a 16 bit word with a 12 bit 2's complement mantissa, a 3 bit exponent, and a valid flag (used during gain changes). The exponent gives gains of 1, 4, 16, 64, 256, and 1024. The sign bit should be removed to increase the signal-to-noise ratio of the incoming data. A Digital Signal Processor (DSP) and a Field Programmable Gate Array (FPGA) Preprocessor are used in the design but several design options exist.

The DSP could have removed the sign as part of the squaring of the signal, however this would have required storing the data as 15 bits plus sign. However, by doing a one's complement rectification in the FPGA Preprocessor, the full 16 bit field could be used for the number. This results in a 6 dB increase in signal level for the three highest gain ranges.

Since the DP uses a fixed point DSP, the next design consideration was how to handle the floating point signal from the WBRU data bus. The change from pseudo floating point to fixed point could have been done in the DSP chip, however there was not sufficient processor time to do that and the other tasks. Therefore the conversion was done in the FPGA Preprocessor. The FPGA Preprocessor also monitors the valid flag in the data and changes the data value to all zeros for invalid data. The DSP can easily test for a zero value and uses the most recent good data if bad data is detected.

The RMS conversion algorithm is achieved by a square root of the sum of the squares. To keep the processing time to a minimum, some of the features unique to DSP's are used. Calculations are done on no more then 256 data points in one calculation. This is because the DSP can do up to 256 multiply-accumulate instructions (sum of the squares) with no overflow of the result register. The square root algorithm operates by making a fifth order polynomial approximation of the square root. This results in a small error (a few counts) on some values. [1, p57-60]

One of the problems encountered in the design, was how to handle the various frame formats typically used in the WBRU. The formats are often switched before flights, and sometimes during flight. However, the DP requires pre-knowledge of the frame format in order to determine which samples to include in the RMS algorithm. One method considered was to load the sample format into Electrically Erasable

Programmable Read Only Memory (EEPROM) and, if required, update it before each flight. This technique could also be extended to format switching during flight. However, it was decided that this was too cumbersome for the user, so a method of auto loading the format was devised.

The selected method operates as follows. When the unit first receives power, the unit performs an initialization sequence where it monitors and stores one major frame of address information from the WBRU address bus. With this information, along with the address assigned to this module, the entire format is reconstructed in DSP Random Access Memory (RAM). Normal data bus monitoring proceeds from this point until either power is removed, or the PCM format is switched.

To maintain alignment between the WBRU format and the DP format, the circuit performs a continuous comparison between the number of words in the major frame and the occurrence of the WBRU's major frame pulse. A counter is used to keep track of the location within each major frame. If there is ever a change in the occurrence of the major frame pulse verses where it is expected, an initialization sequence is re-initiated. This provides for the automatic handling of format changes while power is still applied.

A method was also developed to provide an indication that the DP is operating properly, especially after a frame change or if there is a momentary power loss to the unit. A Test Word is available for reading in the PCM format which counts the number of calculation cycles completed since start up.

The DSP program was optimized to minimize the processing time to a level that would allow all the processing necessary to monitor 10 Mbps. The total percentage of available time that the DSP operates on various processes is: store input data to a buffer (3%) + transfer data buffer to RAM (26%) + process data (31%) + output data (1%) = 61%. This means that the DSP is idle 100-61 = 39% of the time.

The circuits necessary to do the data reduction would not all fit into one hybrid module, and a partition into two module's was necessary. This then caused design constraints on the interconnect availability between the two modules. In order to not modify the WBRU bus structure and use the limited external interconnect capability of the two modules (37 pins), the two serial bi-directional ports and the interrupt line of the DSP were used. The WBRU modules are stackable hybrid modules measuring approximately 1 3/4" wide, 1 1/2" deep, and 1/4" thick. The DP-801/802 takes up only twice this volume. This small size makes the unit ideal for small aircraft and missiles.

WBRU SYSTEM DESCRIPTION

Referring to figure #1, the WBRU consists of from 1 to 30 input signal conditioning modules that include an auto gain ranging amplifier and an Analog to Digital (A/D) converter per channel. The modules are addressed one at a time by the WBRU bus. The digitized output of any input module is presented to the WBRU bus for output via the 10 Mbps PCM output. This is all under control of the WBRU controller, which contains the sample format sequence. The CAIS interface can sample any or all of the outputs going to the 10 Mbps PCM output, limited by the CAIS bus sampling rate. The DP-801 module monitors the traffic on the WBRU bus and outputs average values of channels to the bus as requested. Because of format restrictions, the DP-801 is sampled at least once every major PCM frame, and there can be no more then 32 minor PCM frames per major PCM frame. Therefore the PCM output bandwidth is reduced by no more then 32 to 1, even though the DP-801/802 can reduce the signal bandwidth 2000:1. The further bandwidth reduction comes from the fact that the CAIS can sample the PCU data at any rate down to the CAIS frame rate. Therefore with a 5 KHz vibration signal sampled at 20 KSPS, the CAIS output could be at a rate of 10 Samples Per Second (SPS), and retain signal level information.

DP SYSTEM DESCRIPTION

Referring to Figure #2, the data reduction system consist of two modules. The DP-801 contains a FPGA that contains the unit logic, an EPROM which contains the FPGA program, and buffers for the WBRU bus interface. The DP-801 monitors the WBRU address bus and control signals and analyzes if particular addresses represent signals to be processed. If this is true, then the DP-801 transfers the WBRU data bus value as serial information to the DP-802. If the address represents a request for DP-801/802 data, the interrupt line to the DP-802 is operated and serial data is received from the DP-802, formatted for the WBRU and put on the WBRU data bus. During power up, the DP-801 operates in a frame monitoring mode, transferring addresses to the DP-802 for analysis.

The DP-802 contains the DSP, an EEPROM containing the DSP program, a 32K x 16 static RAM for data point storage, a crystal oscillator to run the DSP, a power supervisor and watch dog timer chip, and a RAM address high bank storage register. On power up, the DSP clears RAM to all zero data. Because the operation of the DP DSP is in an EEPROM, it can be changed either in the WBRU, or with an adapter and any EEPROM programmer. This gives the DP the ability to be reprogrammed for other DSP processes as future requirements require. As an example would be the calculation of vector sums of multi-axis signals, or the filtering of wideband channels for low frequency information. The FPGA is also easily reconfigured if required, only

requiring a new assembly with a different Erasable Programmable Read Only Memory (EPROM) mounted with the new logic configuration.
Upon power up, the modules monitor the frame synchronization pulse, word strobe, and address lines. This is to determine the format that is being sent on the WBRU bus. After analyzing and storing the WBRU format, the modules change to a data monitoring mode. In the data monitoring mode, each data word is stored in a RAM buffer for later processing. When an 8K block of RAM gets filled, then a new block is opened and the old block is processed for RMS average of each channel. After a block is averaged, any where from zero to seven averages from old blocks can be averaged with the new block for a group RMS average. If any old blocks are averaged in, this creates a moving average on the data. These new group averages are then saved in a DSP register bank that is read out by the WBRU. The WBRU reads out the average, based on the sequence the request appears in a frame. The frame pulse is tested ever major frame to be sure that it coincides with the first data request count in the DP-802 word counter. If there is ever a mismatch, then a power up sequence is automatically initiated. If this occurs, the output data will be cleared to zero during initialization. Outputs will remain zero for a few milliseconds and a few frames. This reset allows for synchronizing to new frame formats on the fly.

Referring to Figure #3, the timing diagram shows a detail of a few WBRU master frames. Input data is continually stored in the DSP chip as it is received during a frame. At the end of the frame the data is transferred from a buffer register bank in the DSP chip to an appropriate section of RAM. The line "Process Data" shows test data is not analyzed until the beginning of the next group of 8 major frames, and is completed about halfway through the frame. The tasks shown are interrupt prioritized in the sequence shown in the figure.

The data is received by the DP-801 module as a 12-bit two's complement mantissa with a 3-bit scaled exponent and a valid flag. The first test on the data is the valid flag. If the word is not valid, it is changed to all zeros. An all zero code tells the DSP processor to use the most recent good value. Next the sign bit is used to rectify the data in a one's complement inversion. This results in the negative values being one Least Significant Bit (LSB) off. Next the exponent value is used to shift the eleven data bits to justify them such that for gain = 1 the Most Significant Bit (MSB) data (not including sign) moves to the MSB position of the 16 bit unsigned word. For a gain of 1024, the data is aligned 10 bits over. This gives 11-bit resolution for gains of 1, 4, or 16; 10-bit resolution for a gain of 64; 8-bit resolution for gain of 256; and 6-bit resolution for gains of 1024. This word is then sent to the DP-802 module. The DSP saves each WBRU major frame of input data (up to 960 total values) in channel sequential locations in RAM (up to 32 values per channel). Finally at the end of each block of 8 major frames (up to 256 data values per channel) the RMS average is

calculated, using a square root of the sum of squares. The output RMS value is then calculated by RMS averaging the last 1-, 2-, 4-, or 8-block averages.

CONCLUSION

The DP can provide a 2000:1 reduction in data bandwidth. This reduction can be used to support real-time transmission of critical wideband information over a relatively low bandwidth medium such as the CAIS bus or over RF telemetry. When used in conjunction with the WBRU, the DP capabilities can be applied to up to 30 wideband auto gain ranging analog channels.

REFERENCES

1 Mar, Amy, ed. Digital Signal Processing Applications Using the ADSP-2100 Family, Volume 1, Englewood Cliffs, NJ: Prentice-Hall, Inc., 1992

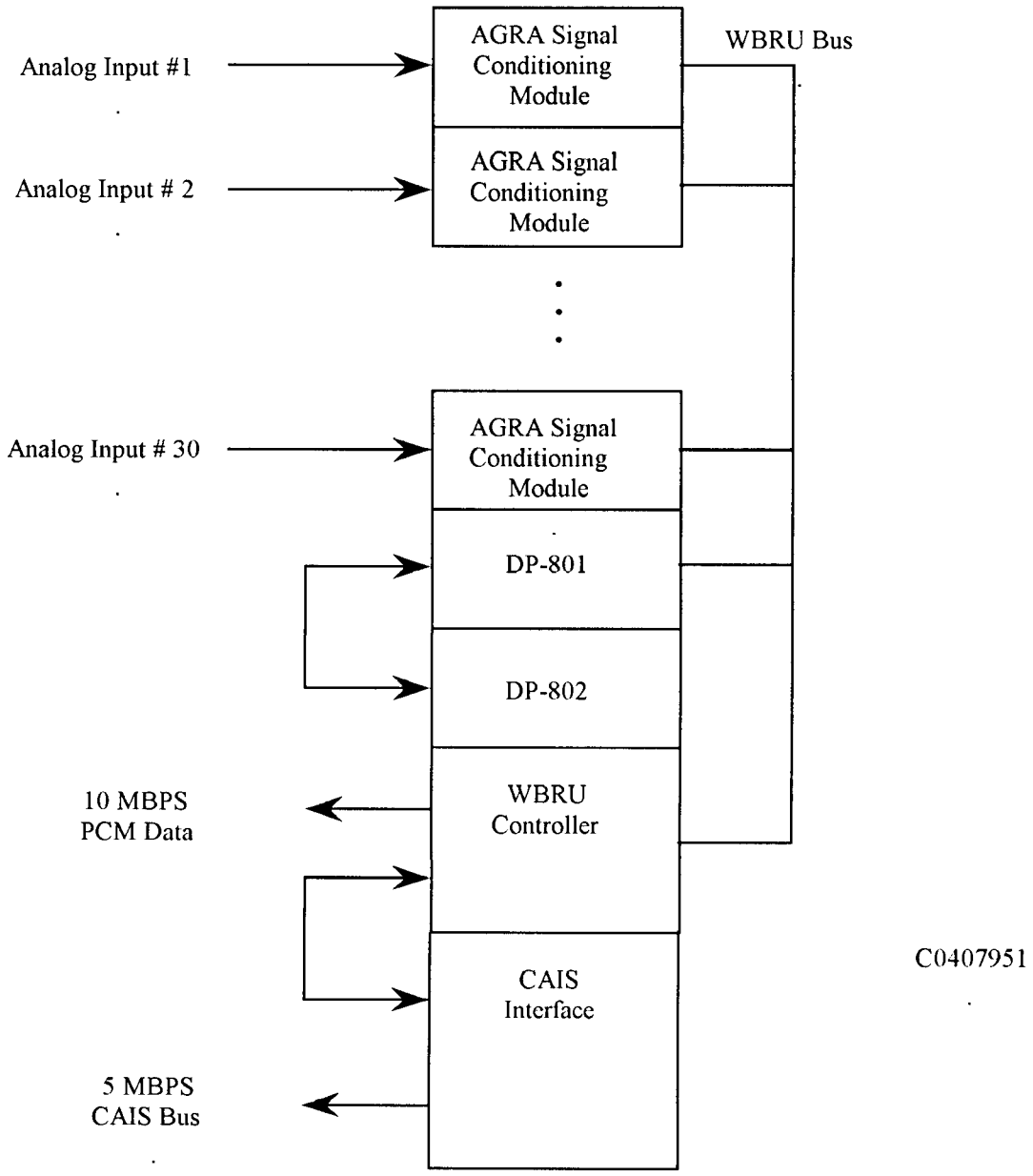

Figure 1. WBRU Block Diagram

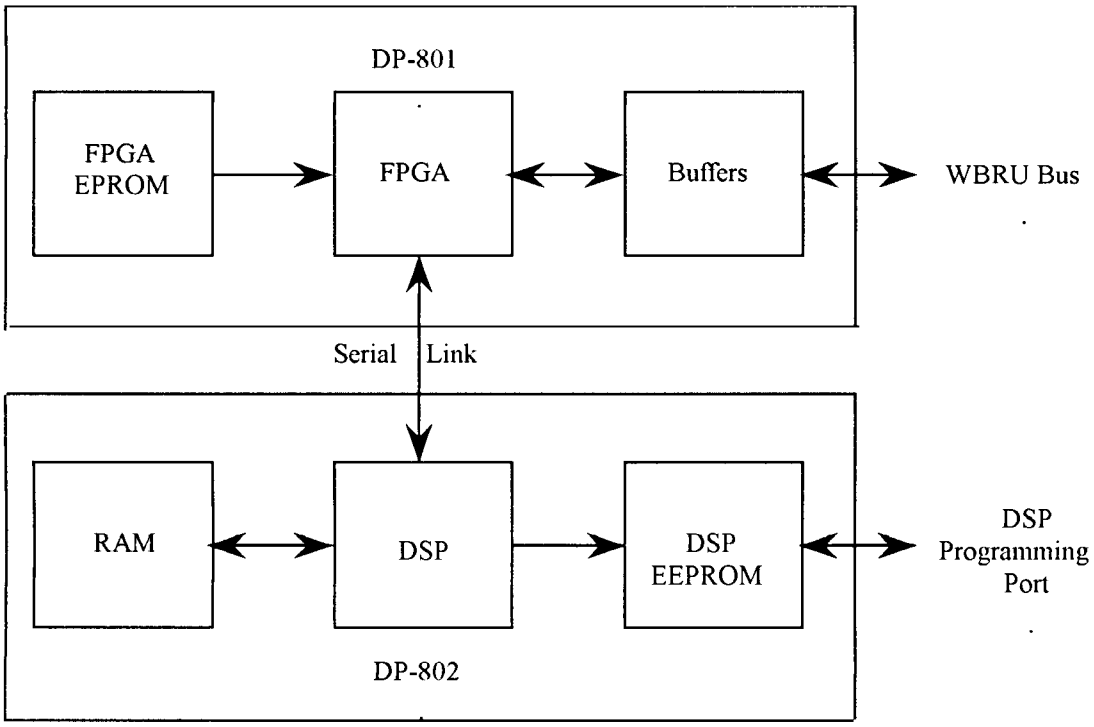

Figure 2. DP-801/802 Block Diagram

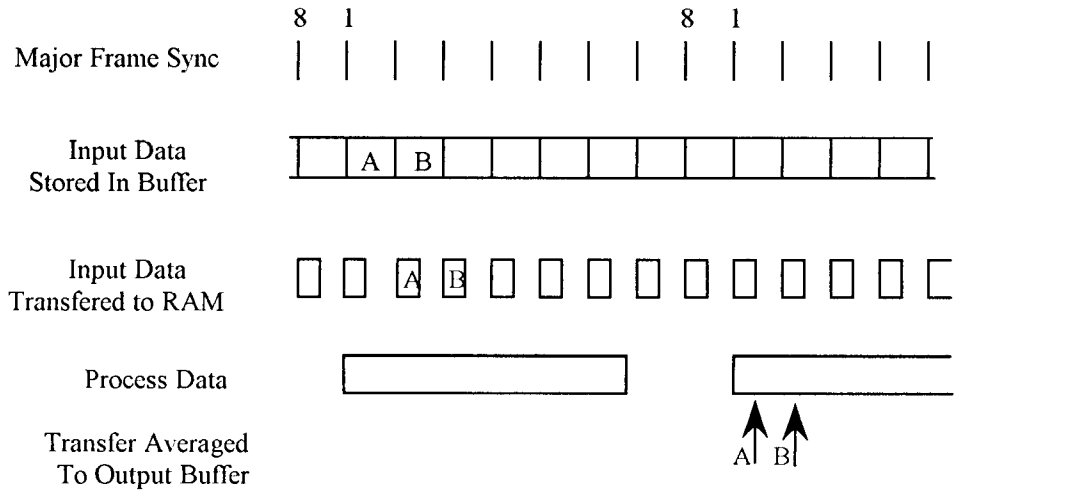

Figure 3. Timing Diagram