ACCELERATING REAL-TIME SPACE DATA PACKET PROCESSING

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ABSTRACT

NASA's use of high bandwidth packetized Consultative Committee for Space Data Systems (CCSDS) telemetry in future missions presents a great challenge to ground data system developers. These missions, including the Earth Observing System (EOS), call for high data rate interfaces and small packet sizes. Because each packet requires a similar amount of protocol processing, high data rates and small packet sizes dramatically increase the real-time workload on ground packet processing systems.

NASA's Goddard Space Flight Center has been developing packet processing subsystems for more than twelve years. Implementations of these subsystems have ranged from mini-computers to single-card VLSI multiprocessor subsystems. The latter subsystem, known as the VLSI Packet Processor, was first deployed in 1991 for use in support of the Solar Anomalous & Magnetospheric Particle Explorer (SAMPEX) mission. An upgraded version of this VMEBus card, first deployed for Space Station flight hardware verification, has demonstrated sustained throughput of up to 50 Megabits per second and 15,000 packets per second. Future space missions including EOS will require significantly higher data and packet rate performance. A new approach to packet processing is under development that will not only increase performance levels by at least a factor of six but also reduce subsystem replication costs by a factor of five. This paper will discuss the development of a next generation

packet processing subsystem and the architectural changes necessary to achieve a thirty-fold improvement in the performance/price of real-time packet processing .

KEY WORDS

CCSDS Service Processing, VLSI, multiprocessor, ASIC

INTRODUCTION

Service Processing refers to the task of extracting instrument data from a multiplexed downlink telemetry stream and formatting it in a useful fashion for scientists and other space data users. The telemetry formats defined by the following CCSDS Recommendations: CCSDS Packet Telemetry [1] and CCSDS Advanced Orbiting Systems, Networks and Data Links [2] have been adopted by NASA and its international partners for use in current and future missions, including EOS and Space Station. The flexibility and complexity contained within these standards lead to very processor intensive solutions. For real-time Service Processing, the processing load of these protocols can quickly overwhelm general purpose processors and requires a specialized architecture to support high data rates . In the past, implementations using general purpose multi-processor workstations have achieved data rates up to several Megabits per second (Mbps) and packet rates up to several thousand packets per second. A single card Service Processor Subsystem developed by the Microelectronics Systems Branch (MSB) uses a specialized architecture to achieve 50 Mbps and 15,000 packet per second [3]. To meet the high packet processing rates required by EOS, the MSB is currently developing a next generation CCSDS Service Processor based on 'system-in-a-chip' technology which will operate at 300 Mbps and 250,000 packets per second. This paper illustrates how this next generation architecture will accelerate service processing. First, we start with a brief explanation of CCSDS frame and packet formats in order to introduce some Service Processing terms . Next, the current Service Processing subsystem architecture and its limitations will be described . Finally, the next generation CCSDS Service Processing architecture and its implementation approach will be presented.

CCSDS FRAME AND PACKET FORMATS

A typical CCSDS telemetry stream consists of spacecraft data, in the form of packets, embedded in fixed length frames . A spacecraft may have multiple instruments on board, each with different sample sizes and rates . These packets may be multiplexed together into frames for transmission . In the multiplexing process, fixed length frames are built from variable length, variable rate packets . Since a perfect fit is not guaranteed, packets are often split between two or more frames . If a source generates

small packets, many of them may be contained in one frame . The Service Processing task is to reconstruct the packet data generated by each instrument and route it to the appropriate source. This task involves the identification, extraction and reconstruction of multiplexed packets from a telemetry stream . A service refers to the CCSDS AOS defined services: Insert, Virtual Channel Data Unit (VCDU), Virtual Channel Access (VCA), Bitstream, Encapsulation, Path Packet . This paper refers to the CCSDS Insert, VCDU, SLC, VCA, and Bitstream services collectively as frame services. CCSDS Encapsulation and Path Packet are referred to as packet services.

To enable packet reconstruction, identification, and delivery to the appropriate destination, five CCSDS defined fields are used: Spacecraft Identifier (SCID), Virtual Channel Identifier (VCID), First Header Pointer (FHP), Application Process Identifier (APID), and packet data length . The locations of these elements within their respective CCSDS data structures are shown in Figure 1 . The frame header field contains the SCID and VCID which determine the frame and packet level services needed on a particular frame . The FHP defines the location of the first packet header in the frame. Since packets may be split between frames, a packet piece may be in front of the first packet header in the frame data field . The APID, located in the packet header, designates which packet services are needed . The packet length field is also in the packet header and is used in conjunction with the current packet location to determine the start of the next packet . Subsequent packet headers are determined by the length and location of preceding packets.

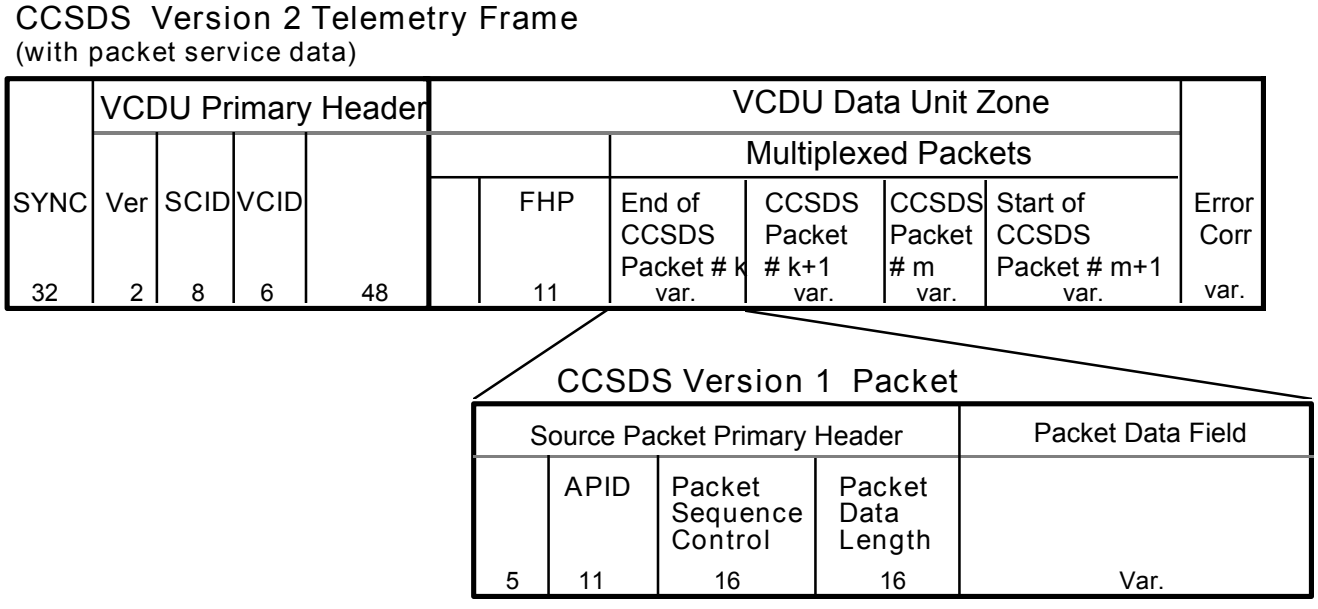

Figure 1: Version 2 CCSDS Frame and Version 1 Source Packet

THE CURRENT SERVICE PROCESSING SUBSYSTEM ARCHITECTURE

The current Service Processing Subsystem uses a combination of Very Large Scale Integration (VLSI) acceleration hardware and real-time multi-processing software to achieve high data and packet throughputs . The VLSI acceleration hardware, implemented using Application Specific Integrated Circuit (ASIC) technology, facilitates the real-time extraction and reordering of telemetry data into packet streams. Three commercial microprocessors (Motorola MC68040's) implement algorithms and generate instructions that are executed by the ASICs . The pipelined architecture, shown in Figure 2, uses two separate Random Access Memory (RAM) systems; the Tribuffer RAM and the Reassembly RAM . The programmability of the microprocessors, labeled Header Processor, Quality Processor, and Output Processor, provide flexibility for alternate data formats . Dual ported RAM devices (DPRs) provide inter-processor communication paths.

The first RAM system consists of three 4 KByte memory devices which interface with the Tribuffer Controller ASIC to triple buffer input telemetry transfer frames . Triple buffering provides a full frame period for extraction of frame and packet header data . The Header Processor configures and controls the Tribuffer Controller ASIC . Through the generation of instructions to the Tribuffer Controller ASIC, the Header Processor reads frame and packet headers . From these, it generates a piece index for each packet piece and passes the list along with location information to the Quality Processor and Output Processor. The Header Processor then instructs the Tribuffer Controller to output the frame to the second RAM system . The second RAM system contains the Reassembly RAM, 4 Megabytes of storage partitioned into 32 Virtual Channel Identifier (VCID) partitions . The Header Processor programs the RAM Controller ASIC with an offset address, based on the VCID found in the frame header . The RAM Controller ASIC uses this offset to route the frame (as it is output from the Tribuffer Controller ASIC) to the appropriate partition.

The Quality Processor performs analysis of header data to check and reassemble source packets and to generate quality and accounting information . The result is a list of packet piece indexes and annotation data which are passed to the Output Processor . The Output Processor, using Quality Processor data and packet piece locations from the Header Processor, generates instructions for the RAM Controller ASIC to output reassembled source packets with quality annotation.

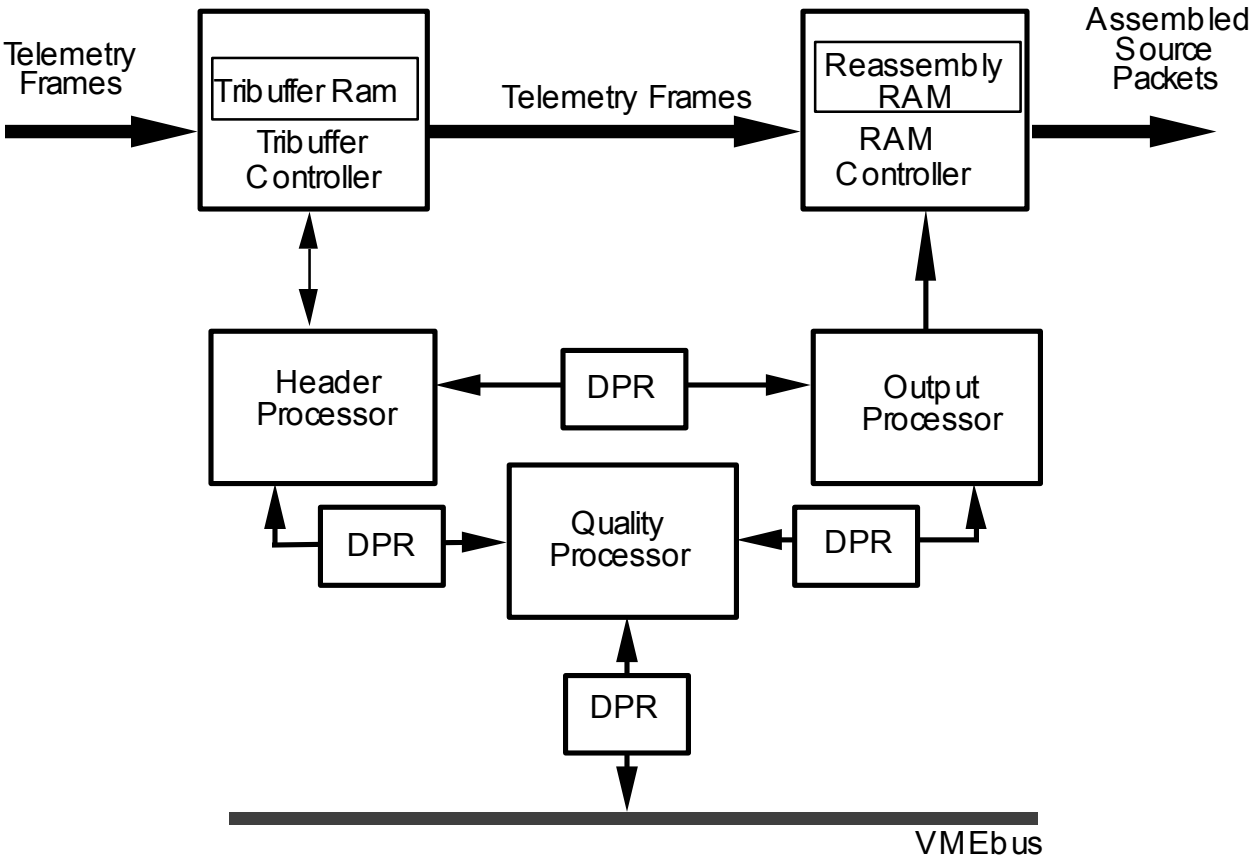

Figure 2: VMEBus Service Processor Subsystem

The software overhead involved in the current service processing implementation results in an overall pipeline bandwidth utilization of less than 32% . While the Tribuffer Controller and the RAM Controller ASICs are capable of moving data at rates up to 160 Mbps, the subsystem throughput is 50 Megabits per second . Although the pipelined, multi-processing Service Processing subsystem is significantly faster than general purpose multi-processing implementations, it can be shown that an even greater improvement in speed is possible . Algorithms currently performed in software can be implemented in hardware which will remove a significant amount of overhead and attain a bandwidth utilization approaching 100%.

CCSDS SERVICE PROCESSOR ASIC ARCHITECTURE

Due to technological breakthroughs in submicron integrated circuit manufacturing, enormous integration levels and very high speeds are attainable . The next generation CCSDS Service Processor will exploit this technology to integrate most of the functionality of the current Service Processing subsystem hardware and software into a single CMOS device . This will result in significant cost savings and greatly increased performance . The next generation Service Processor will consist of a CCSDS Service Processor ASIC, external memory, and a low-cost microprocessor to configure the ASIC and interface with other system elements . Thus, the cost for

software development and maintenance will be minimal. This device is being designed to accommodate a pipeline bandwidth in excess of 300 Mbps . With no real-time processing software required, the overall bandwidth utilization will approach 100%, attaining data rates at the full device rate and packet rates in excess of 250,000 packets per second.

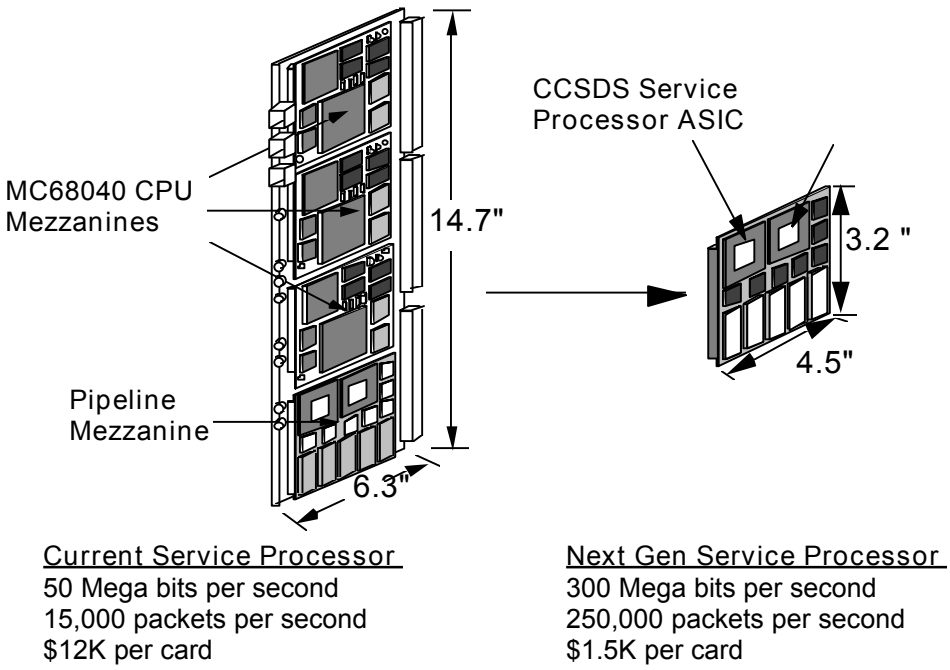

Figure 3: Current vs. Next Generation Implementation

The CCSDS Service Processor ASIC is being designed to provide a solution to space data packet processing at unprecedented levels of performance and price . The use of commercial submicron Complementary Metal Oxide Semiconductor (CMOS) technology for the Service Processor ASIC will yield very high processing clock rates . The ASIC includes embedded memory to provide quick access to data which needs frequent recall and updating and dedicated access for different processing elements to eliminate contention. Internal busses can also be sized according to processing needs; thus allowing the most efficient transfer of data between blocks .

The architecture of the next generation CCSDS Service Processor ASIC, shown in Figure 4, is constructed of a two stage pipeline consisting of frame input and frame output. In the first stage of the pipeline, the Frame Input and Autocapture Subsystem reads frames into the ASIC from an external FIFO memory and stores them temporarily in an internal pipeline FIFO memory . During frame input, all frame header and quality elements are automatically captured and stored . The Frame Quality and Lookup Subsystem checks the frame quality and 'looks up' required services based on header identifiers in an external Frame Lookup Table . The Frame Lookup Table

entry specifies which frame services to perform and if any packet services are desired . If packet services are desired, a seven bit Index is assigned via the Frame Lookup Table, thus supporting 128 Virtual Channels . Frame status information is updated in the external Frame Status Memory . Service selection and quality information is passed to the frame output stage of the pipeline and the Frame Input and Autocapture Subsystem starts reading in the next frame .

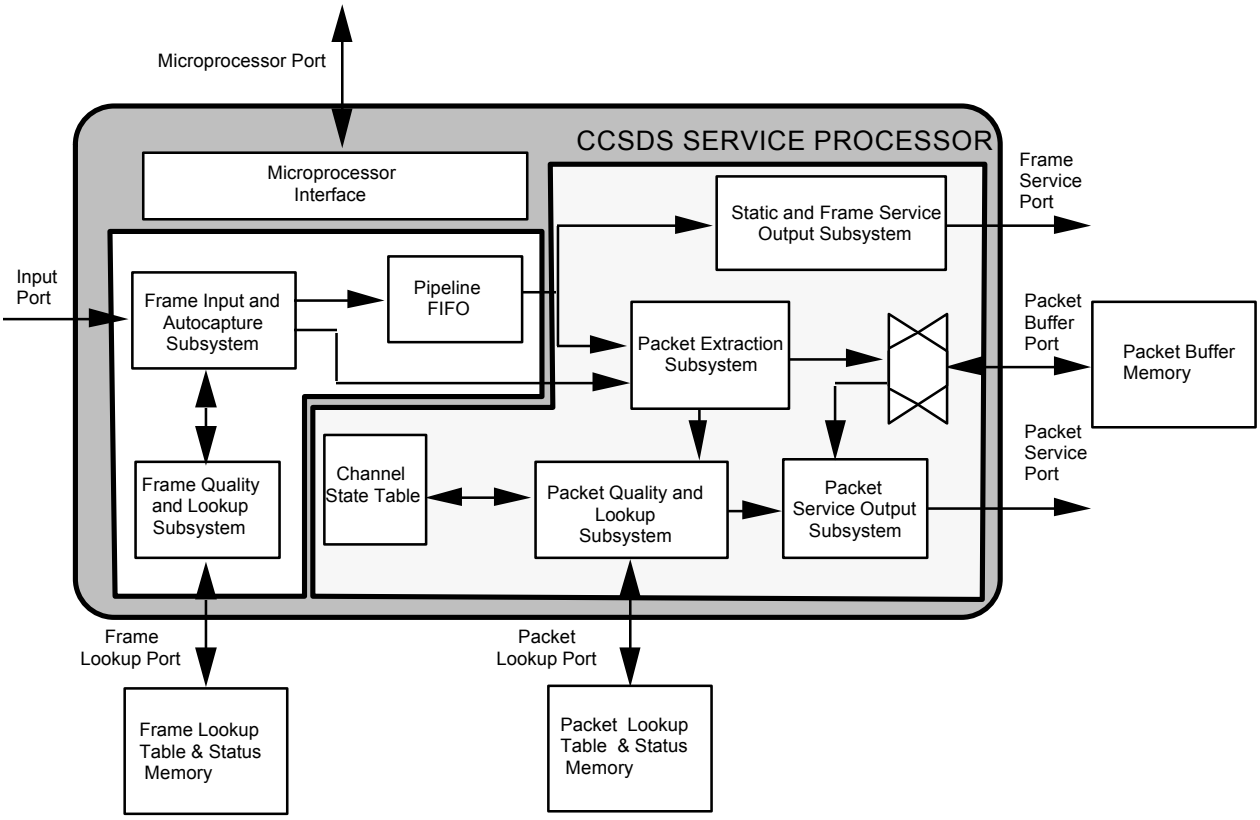

Figure 4: Next Generation CCSDS Service Processor Chip Block Diagram

The second stage of the pipeline includes frame service output, packet processing, and packet output functions. Once the frame input stage is done, the Static and Frame Service Output Subsystem pulls the frame out of the internal Pipeline FIFO and outputs the selected services through the Frame Service Port . During this time, all desired non-packet services are performed on the frame . Quality annotation may also be included with each frame .

If packet services are indicated in the Frame Lookup Table, the Packet Extraction Subsystem accepts the data while the Static and Frame Service Output Subsystem is reading the frame from the Pipeline FIFO . The Packet Extraction Subsystem extracts packet headers, determines packet boundaries, and routes packet data to the Packet Data Buffer. Boundary and header information are passed to the Packet Quality and Lookup Subsystem which analyzes extracted packet headers, marks complete packets,

and determines the status of each packet . When a packet is split across frame boundaries, the information on the packet piece is stored in the Channel State Table until the next frame on the same Virtual Channel is processed (which completes or continues the split packet.) For completed packets, the associated seven bit Index combined with the packet header APID are used to address the Packet Lookup Table . This combined field supports up to 8K sources from any of the selected 128 channels . Like the frame lookup entry, the retrieved packet lookup entry is used to determine which packet services to perform and optionally the expected packet length . The Packet Quality and Lookup Subsystem verifies packet lengths and sequence counts . The starting addresses and lengths of the reconstructed packets in the Packet Data Buffer are sent to the Packet Service Output Subsystem . The Packet Service Output Subsystem reads packets from the Packet Buffer Memory and writes them out the Packet Service Port. Quality annotation may be included with each output packet .

CONCLUSION

This paper has presented a high performance, next generation VLSI ASIC with system-in-a-chip capabilities that performs Service Processing for Advanced Orbiting System (AOS) and conventional CCSDS telemetry data streams at rates exceeding 300 Megabits per second with virtually no software overhead . The performance, integration, and cost effectiveness of this solution is expected to yield significant improvements in NASA's future data systems.

REFERENCES

1 CCSDS Packet Telemetry Standard, CCSDS 102.0-B-3, November 1992

2 CCSDS Advanced Orbiting Systems, Networks and Data Links, CCSDS 701.0-B-2, November 1992.

3 Gerald J. Grebowsky, Carol T. Dominy, "VLSI High Speed Packet Processor", Proceedings of the International Telemetering Conference, 1988.

NOMENCLATURE

AOS	Advanced Orbiting Systems
APID	Application Process Identifier
ASIC	Application Specific Integrated Circuit
CCSDS	Consultative Committee for Space Data Systems
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit

DPR	Dual Ported RAM
EOS	Earth Observation System
FIFO	First In First Out memory
Mbps	Megabits per second
MSB	Microelectronics Systems Branch
NASA	National Aeronautics and Space Administration
RAM	Random Access Memory
SAMPEX	Solar Anomalous & Magnetospheric Particle Explorer
SCID	Spacecraft Identifier
SLC	Space Link Command
VCA	Virtual Channel Access
VCDU	Virtual Channel Data Unit
VLSI	Very Large Scale Integration
VMEBus	Versa Module Eurocard bus