ADVANCED TELEMETRY PROCESSING SYSTEM (ATPS)

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ABSTRACT

The Advanced Telemetry Processing System (ATPS) is the result of a joint development project between Harris Corporation and Veda Systems, Incorporated. The mission of the development team was to produce a high-performance, cost-effective, supportable telemetry system; one that would utilize commercial-off-the-shelf (COTS) hardware and software, thereby eliminating costly customization typically required for range and telemetry applications. A critical element in the 'cost-effective, supportable' equation was the ability to easily incorporate system performance upgrades as well as future hardware and software technology advancements.

The ATPS combines advanced hardware and software technology that includes a high-speed, top-down data management environment; a mature man-machine interface; a B1-level Trusted operating system and network; and stringent real-time multiprocessing capabilities into a single, fully integrated, 'open' platform. In addition, the system incorporates a unique direct memory transfer feature that allows incoming data to pass directly into local memory space where it can be displayed and analyzed, thereby reducing I/O bottleneck and freeing processors for other specialized tasks.

KEY WORDS

B1-level Trusted operating system, commercia-off-the-shelf, real-time multiprocessing

INTRODUCTION

Telemetry processing systems must acquire and synchronize incoming data streams and provide real-time processing of critical parameters (measurands) for display and analysis, as well as support data archival of raw processed data. Today, more than ever before, telemetry processing systems must provide increased process and display capabilities to handle the increase in data rates, measurements, and quantities, while they face the added burden of meeting requirements for a secure computing environment. The ATPS meets today's telemetry processing challenges by integrating a high-performance real-time multiprocessing system, a graphical user interface-based telemetry processing software system, and a multi-level secure operating system and network product into a single box.

PRINCIPLES OF OPERATION

The ATPS design facilitates real-time data transfers that support up to 20 data streams; aggregate bandwidth of up to 20 Mbps; one or more encryption/decryption device(s); GUI and high-level software interaction displays; and a unique direct memory data transfer card. Furthermore, the ATPS hardware is equipped with fault isolation circuitry, on-line and off-line diagnostics, and data archival/playback and satellite commanding capabilities.

A basic ATPS is configured with one high-speed telemetry data bus (GME-bus), although many hardware and software configurations are possible based on user requirements. Each GME-bus is capable of accommodating 21 GME-bus devices, such as decommutators, discrete input cards, and analog to digital converters. A dual GME bus system is shown in figure 1.0.

The foundation of the ATPS consists of a modular, open hardware platform and a multiprocessor. UNIX® operating system which supports stringent real-time and multi-level secure (MLS) kernel extensions, both developed by Harris Computer Systems. Security features are actually built into the hardware, and a single chassis will implement up to four separate security levels. Therefore, ir cases where multiple telemetry streams require various levels of security, the amount of hardware required to secure the entire data stream is drastically reduced.

CX/UX™ operating system provides an I/O-intensive, deterministic computing environment ideally suited to telemetry processing applications. This industry-standard, SVID-compliant UNIX, System V Release 4, operating system is enhanced with a collection of utilities, software development tools, and real-time extensions to provide high bandwidth and true real-time processing performance in

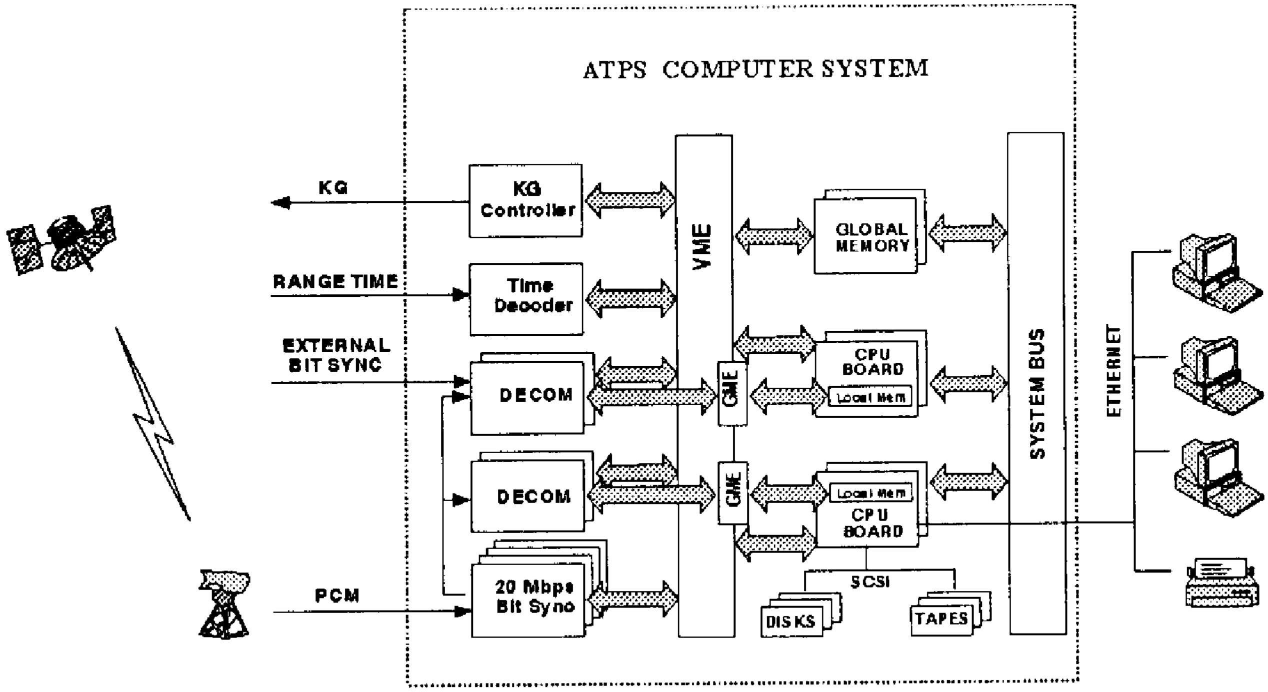


Figure 1.0

demanding development and production environments. CX/UX incorporates POSIX™-compliant features such as priority scheduling, process memory locking, memory mapping and sharing, real-time signal extensions, clocks and timers, both synchronous and asynchronous I/O.

Based on a tightly-coupled multiprocessor model, the operating system effectively eliminates the typical bottlenecks encountered with the traditional 'master-slave' model, and makes optimum use of I/O, processors, and memory resources. The operating system kernel is both multi-threaded and fully preemptive, allowing multiple processes to reside in the kernel simultaneously, while allowing higher priority processes to take precedence over lower priority processes.

An RT kernel extension is available for hard real-time processing environments where concurrent development is not required. Through the use of compile-time options, functions not critical to a stringent real-time environment have been removed or streamlined to increase the responsiveness of the operating system.

The emergence of distributed networks has led to a critical requirement for system security in today's range and telemetry programs. Typically, telemetry system users are forced to sacrifice real-time functionality, adding the burden of significantly increased overhead and multiple systems, to attain a multi-level secure computing environment. Neither tradeoff is necessary with the ATPS configured with CX/SX™, multi-level secure (MLS) operating system. Full system security is achieved at the operating system and network level with minimal real-time performance degradation, even with full system auditing activated.

CX/SX retains all of the real-time functionality of CX/UX, and provides both system and device security features such as data device labeling, mandatory and discretionary access control, multi-level directories, user and device-clearance management tools, object reuse, system audit trail, trusted path, and system assurance tools. The operating system is evaluated at the B1-level of trust by the National Computer Security Center (NCSC). To meet security requirements in secure or nor-secure distributed network and multi-vendor environments, CX/SX may be coupled with Harris' LAN/SX, providing an evaluated B1-level integrated MLS operating system and network solution.

ATPS Hardware Principles

The hardware foundation for the ATPS is the Harris Night Hawk®, a family of scalable, open architecture, industry-standard systems. The RISC-based (Reduced Instruction Set Computer) system is the ideal platform for real-time telemetry applications since it supports standard operating systems and languages as well as COTS hardware, software and peripherals; provides portability to fail-over platforms and multi-channel interconnect allowing separate processors performing different tasks to talk to each other; and requires a smaller footprint, thereby reducing overall operations and maintenance costs.

Current Night Hawk systems incorporate MC88100™ and MC88110™ chip technology and are 88open™-compliant, while future generations will incorporate PowerPC® and support the PowerOpen™ software environment. The Night Hawk's unique Pre-Planned Product Improvement design enables easy upgrade from one generation of system to another.

Night Hawk supports standard interfaces and protocols including Ethernet®, TCP/IP, FDDI, POSIX, SVID, X Window System™, OSF/Motif™, as well as ANSI-standard compilers and SCSI peripherals. The goal of this standards-based system approach is to ensure that all application and runtime code developed on any Night Hawk platform will be portable to other standards-based systems.

To achieve true linearity and boost performance, the Night Hawk employs up to eight CPUs in a dual-bus architecture. This architectural scheme provides a deterministic, multitasking environment and increased throughput that support concurrent multiple task executions and data paths, preemptive task scheduling, distributed interrupts, rapid context switches, and yields low interrupt latencies. Shielded CPUs, another plus for the multiprocessor environment, lets users direct all interrupts to a single CPU, allowing other processors to handle tasks requiring maximum determinism.

Since local memory accesses are faster and consume significantly less bandwidth than global memory, the Night Hawk installs local memory directly on the processor boards; each processor pair shares local memory. This unique memory hierarchy contributes to achieving linearity when adding processors, and allows CPU-to-CPU or CPU-to-global memory accesses without bandwidth consumption. In addition, this scheme contributes to the Pre-Planned Product improvement, which enables easy system upgrades and technology insertions through a simple CPU and memory board replacement method. A typical Night Hawk system configuration is shown in figure 2.0

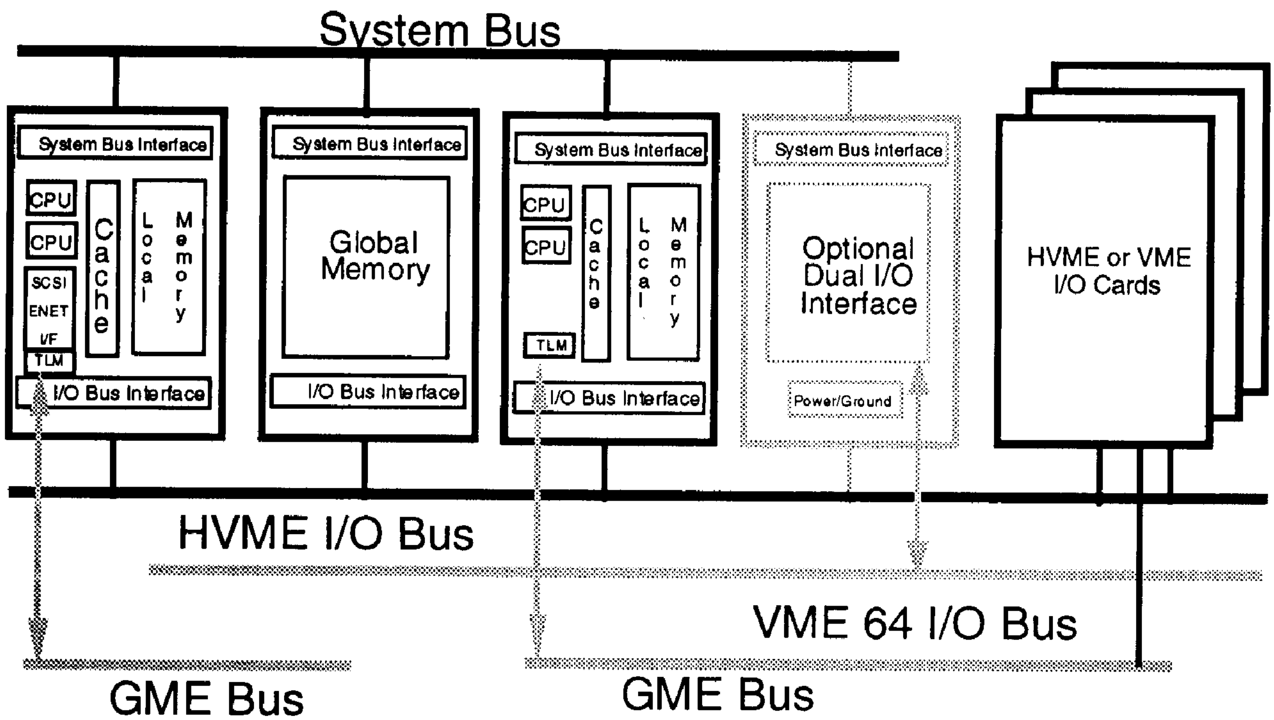


Figure 2.0

The ATPS utilizes the Night Hawk's unique memory architecture to support the Telemetry Local Memory (TLM) card, developed by Harris specifically for the ATPS. The TLM card is mounted on the CPU board, and allows data to pass directly to the processor, thereby eliminating the performance delays and processor waste typically encountered when transferring data over the VME-bus.

Since many range and telemetry applications include an Ada language requirement, the ATPS uses the Harris Ada Programming Support Environment (HAPSE™), an integrated set of software tools for the development of large-scale, real-time Ada software. One such tool is the Ada Real-time Multiprocessor System (ARMS™), an

Ada executive designed for critical real-time tasking applications. ARMS provides a real-time multiprocessor/parallel execution environment, whereby all tasks are implemented as individual threads of execution (executing on different processors) sharing a common physical memory image. The result is true concurrence among tasks. Powerful graphics capabilities are available to Ada designers through AXI™, an interface to the X Window System and Motif™ graphical user interface (GUI).

ATPS Software Principles

Today's telemetry systems must accommodate frequently changing telemetry formats and processing requirements. To meet this challenge, the APTS system uses a mature GUI software package developed by Veda Systems, Incorporated.

Veda's ITAS OMEGA™ setup and control software is a third generation, telemetry-specific environment that provides complete setup, control, data processing, display, and command processing. A central dispatcher module controls the activation of specific task modules based upon the user's request. The task modules are small, easily maintained, and provide specific functions to meet various telemetry processing requirements.

The OMEGA system software features a top-down environment for describing the characteristics of data streams and for parameter processing. Features such as project, stream, parameter, and list editors simplify these processes. In this multi-stream system, multiple bit synchronizer and decommutator pairs are supported, while the processing and associated measurements reside in a single format-parameter-list database. Here, the entire project is treated as a whole rather than creating mini-databases for each processing unit, as is typical with traditional telemetry systems. Many projects can be active in the network simultaneously. For example, one engineer may be analyzing and testing archived data; another may be acquiring and analyzing incoming real-time data; while yet another engineer is planning and designing a new mission.

The parameter database is the heart of the OMEGA system, as shown in figure 3.0 Since all parameters from all input streams are defined in this single database, configuration management of the project is significantly enhanced. In addition, the system offers a GUI-based parameter database editor, specifically designed for real-time telemetry applications OMEGA also offers integrated ANSI Structured Query Language (SQL) database tools to maximize the open systems benefit. Two levels of data display capability are available. A wide selection of optimized, standard X Window System-based display types for real-time environments and DataViews® for

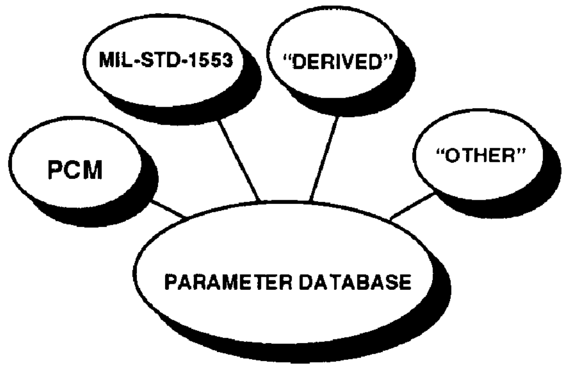


Figure 3.0

custom 2-D drawing environments. Unlike other systems that force the user to enter a display builder editor each time a new display is desired, the OMEGA system provides a unique parameter list approach which lets the user direct a parameter list to display type in real-time. This approach enhances the user's ability to respond rapidly to changing data display requirements during test operation.

A key design feature is the list-based architecture, as shown in figure 4.0, where lists are layered to allow simple access to specified data elements or groups. A complete,

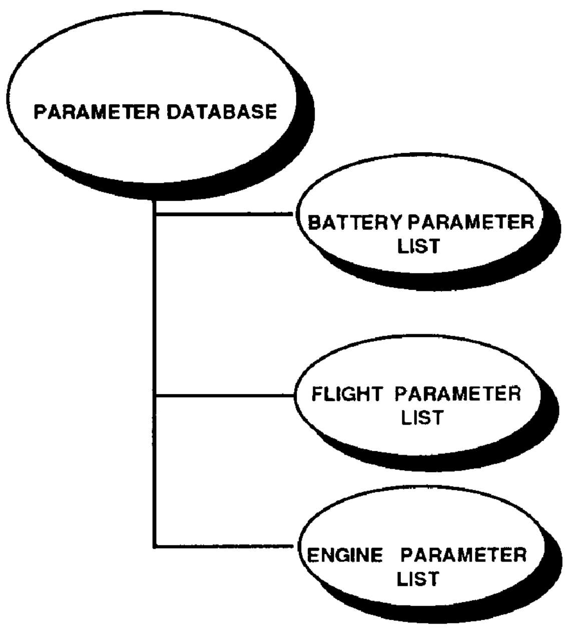


Figure 4.0

graphically-oriented list editor adds increased system flexibility by enabling editing during runtime, retrieval during runtime, and easy test preparation. For example, a structural engineer, test director, and safety officer, each focused on different test scenarios, can develop separate data lists containing only the parameters that correlate to their individual areas of interest. This capability is extremely effective since global lists typically become quite large, often containing 20,000 or more entries in a single flat file, making it difficult to locate a particular parameter. The list-based technique can also be used to limit bandwidth to selected devices by creating sublists for specific archive, processing and display duties, and by enabling manipulation of the list as a single unit.

Derived parameter processing is a critical element in telemetry applications since standard computed measurement units are often inadequate. The OMEGA system provides multiple levels of derived parameter processing capability. Here, the processing of real-time derived parameter data and external system commanding is accomplished in three distinct levels: operation, system, and application. Each provides an increased level of sophistication, flexibility, and direct data-driven CX/UX operating system connectivity.

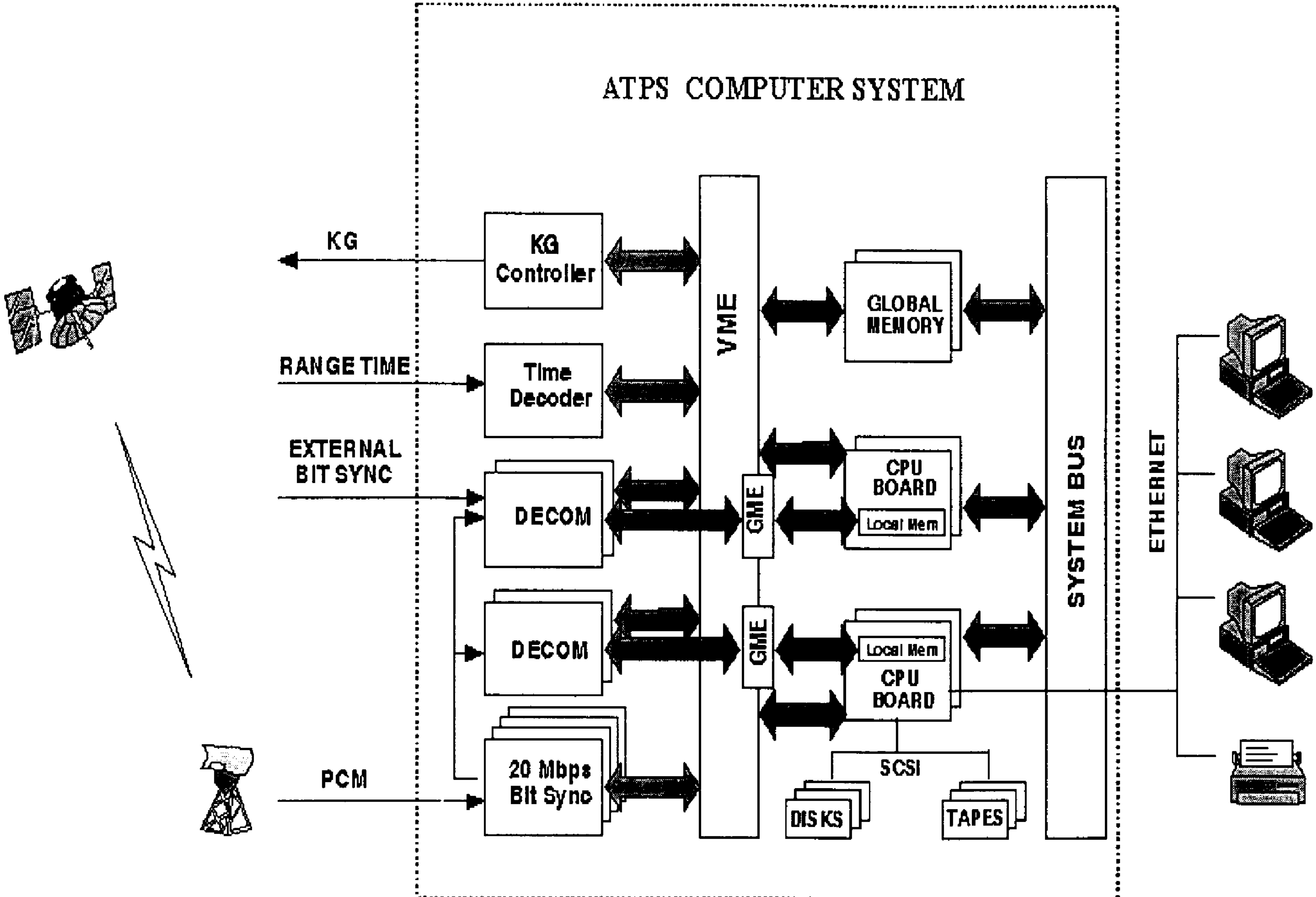
Other traditional telemetry processing software features include task dispatcher, process control and data processing mechanisms, optimized LAN management implementations, and archiving options.

SUMMARY

The unique ATPS architecture is designed to accommodate system upgrades and technology insertions though the replacement of existing processor boards with new boards, while retaining the rest of the system. All investment in software, system packaging, and peripherals is preserved. With the ATPS system, engineers need only redesign the interface card when incorporating advanced technology rather than reinvent the entire system from the CPU on up. The standards-based system supports COTS software and enables easy porting of existing code instead of necessitating the costly design, and subsequent redesign, of software.

The integrated ATPS provides the best-value solution for today's range and telemetry processing applications. The benefits of the ATPS architecture are significant in terms of ease of growth, life-cycle savings, reliability, and maintainability. Telemetry processing environments can now utilize a single box where, previously, multiple cumbersome platforms were required Open, standards-based architecture assures COTS supportability and system interoperability in multi-vendor environments, and generally attracts a large pool of users already familiar with system features, thereby reducing training efforts.

The ATPS represents a new approach to telemetry data acquisition, processing, and analysis. By incorporating a core telemetry processing software system that easily moves across scalable hardware processor platforms, the ATPS effectively protects the customer's investment. As the bandwidth and practicality of fiber-based information networks increases, along with workstation processing performance, the ATPS will continue to provide an effective bridge between front-end, processor-intensive systems and distributed workstations.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RANGE TIME
EXTERNAL
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PCM
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Controller
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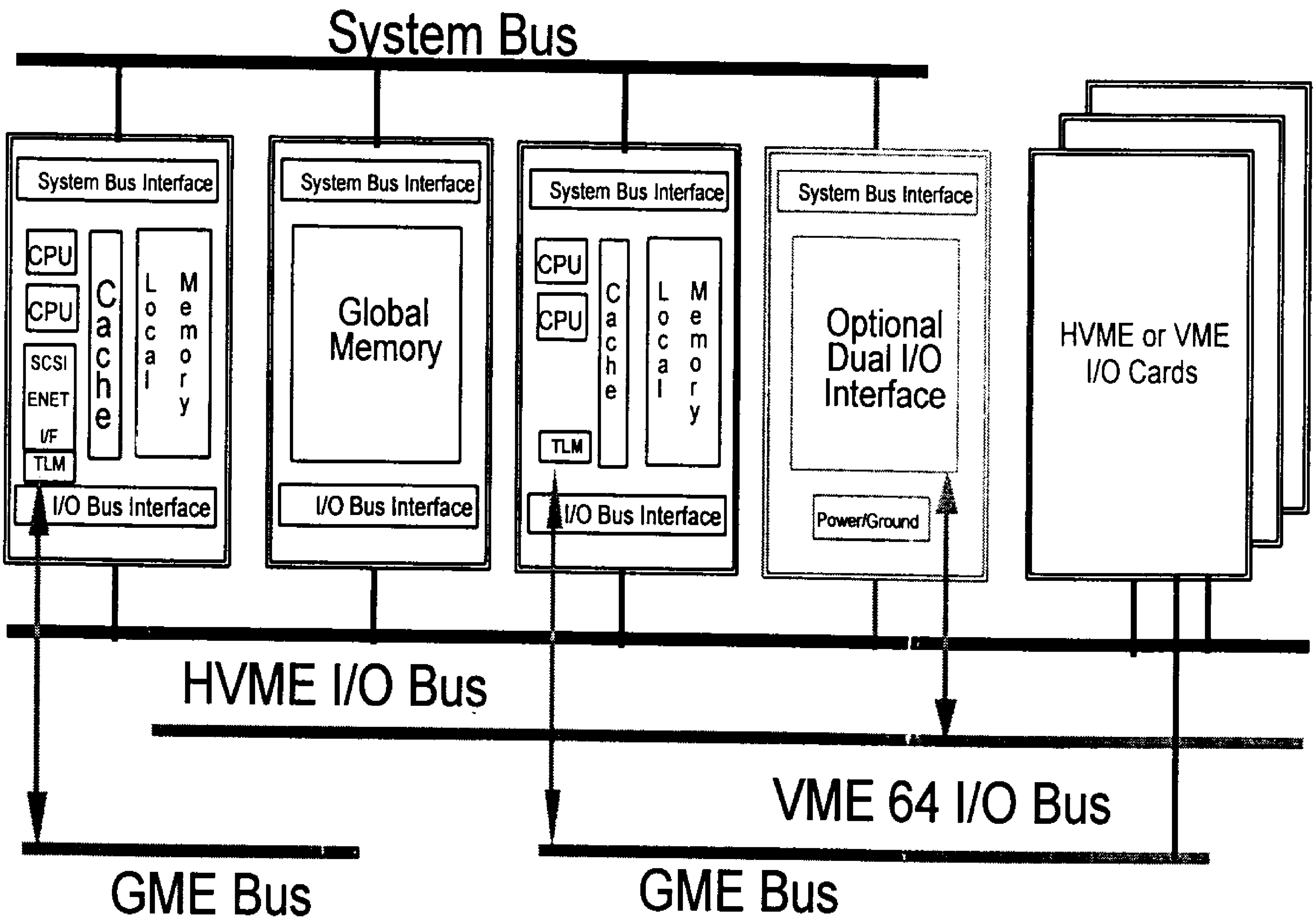
System Bus
System Bus Interface
CPU
CPU
SCSI
ENET
I/F
TLM
Cache
Local
Memory
I/O Bus Interface
System Bus Interface
Global
Memory
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System Bus Interface
CPU
CPU
TLM
Cache
Local
Memory
I/O Bus Interface
System Bus Interface
Optional
Dual I/O
Interface
Power/Ground
HVME or VME
I/O Cards
HVME I/O Bus
VME 64 I/O Bus
GME Bus
GME Bus