A HIGH SPEED REAL TIME SPACE QUALIFIED TIME DIVISION MULTIPLEXED DATA FORMATTER

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ABSTRACT

A system to generate a contiguous high speed time division multiplexed (TDM) spacecraft downlink data stream has been developed. The 25 MBPS downlink data stream contains high rate real time imager data, intermediate rate subsystem processor data, and low rate spacecraft housekeeping data. Imager data is transferred directly into the appropriate TDM downlink data window using control signals and clocks generated in the central data formatter and distributed to the data sources. Cable and electronics delays inherent in this process can amount to several clock periods, while the uncertainty and variations in those delays (e.g. temperature effects) can exceed the clock period. Unique (patent pending) electronic circuitry has been included in the data formatter to sense the total data gathering delay for each high speed data source and use the results to control series programmable delay elements to equalize the delays from all sources and permit the formation of a contiguous output data stream.

KEYWORDS

Space Qualified Data Formatter, Propagation Delay Compensation, High Speed Data Formatter, Telemetry Processor.

INTRODUCTION

The Midcourse Space Experiment (MSX) Program is being conducted by The Johns Hopkins University/Applied Physics Laboratory (JHU/APL) for the Ballistic Missile Defense Organization (BMDO). MSX will be a data collection experiment, concentrating on the phenomenology of target detection and tracking and the gathering of celestial and earth limb background data.

The MSX spacecraft instrumentation includes a Space Infrared Imaging Telescope (SPIRIT III) provided by Space Dynamics Laboratory/Utah State University (SDL/USU), an Ultraviolet and Visible Imagers and Spectrographic Imagers (UVISI) instrument provided by JHU/APL, and a Space Based Visible (SBV) instrument and several Reference Objects provided by MIT Lincoln Laboratory (MIT/LL). An Onboard Signal and Data Processor (OSDP) experiment, developed by BMDO and provided by Hughes Aircraft Company, will also be flown as a demonstration of real time onboard processing and orbital radiation effects. The MSX spacecraft includes an X-Band transmitter for downlinking SPIRIT III, UVISI, and SBV Imager data as well as an S-Band (SGLS) transponder.

The MSX Data Handling System (DHS) gathers, formats, and outputs real time science and housekeeping data to generate three output data streams:

(1) A 25 MBPS (or 5MBPS) prime science data stream containing imager, processor, and housekeeping data which is transmitted in real time or stored on the spacecraft tape recorder and downlinked over the X-Band link.
(2) A MBPS wideband downlink data stream containing snapshot imager data and housekeeping data which is transmitted in real time over the S-Band link.
(3) A 16KBPS narrowband downlink data stream containing spacecraft housekeeping data and/or processor memory dump data which is transmitted in real time over the S-Band link.

The DHS provides four selectable prime science data formats (one 25 MBPS format and three 5MBPS formats), three selectable wideband data formats, and ten selectable narrowband data formats. The prime science, wideband, and narrowband data formatters are independently controlled, and all three may be operated simultaneously.

The DHS also performs several critical spacecraft functions including maintaining and distributing mission elapsed time (MET) and universal time (UT), recording and downlinking selected critical spacecraft housekeeping data, and providing spacecraft fault protection and autonomous control via a dedicated link to the MSX command system. The DHS consists of the data formatters with associated interface electronics, a housekeeping data gathering subsystem, clock generation/timing chain electronics, and a microcomputer to process commands and keep mission time (see Figure 1).

The prime science formatter processes real time high rate data from the SPIRIT III instrument, the UVISI instrument, and the SBV instrument. It also processes data which was previously transferred to and stored in the DHS from the attitude and tracking processors, contamination experiments, OSDP, and interferometer as well as data (sync word, frame count, etc.) which originated within the data handling system.

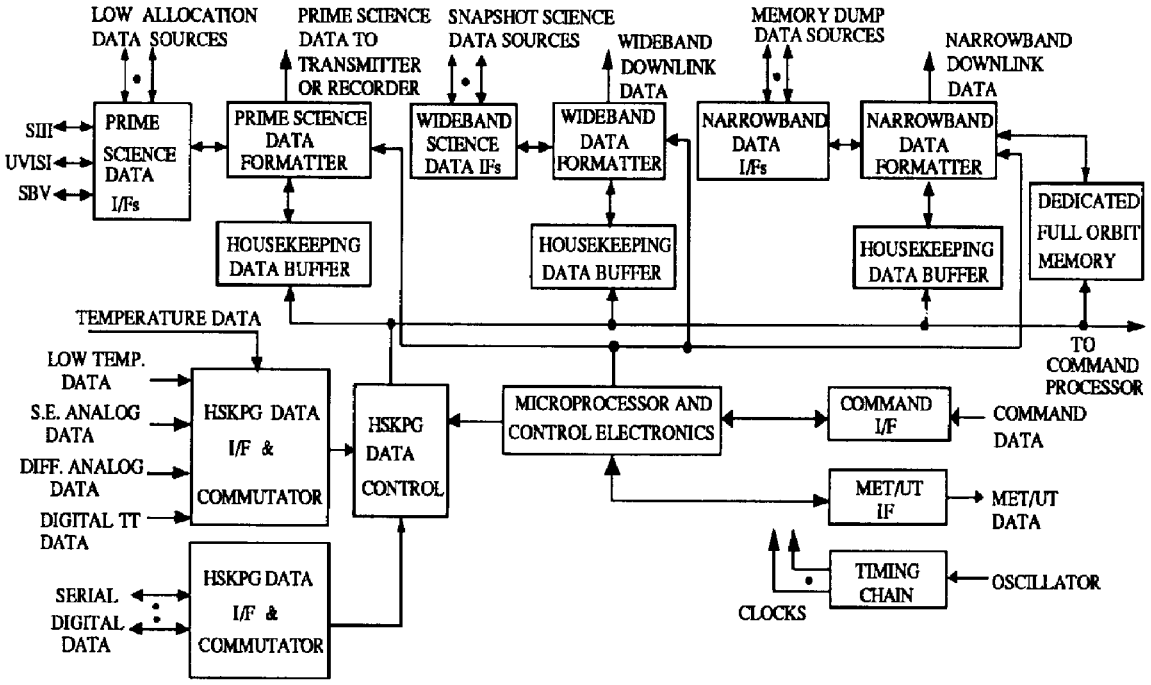

Figure 1. MSX Data Handling System

The formatter multiplexes the data from the various data sources into a single data stream at the output bit rate in the selected science output format (see Figure 2).

32	48	96	160	512	704	928	1536	17792	64368	69424	69440
SYNC	ID. & FRM. CNT	HSKP DATA	TRAKG. PROC. DATA	ATTIT POINT. DATA	CONTAMIN. EXPT. DATA	OSDP DATA	INTERF. EXPT. DATA	UVISI EXPT. DATA	SPIRIT III RADIOMETER INST. DATA	SBV EXPT. DATA	*
32 B	16 B	48 B	64 B	352 B	192 B	224 B	608 B	16,256 B	46,576 B	5,056 B	

1) FREQUENCY = 25 MBPS
2) 360 MINOR FRAMES/MAJOR FRAME
3) MAJOR FRAME = 1 SEC.
4) * ≡ UNDEFINED

Figure 2. MSX X-Band Prime Science Minor Frame Data Format (High Rate Mode)

Frame markers, read out gate signals, and clocks used to gather and format the high speed data are generated in the data system and distributed to the data sources. Variations in the cable, driver, receiver, and data source logic gate propagation delays in the processing of these signals preclude formation of a contiguous output data stream without compensating for these effects. The prime science formatter senses the total data gathering delay for each high speed data source and uses the result to control series programmable delay elements to equalize the delays from all sources and permit formation of a contiguous data output.

PRIME SCIENCE FORMATTER

Prime science format selection is accomplished when a command message is received via the MSX command processor and the DHS microcomputer electronics. In each prime science format, a minor frame contains information from each of the imagers, experiments, and onboard processors in addition to a partial housekeeping data set (see Figure 2). Each major frame of data consists of 360 minor data frames and contains one complete housekeeping record. Format and rate selection transitions occur only at major frame boundaries upon generation of a major frame pulse. The prime science formatter determines the output data rate (25 MBPS or 5MBPS) from the format selection command.

Prime science formats are programmed in radiation hardened PROM memory, which is read at intervals determined by the PROM code itself (see Figure 3). PROM address information is derived from a counter which is the final stage of a bit rate counting chain, which consists of a sixteen bit word boundary counter, a programmable word counter, and the PROM address counter. PROM output data contains the identity of the selected TDM downlink data source in addition to the programmable word count which represents the data source bit allocation. Since radiation hardened PROM access times (~120 nS) are long compared to the high rate bit period (40 nS), it was necessary to configure the PROM code to identify data source transition word boundaries one word prior to the actual data source transition and to specify the data source to be selected at the following word boundary. Similarly, the hardware is designed to process the PROM data during the sixteen bit word cycle prior to a data source transition, and to change the data source at the next word boundary.

The prime science formatter contains a dedicated housekeeping FIFO memory which is loaded with a new complete housekeeping data set every second by the DHS housekeeping data gathering subsystem, and read out by the formatter electronics. The housekeeping data memory consists of ping pong FIFOs, with the housekeeping data gathering subsystem loading one FIFO while the formatter reads the previously loaded alternate FIFO. Each major frame pulse switches the FIFO selection, with the result that all MSX downlink data frames contain all housekeeping data gathered during the second prior to the major frame pulse. A hardware frame counter keeps the minor frame count and inserts it into the downlink data stream each minor.

In addition to real time imager data, the prime science formatter processes low rate data from seven data sources including the onboard licking and attitude processors, the contamination experiments, the OSDP electronics, and the interferometer instrument. Since the bit allocation for each source is relatively small, data transfers between the low rate sources and the prime science formatter are accomplished using a low speed

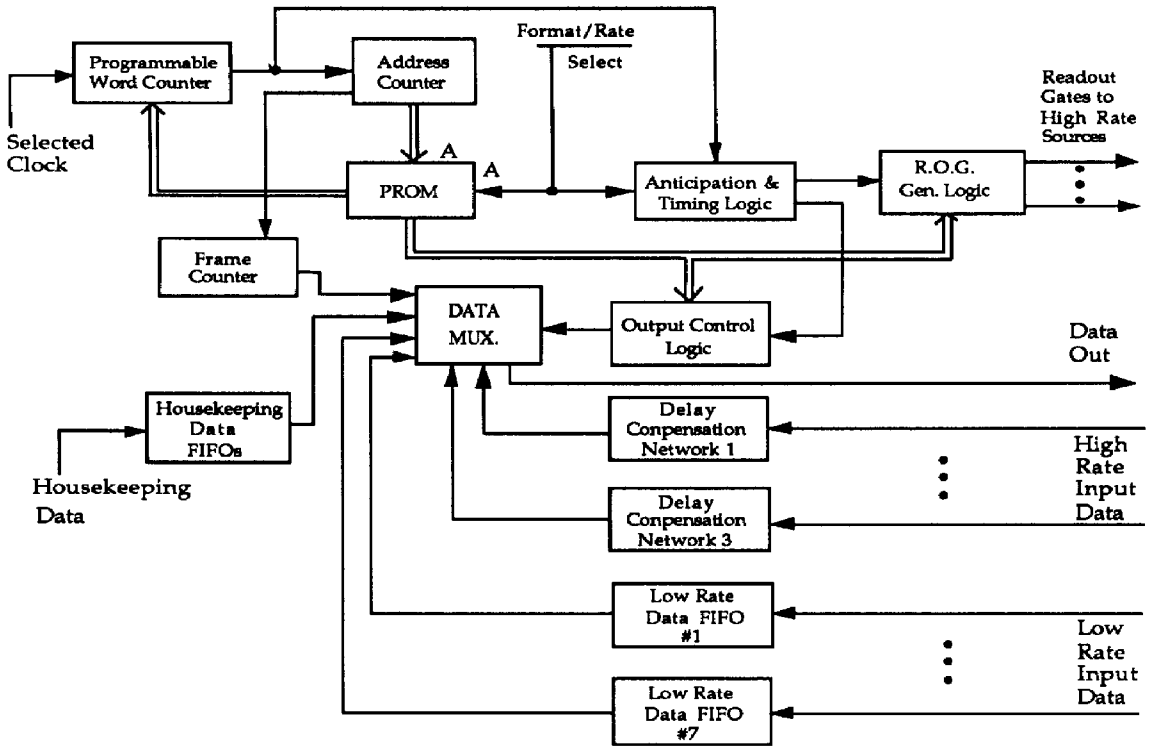

Figure 3. MSX Prime Science Data Formatter

RS 422 interface with an RC termination network. This interface permits the low rate instruments to be designed without the high speed, high power, ECL interface electronics required for imager data transfers. The prime science formatter distributes major frame and half minor frame markers to each low rate data source, with data transfers consisting of data source generated clock, data, and enable signals occurring during the second half of each minor frame. The transferred data is loaded into dedicated FIFO memory in the DHS prime science formatter using the data source generated transfer clock of MBPS. It is then read out from the FIFO memory by the prime science formatter at the output bit rate (25 MBPS or 5 BPS) during the appropriate data window in the first part of the next minor frame. Radiation hardened high speed "serial in-serial out" FIFO memories and output level shifters are used for this application. Unlike the interfaces with the low rate data sources, output data from the three onboard imagers is not buffered, but is read out in real time and placed directly into the appropriate downlink data stream window. Data transfers from the imagers to the DHS prime science formatter are controlled by the formatter, which generates frame pulses, read out gates, and read out clock signals to each of the imagers. Output data is internally loaded by each imager data source on receipt of a minor frame pulse, and read out serially by the prime science formatter. The imager output electronics shifts output data bits on the falling edge of the clock from the prime science formatter while data bits are latched in the formatter electronics on the

rising edge. Read out gate (ROG) transitions occur during the negative phase of the data transfer clock.

Prime science data transfer electronics for all signals between the prime science formatter and the imager electronics consists of an MC10501 emitter coupled logic (10K ECL) driver element and an MC10515 (10K ECL) receiver element connected by 77 ohm twinax cable. Resistors and diodes are included in the interface design to, among other things, match the cable impedance and provide for a proper voltage at the receiver when the driver is unpowered.

TABLE 1. PRIME SCIENCE FORMATTER PATH DELAYS

	MIN (NS)	MAX (NS)
Central Data System Clock Output Driver	1.0	3.3
3' – 15' Twinax Cable	4.9	24.3
Instrument Total Delay – (Clock ↓ to Data Valid)	12.0	35.0 *
3' – 15' Twinax Cable	4.9	24.3
Central Data System Data Receiver	1.0	3.7
[Programmable Delay Unit Inherent Delay]	[8.0 **	15.0 **]
Central Data System Data Multiplexer	1.5	5.3
Central Data System Latch Setup Time	0.0	2.5
	33.3 NS	113.4 NS

* Specified, ** 25 MBPS only

Distances between the MSX DHS formatter electronics and the imager output electronics range from approximately three feet to approximately fifteen feet. Expected cable propagation delays as well as electronics delays for data transfers between the imagers and the prime science formatter are summarized in Table 1. The total path delay represents the time between a selected imager clock edge and the appearance of valid data at the input to the DHS prime science formatter. The difference between minimum and maximum electronics delays is primarily due to fabrication process effects (i.e. part to part variations) and temperature effects, while the cable propagation uncertainty is primarily due to package location and cable routing.

The maximum total path delay for data from each of the three imagers of 113.4 nS and the uncertainty in the path delay of 80.1 nS preclude formation of a contiguous 25 MBPS output data stream. Shifting serial imager data on one clock edge and reading the data into the prime science formatter on the following clock edge would require a

maximum data valid path delay of one-half bit period (20 nS) from each imager, while the actual delay from any imager data source can be anywhere from 33.3 nS to 113.4 nS. A delay compensation mechanism to equalize the delays for all prime science formatter data sources was introduced to overcome this problem and permit formation of the 25 MBPS output.

PROPAGATION DELAY COMPENSATION

The prime science formatter implements imager data delay compensation by transitioning imager data source ROG signals three clock cycles early and adding a compensating delay to the returned imager data such that the first transition of the compensated data occurs precisely where it would have occurred if no ROG anticipation had been implemented and the ideal zero propagation delay data path existed. The three imager data sources preface each minor frame data transfers with a fixed pattern of 7F or 7FFF which is used by the formatter to identify the first data transition. Delay compensation is only implemented in the 25 MBPS prime science mode. The programmable delay element used in the compensation electronics is bypassed in the 5 MBPS mode.

Operation of the delay compensation electronics is illustrated in Figure 4 where the desired position of imager data in the composite formatted downlink data stream and the relative phasing of an imager ROG signal are shown on lines 2 and 3, respectively. Note that the imager data source outputs its first data bit (B_0) on the minor frame pulse and shifts its data on negative clock edges once it receives an active ROG signal. The data received by the prime science formatter for the ideal zero delay condition and for a typical propagation delay condition are shown on lines 4 and 5, respectively. Since the first eight bits are defined as a synchronization header (7F), the B_0 B_1 transition shown on line 5 is defined as a change from an extended low data condition to a long ($\geq$7 bits) string of high data. The prime science formatter implements closed loop phase control to add a complementary delay to the delay contained in the waveform on line 5 to locate the B_0-B_1 data transition in the appropriate position, (line 6), for data system sampling (line 8). The total propagation delay (i.e. the time from the B_0-B_1 data transition on line 4 to the B_0-B_1 data transition on line 6) now consists of the inherent propagation path delay plus the imparted delay from the delay compensation network. The three clock cycle, (120 nS), total delay was selected since it exceeded the worst case maximum inherent propagation delay (113.4 nS) and thus insured a positive value for the imparted delay.

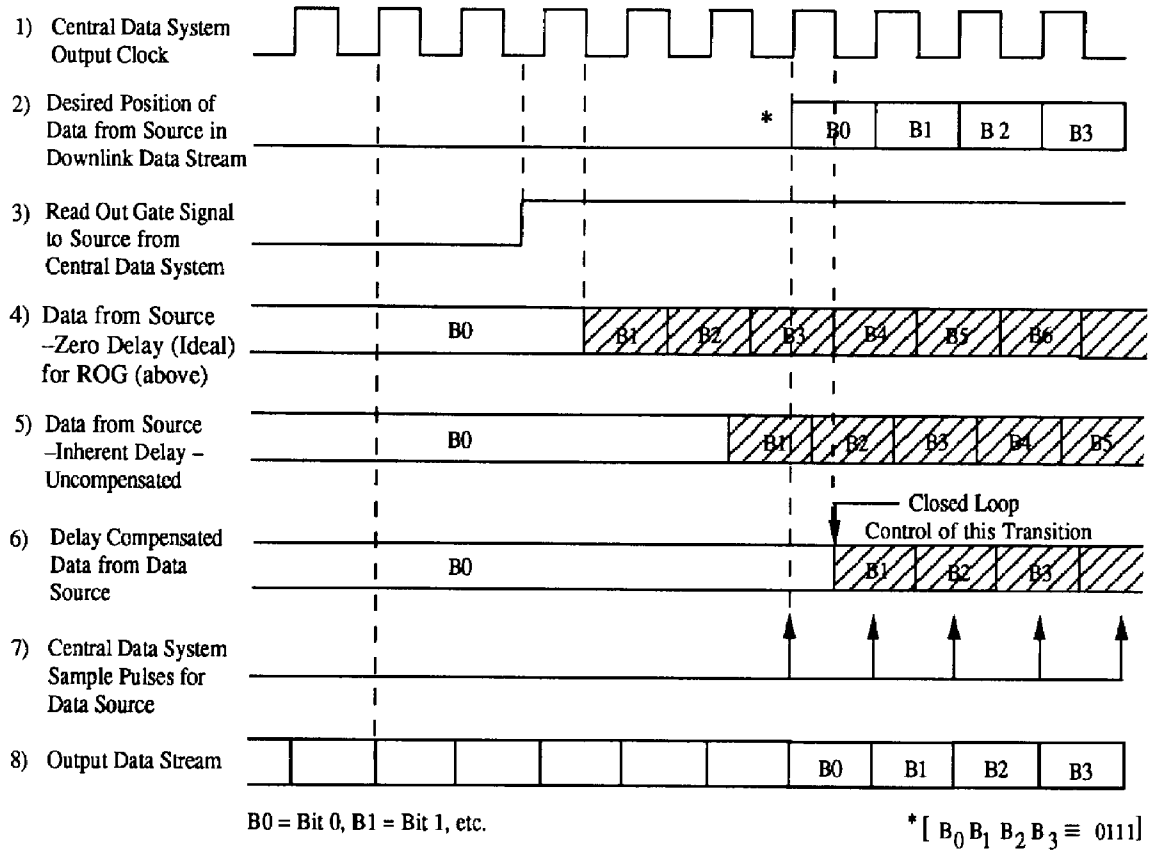

Figure 4. Delay Compensation Timing for One Data Source

In Figure 5 the delay compensation network consists of a programmable delay unit, an up-down control counter, phase detector electronics, and electronics to generate a phase detector sample pulse at the desired B_0-B_1 transition time (line 6, Figure 4). All delay compensation network electronics is implemented with 10K ECL components operating at -5.2 VDC. The programmable delay unit imparts a delay between zero and 120 nS (in 8 nS steps) to the imager data depending on the current state of the control counter. The control counter is adjusted one count each minor frame based on the results of the phase comparison performed during the previous minor frame.

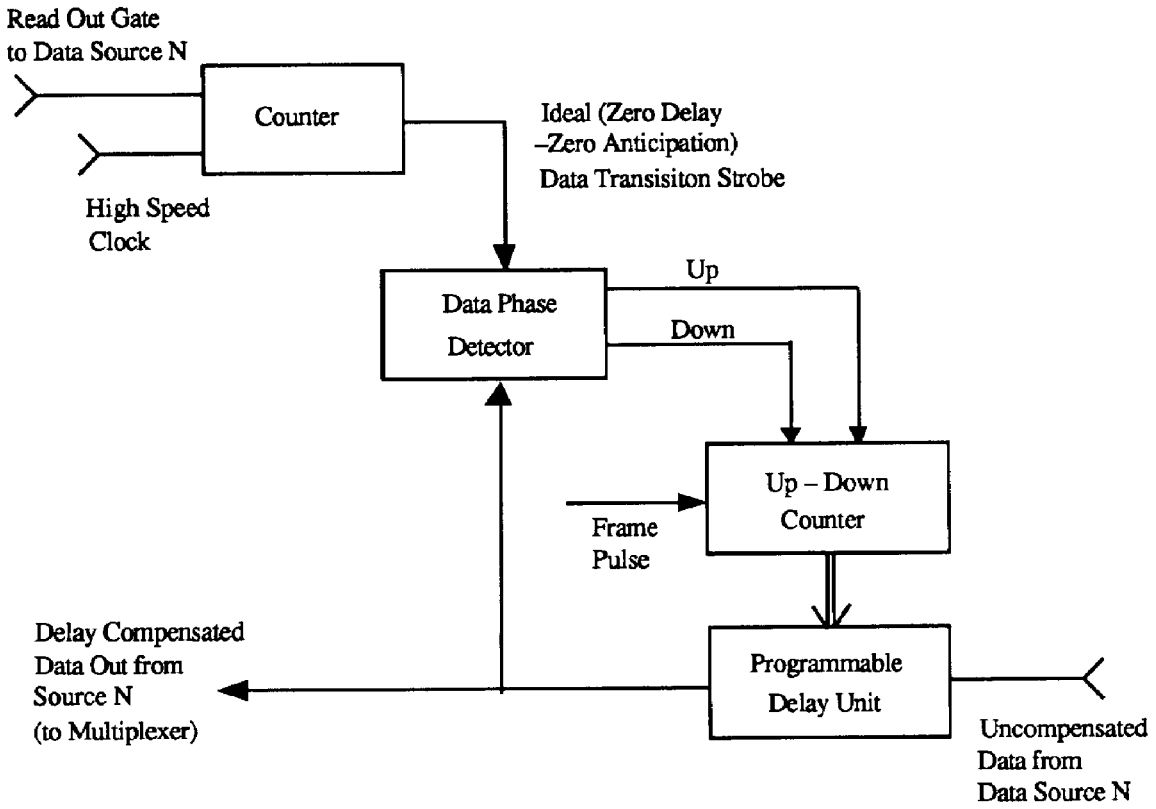

Figure 5. High Rate Data Delay Compensation Network

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