HSTSS-DAC CUSTOM INTEGRATED CIRCUITS FOR SUBMINIATURE PCM TELEMETRY AND SIGNAL CONDITIONING

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ABSTRACT

To meet specific test and evaluation requirements, the Hardened Subminiature Telemetry and Sensor Systems (HSTSS) program is addressing the miniaturization and 'G' hardening of telemetry components. Two custom Integrated Circuits (ICs) are in development to support the design of miniature Pulse Code Modulation (PCM) systems with up to 128 analog input channels. This paper describes the design and development of the custom IC chips of the HSTSS Data Acquisition Chipset (DAC). The original requirements, the roll of the Integrated Product Team (IPT), design decisions, a discussion of the additional features, and practical limitations of the Data Acquisition Chipset will be covered.

KEY WORDS

IRIG-106 PCM, Custom Integrated Circuit, Signal Conditioner, Integrated Product Team (IPT).

INTRODUCTION

A severe problem in the testing and evaluation of projectiles and missiles is the lack of volume available for on-board telemetry instrumentation. Telemetry is sometimes an afterthought in the system design or is utilized as a tool if failures are encountered after limited initial production has started. The HSTSS project has chosen to address the volume limitation issue by developing miniaturized telemetry building blocks. In particular the project has initiated the design and development of a Data Acquisition Chipset (DAC). The DAC is a set of custom integrated circuits (ICs) which will be used to support the flexible design of telemetry instrumentation compatible with IRIG-106 standards.

The original specifications outlined a four-channel PCM DAC [1] with a fixed frame format and word size and a 64-channel PCM DAC [2] with a programmable frame format and fixed word size. These were to be the initial building blocks for the HSTSS PCM systems. The two specifications were mutually exclusive, but the actual intent was to arrive at a single chip set solution that would satisfy both sets of requirements.

REQUIREMENTS

The following is a summarization of the original specifications for the four-channel PCM DAC and the 64-channel PCM DAC:

The four-channel PCM DAC will operate at +5.0 (±10%) VDC (VCC). The maximum current consumption will not exceed 50 milliamperes (mA). The four-channel PCM DAC will be packaged in a surface mountable plastic package not to exceed 14 mm by 14 mm.

The four-channel PCM DAC will have four analog input channels with an input impedance greater than 1 Meg Ohm and will accept signals from 0 to VCC Volts. An analog multiplexer will select one of the four inputs and route that signal to an analog to digital converter (A/D). The A/D will sample the signals from the multiplexer at up to 480 kilosamples-per-second (kS/s). The A/D will provide a 12-bit word conversion with a minimum SNR of 54 dB. The data will be PCM encoded in accordance with the IRIG-106-96 Telemetry Standard. The PCM DAC will be capable of output bit rates from 62.5 kilobits per second (kb/s) to 10 megabits per second (Mb/s).

If the internal clock is used, the encoder bit rate stability will be within 2%. If an external clock source is used the encoder bit rate stability will be within 0.1% of the external clock stability.

The output code type will be NRZ-L or RNRZ-L. The default will be NRZ-L. The frame synchronization pattern will be FAF320 in hexadecimal and will be placed at the end of the frame. A 12-bit word frame counter will increment with each occurrence of the synchronization word. The frame format will be 7 words-per-frame and numbered in sequence from 1 to 7, where the first 4 are the four analog channels, followed by a frame counter word, and 2 sync words. Word alignment will be most significant bit first.

The 64-channel PCM DAC required all the above, plus the following additional requirements:

The PCM frame format will be programmable with 7 to 1024 words-per-frame. Supercommutation capability will be supported. A PC based user-programming interface will be provided to select the frame format and signal conditioning values.

The maximum current consumption will not exceed 250 mA at 10 Mb/s. The maximum package shall be a disk, which is 2.3” in diameter and 0.25” thick. This disk diameter and thickness is compatible with a 2.75” missile application.

The PCM DAC will have the ability to acquire and condition 64 analog input signals with programmable gain and offset voltages. The PCM DAC shall include; an asynchronous RS-232/RS-422 serial input interface that will operate at selectable baud rates of 56K to 5M baud with 8 bits, 1 stop bit, no parity, or 8 bits plus parity; a 12-bit parallel TTL compatible input port with handshaking, operating at up to 900K words per second; and twelve discrete input channels.

RESULTS OF THE SOLICITATION

Systems & Processes Engineering Corporation (SPEC) responded to the specifications and proposed a two-chip and Circuit Card Assembly (CCA) solution to meet the above design requirements. One chip (later called a PCM DAC) integrates a 12 bit, 480 kS/s Analog to Digital converter and four input multiplexer, with a programmable frame formatter. Another chip called the Input Signal Conditioner (ISC), integrates 16 analog channels, with independently selectable gain and offset, and a 16 to 1 analog multiplexer. The CCA, which is covered in another paper, combines the two chip types and allows for the testing and validation of the design for the 64-channel system. See Figure 1 for a block diagram of the original ISC chip and Figure 2 for a block diagram of the original PCM DAC chip.

THE INTEGRATED PRODUCT TEAM

The Integrated Product Team, consisting of SPEC, Army, Air Force, and Navy representatives set out to improve on the original requirements and the proposed design. The goal was to make the chip set more universal, without affecting the contract, if possible, thus applying the “Cost as an Independent Variable” concept.

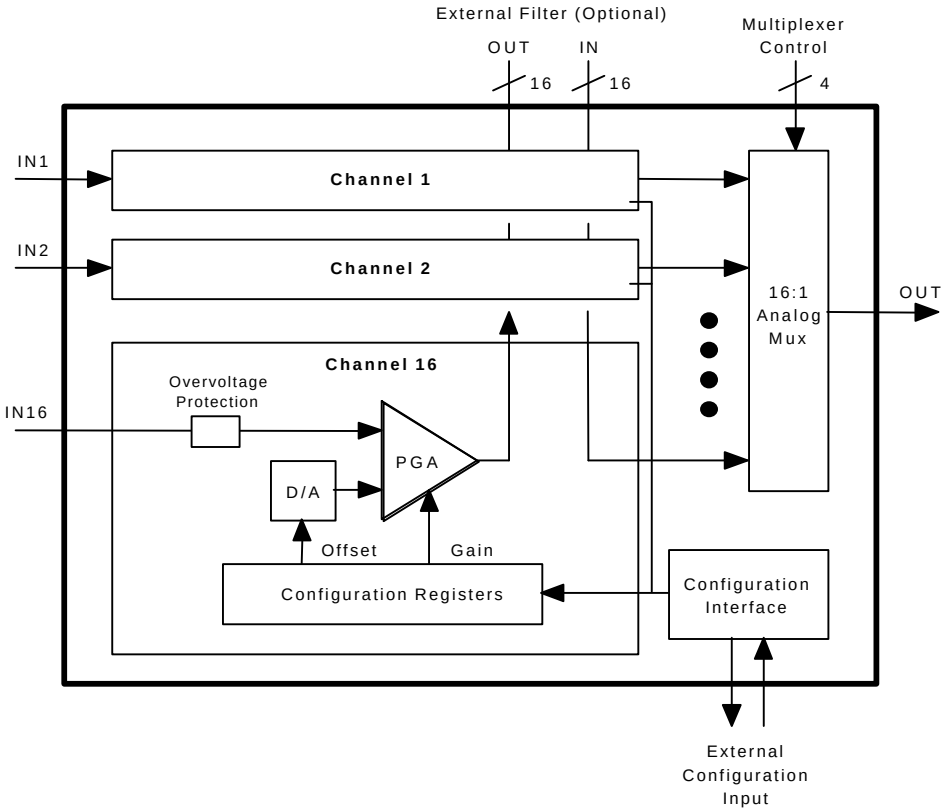

Figure 1: Original ISC Chip Architecture

DESIGN DECISIONS

One of the design changes was the addition of anti-aliasing filter for each of the 16 analog channels in the ISC chip. The original plan called for each channel to have an output pin after the gain and offset circuit and then an input pin going back into the multiplexer. This was done to allow for external anti-aliasing filters to be added based on the sample rate and required filter characteristics. The decision to place the filters off chip was based on calculations that indicated that the filters could not be integrated on-chip due to die size constraints. After further studying of the design, a recalculation of chip area was performed which resulted in the inclusion of filters for every channel (see Figure 3 for the revised block diagram of the ISC chip). The anti-aliasing filters are switched capacitor Butterworth type and are composed of two filter sections, 4 poles each, which can be selectively cascaded or disabled. The cut off frequency is selectable and is based on a submultiple of the input clock frequency.

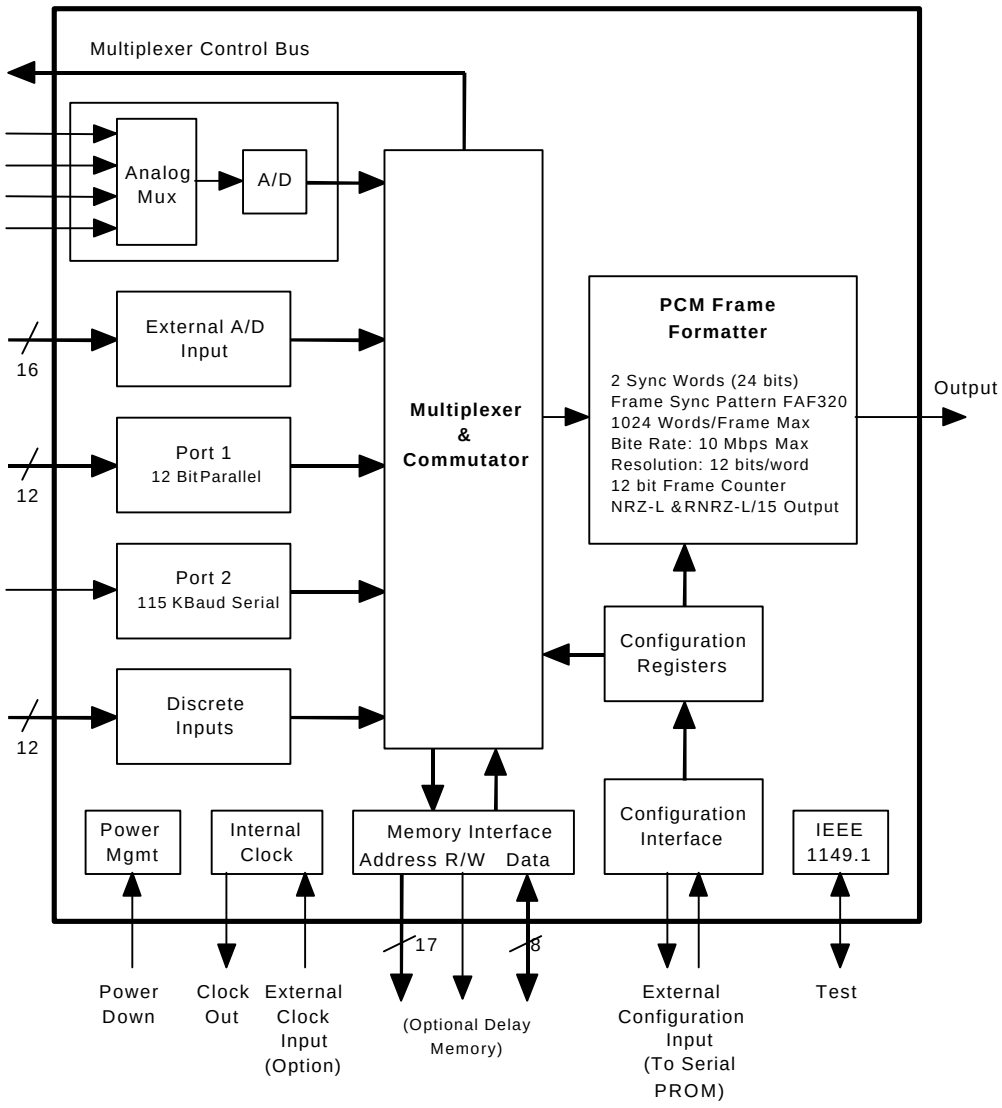

Figure 2: Original PCM DAC Architecture.

The next improvement to the design was the addition of programmable word size. A method was jointly devised that would allow for the implementation of PCM word sizes other than just 12 bits. The method allows the PCM frame to consist of words with a size of 8, 10, 12, or 16 bits. The external parallel and discrete ports were increased from 12 to 16 bits wide to accommodate the programmable word size.

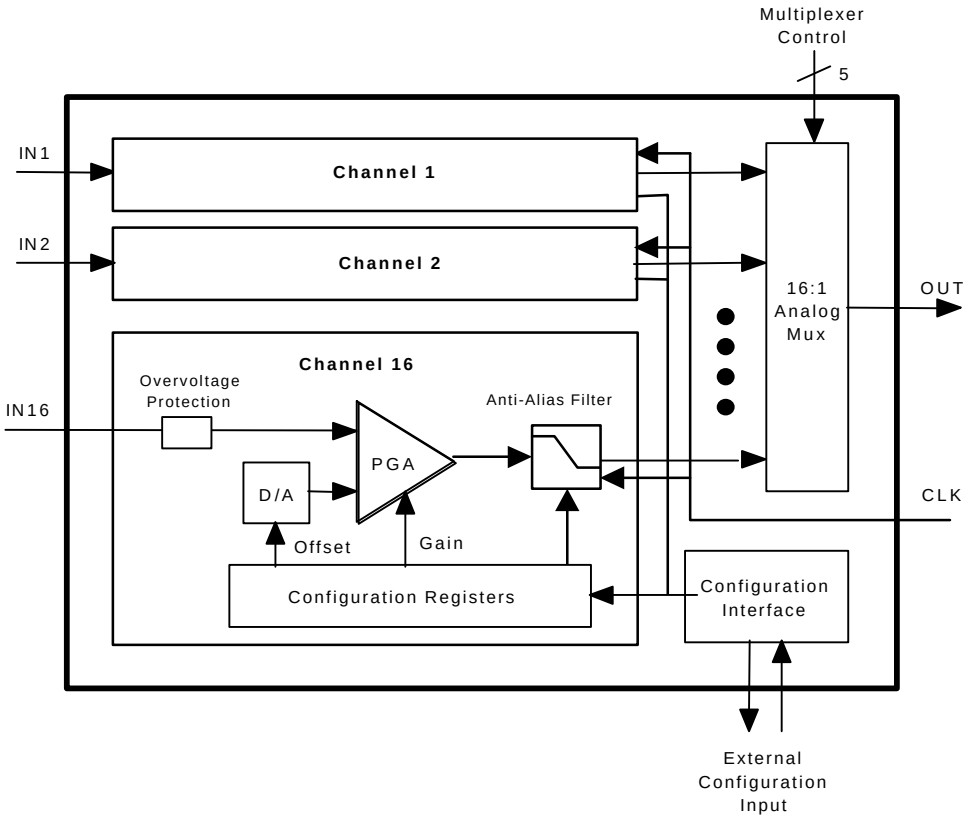

Figure 3: Current ISC Chip Architecture.

An increase in the flexibility of the PCM frame format programmability was added next. A method was devised that would allow for the PCM frame to consist of any major frame length between 7 and 2048 words, with up to eight minor frames per major frame. This allows for subcommutation of the PCM words and makes it possible to implement IRIG 106 Class II PCM frames types with a maximum of 16,384 bits per minor frame [3]. Examples of possible major frames include; (a) eight minor frames of 256, 8-bit words, (b) two minor frames of 1024, 10-bit words, (c) four minor frames of 256, 12-bit words, or (c) one frame of 1024, 16-bit words.

A decision was also made on how the PCM DAC and ISC chips would be electrically and functionally configured during system setup. A serial Programmable Read Only Memory (PROM) would be used to both setup the PCM frame format and the Gain/Offset/Filter values. The PCM DAC will control the serial PROM via clock, enable, and acknowledge lines. If the PROM is present the PCM DAC will clock the PROM until all information is clocked out. The DAC will simultaneously buffer and provide the serial data to the ISC chip(s) for their internal configuration settings. If no PROM is present the PCM DAC will power up in a default seven-word frame setting. See Figure 4 for a block diagram of the revised PCM DAC and Figure 5 for a complete 64-channel system.

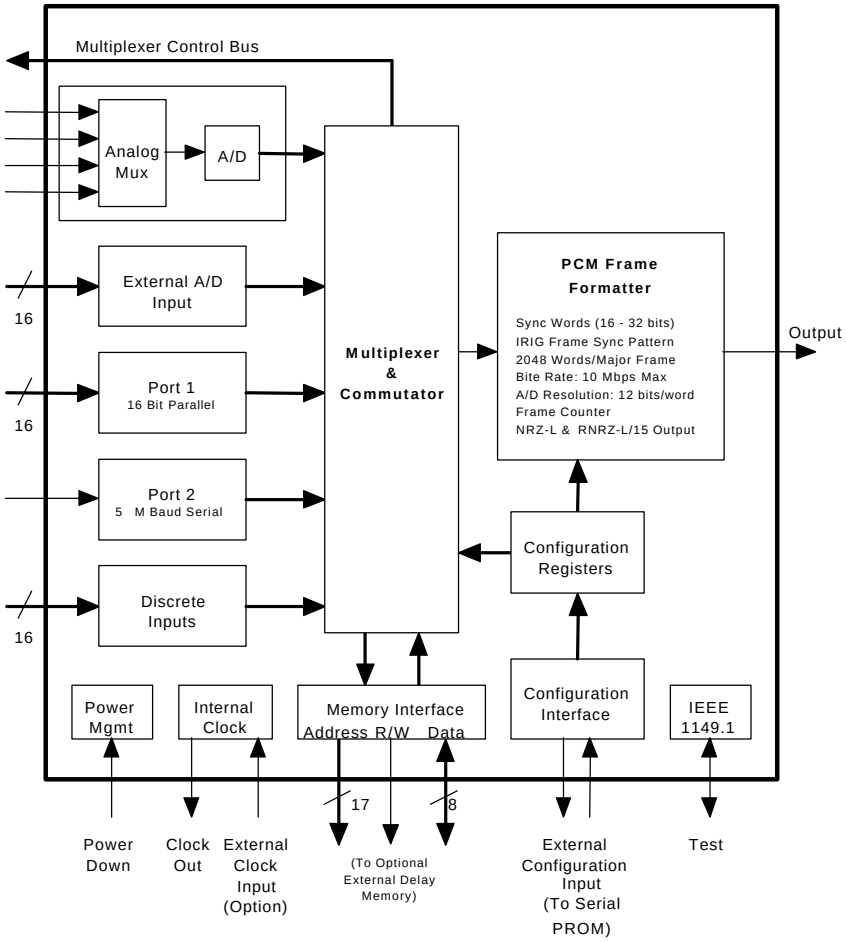

Figure 4. Current PCM DAC Architecture.

ADDITIONAL FEATURES

SPEC's design provides for an external memory interface capability for delaying and repeating the captured data. The delay time is dependent on the amount of external memory the system contains. This feature allows for the recording and later replaying of data that may not otherwise be transmitted and received. An example of this data could be in-bore pressure data for artillery rounds.

Several power saving techniques are planned to improve chip performance. These include selectively clocking only the functions that are needed to perform the task at hand, powering down the entire chip into a sleep mode, and developing the IC's core functions to be as power efficient as possible.

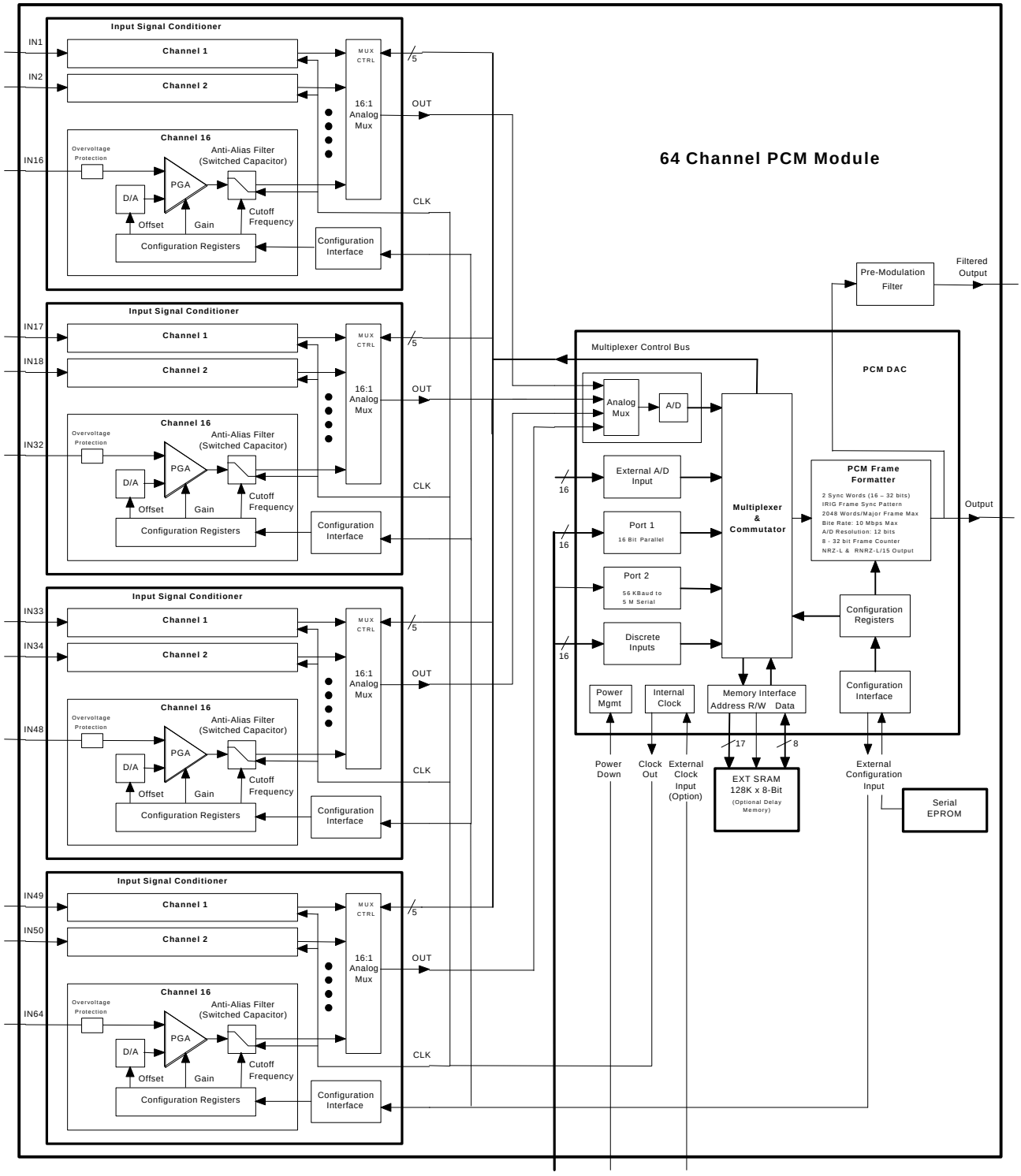

Figure 5. Block Diagram of a Complete 64-Channel PCM DAC System.

A minor frame counter will be available to include in the PCM stream. The frame sync word will be IRIG 106 compliant and will consist of two words (16-bits, 20-bits, 24-bits, or 32-bits).

A 16-bit port will be provided to allow for interfacing to an external A/D converter. This will allow for future upgrades as technology changes and improves.

PRACTICAL LIMITATIONS

The base size of the A/D converter internal to the PCM DAC will be 12 bits with a maximum sample rate of 480 kS/s. If a word size of 16 bits/word is selected and the internal A/D is used, the Least Significant Bits (LSB's) of the analog word will be output as zeros. If 10 or 8 bits per word are selected, the Most Significant Bits (MSB's) of the A/D converter will be output. The LSB's of the 16 bit external ports are not sampled if less than 16 bits per word is selected for the bits/word.

All words in the PCM frame will have the same bit length. Any non-standard or variable word size formatting will have to be preformed external to the PCM DAC and forced to conform to selected word size. The formatted data can then be input through one of the digital port interfaces, placed in the PCM frame, and then decoded after reception.

Analog input signals to the ISC and PCM DAC chips will be limited to 0 to VCC (+5) Volts. This is necessary due to the I/O protection circuitry and the single supply rail of the parts. The full, undistorted, analog input range to the chips will be about 0.2 Volts to 4.2 Volts. This constraint is due to the voltage reference circuitry and opamp distortion characteristics. The above limitations require that major voltage offset and attenuation adjustments be performed external to the chips. However, because the gain and offset is programmable for each channel, it is possible for the input adjustment circuits to use common component values, thus reducing system complexity and cost.

SUMMARY

This paper discussed the design and development of the HSTSS Data Acquisition Chips. The development effort is a prime example of what can be accomplished if the Government and Industry work together as a team. The design and development of the HSTSS components is resulting in the creation of telemetry building blocks for use in a multitude of applications. With the goals of low cost and ease of use for the end user, the components will allow for the instrumentation of previously uninstrumented systems and cost reductions to current telemetry systems. The PCM DAC and ISC chip are integral building blocks to these systems and with the forethought of future expandability, should remain viable components for many years to come.

REFERENCES

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