

# **Digital FDM for the HSTSS DAC Program**

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## **ABSTRACT**

This paper presents the design of an innovative approach to Frequency Division Multiplexing (FDM) for the STRICOM Hardened Subminiature Telemetry and Sensor System (HSTSS) Data Acquisition Chipset (DAC) program. An ASIC (Application Specific Integrated Circuit) is being developed by Systems & Processes Engineering Corporation (SPEC) that implements this new digital FDM approach for telemetry applications. The FDM ASIC provides six channels that are IRIG-106 compatible, and may be used in conjunction with a Delay/Repeater ASIC. Together these ASICs make a complete instrumentation system for those applications requiring very small size, simplicity of use, and low cost, e.g. munitions/armament testing.

## **KEY WORDS**

Frequency Modulation, Frequency Division Multiplexing, Digital Modulation, Telemetry, ASIC

## **INTRODUCTION**

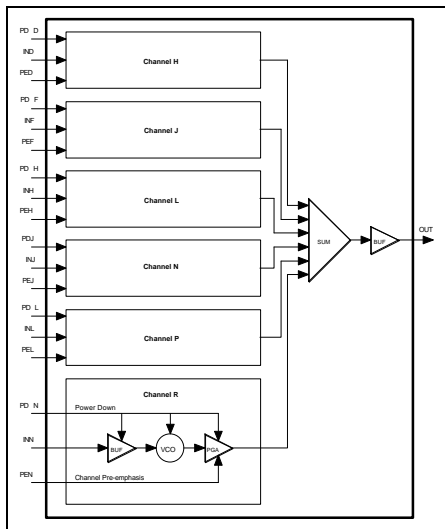
Traditional FDM approaches are based on analog schemes in which the outputs of frequency modulated voltage controlled oscillators are summed into a composite signal. However, this traditional approach offers limited programmability and accuracy when integrated into a modern semiconductor process. SPEC's mixed-signal approach implements the same functions, but with increased capabilities by performing all the modulation and summing in the digital domain. This allows more flexibility to be built into the chip, e.g. programmable center frequencies, programmable bandwidths, programmable pre-emphasis, and cascading of ASICs to increase the number of channels.

The Delay/Repeater ASIC will accept up to three analog inputs with a bandwidth of 0 to 60 KHz and provide programmable delay times of 0 to 175 ms (with external SRAM). The FDM ASIC and Delay/Repeater ASIC, combined, are fully IRIG-106 compliant and provide the instrumentation community with a miniature, low power, low cost solution.

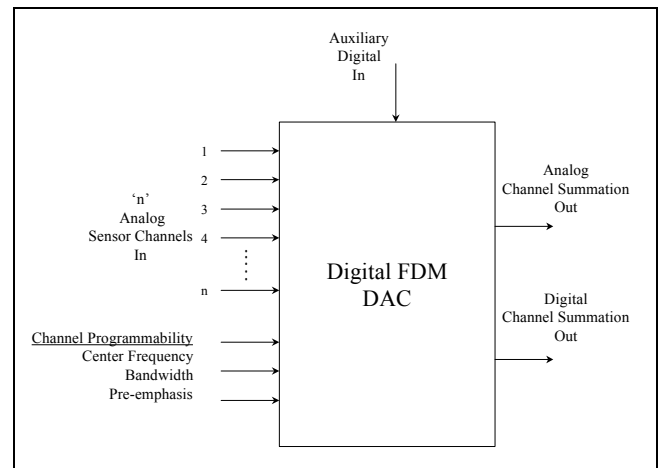
## THE DIGITAL FDM ASIC: TRADITIONAL FDM WITH A NEW TWIST

Traditional FDM/FM approaches are based on analog schemes consisting of frequency modulation (FM), voltage controlled oscillators and summer elements, as shown in Figure 1. SPEC and the STRICOM HSTSS program have recognized a need for a FDM/FM chip that allows more flexibility than can be achieved through the traditional analog approach.

Therefore, SPEC is developing the Digital FDM shown in Figure 2. The main principles are the same. It takes analog signals in, modulates them according to the IRIG 106 Telemetry Standard and sums the channels for output. The difference is that all the traditionally analog functions in the chip are now performed in the digital domain. However, the digital functionality is totally transparent to the user.



**Figure 1: Traditional FDM/FM Analog Approach**



**Figure 2: The Digital FDM ASIC**

The Digital FDM DAC accepts six analog inputs, and outputs the summed FDM/FM channels. The Digital FDM's supported default PBW channels are outlined in Table 1. The analog inputs are linearly mapped into the phase domain where they are synthesized and summed into a single composite radio frequency signal ready for up conversion and transmission. Pre-emphasis amplifiers are provided to enhance selected frequency components of the independent channels. Each channel can be independently enabled,

permitting lower power consumption in standby mode or if fewer than six channels are required by the application. The chip can also be programmed to support both proportional bandwidth (PBW) and constant bandwidth (CBW) channels.

**Table 1: Digital FDM PBW Default IRIG-106 Channels**

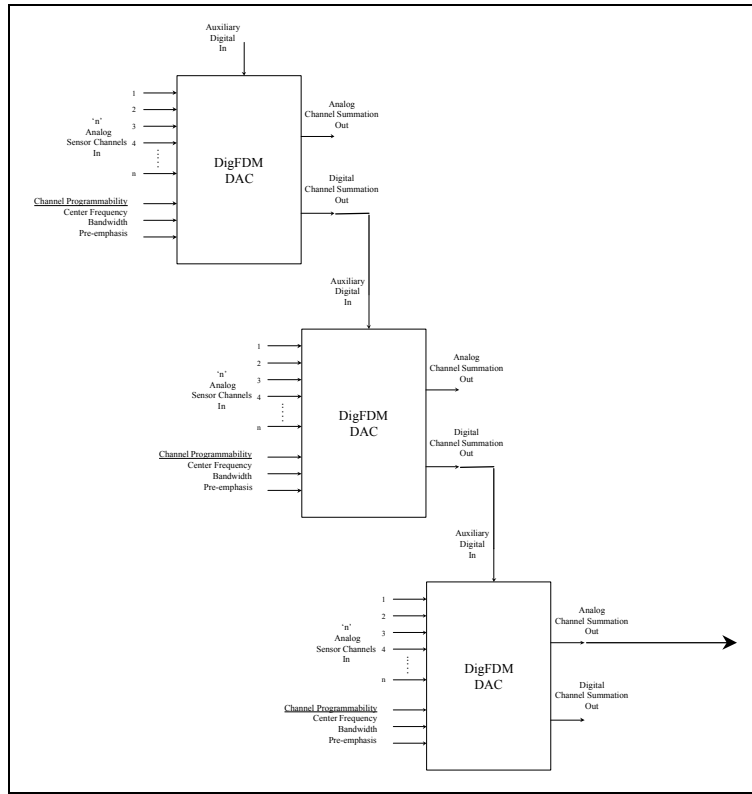
PROPORTIONAL BANDWIDTH FM SUBCARRIER CHANNELS ± 15 % CHANNELS					
Channel	Center Frequency (KHz)	Lower Deviation Limit (KHz)	Upper Deviation Limit (KHz)	Nominal Frequency Response (Hz)	Maximum Frequency Response (KHz)
F	93.0	79.050	106.95	2790	13.95
H	165.0	140.25	189.75	4950	24.75
J	300.0	255.0	345.0	9000	45.0
L	560.0	476.0	644.0	16800	84.0
N	930.0	790.5	1069.5	27900	139.5
P	1650.0	1402.5	1897.5	49500	247.5

The benefits to performing modulation in the digital domain are the following:

- Programmable and reconfigurable channel center frequency
- Programmable and reconfigurable channel bandwidth
- Programmable and reconfigurable channel pre-emphasis
- Cascading Chips provide an increased number of available channels

The digital channel summation out and auxiliary digital in ports are employed to cascade the chip. Cascading the Digital FDM DAC increases available channels from ‘6’ to “6 \* n of chips” so that the user is not limited to the number of channels on a single chip. Figure 3 illustrates this principle.

The digital approach, described in the following sections, allows for more flexibility to be built in to the chip through its increased technical capabilities. This, in turn, leads to its use in a broader spectrum of applications including those requiring small size, simplicity of use, and low cost.



**Figure 3: The Digital FDM DAC Cascaded System**

### DEFINING FREQUENCY MODULATION

Frequency modulation is a type of angle modulation. To generate an angle modulated signal, the modulated carrier is held constant and either the phase or the time derivative of the phase of the carrier is varied linearly with the message signal  $m(t)$ . Therefore, the general form of an angle modulated signal is

$$x_c(t) = A_c \cos[2\pi f_c t + \mathbf{f}(t)] \quad (1)$$

The instantaneous phase of  $x_c(t)$  is

$$\mathbf{q}_i(t) = 2\pi f_c t + \mathbf{f}(t), \quad (2)$$

where  $\mathbf{f}(t)$  is the phase deviation.

The phase deviation of a frequency modulated carrier is

$$\mathbf{f}(t) = 2\pi f_d \int_{t_0}^t m(\mathbf{a}) d\mathbf{a} + \mathbf{f}_0, \quad (3)$$

where  $\mathbf{f}_0$  is the phase deviation at  $t = t_0$ .

Therefore, the frequency modulator output is

$$x_c(t) = A_c \cos \left[ 2\pi f_c t + 2\pi f_d \int_{t_0}^t m(\mathbf{a}) d\mathbf{a} \right]. \quad (4)$$



## DIGITAL IMPLEMENTATION RESULTS

The following simulation results of the Digital FDM DAC were performed in SPW (System Processing WorkSystem<sup>®</sup> ALTA GROUP<sup>™</sup> of Cadence Design Systems, Inc.).

Figure 5 shows the results of Channel P ( $f_c = 1650$  MHz) modulated with  $1 \cdot \cos[2\pi f_m t]$  and  $f_m = 49.5$  KHz, which corresponds to  $b = 5$ .

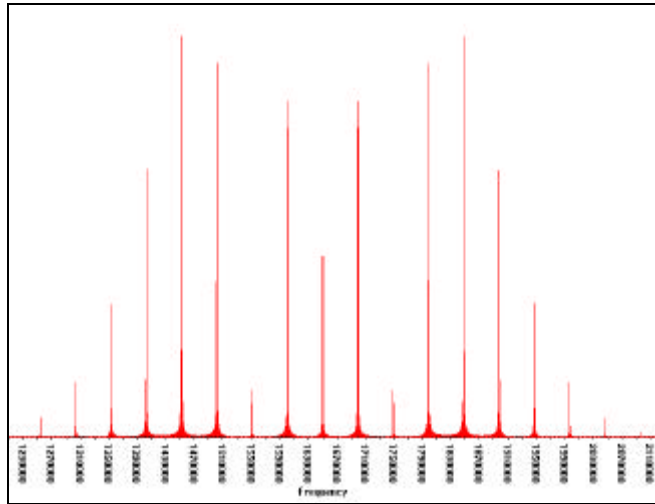


Figure 5: Amplitude Spectral Density of Channel P modulated with  $b = 5$ , and  $f_m = 49.5$  KHz.

Figure 6 shows simulation results of all channels from Table 1 being modulated with frequencies corresponding to  $b = 5$  on a linear scale.

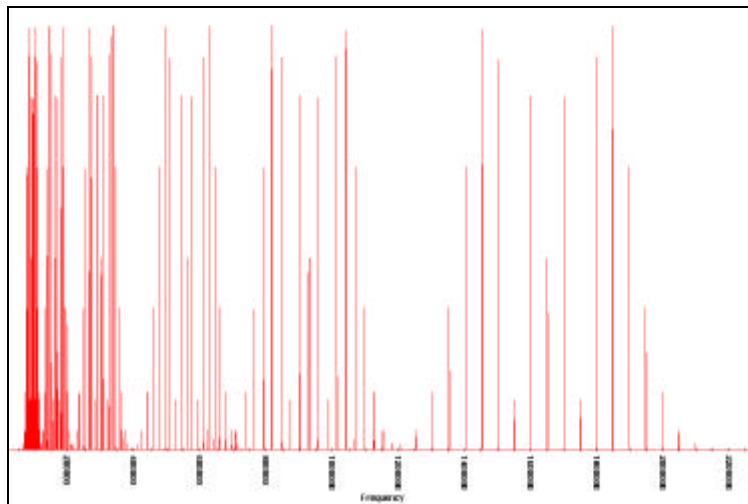


Figure 6: Amplitude Spectral Density of all channels modulated with  $b = 5$  on a linear scale.

Figure 7 shows simulation results of all channels from Table 1 being modulated with frequencies corresponding to  $b = 5$  on a dB scale.

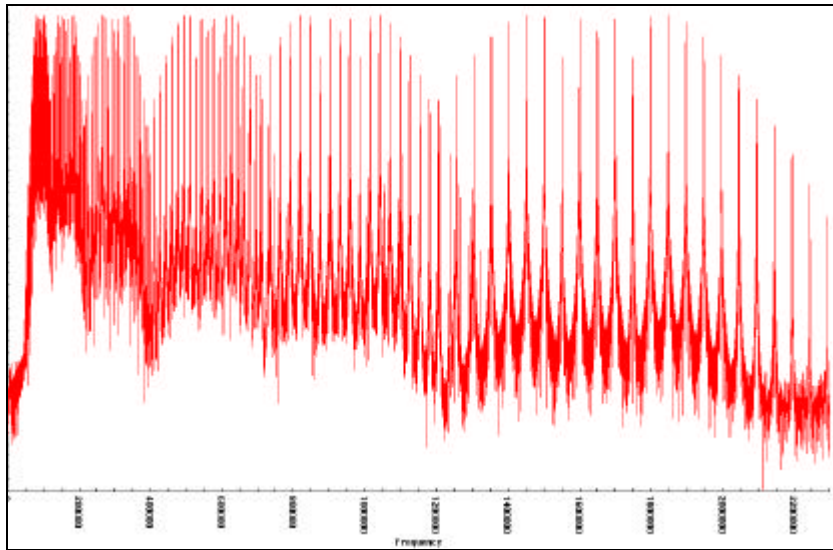


Figure 7: Power Spectral Density of all channels modulated with  $b = 5$  on a dB scale.

## THE DELAY/REPEATER DAC

The Delay/Repeater DAC, shown in Figure 8, provides three channels of delayed or delayed and repeated analog signals with a bandwidth range of 0 to 60 KHz. The DAC Delay/Repeater provides up to 20 ms of time delay in 5 ms increments on-chip. A maximum delay of 175 ms can be achieved using an external COTS SRAM with the DAC Delay/Repeater. The 3 Channel Delay/Repeater DAC uses a mixed signal implementation whereby the signal is digitized, stored in a digital memory, and reconstructed at a later time through a digital-to-analog (D/A) converter.

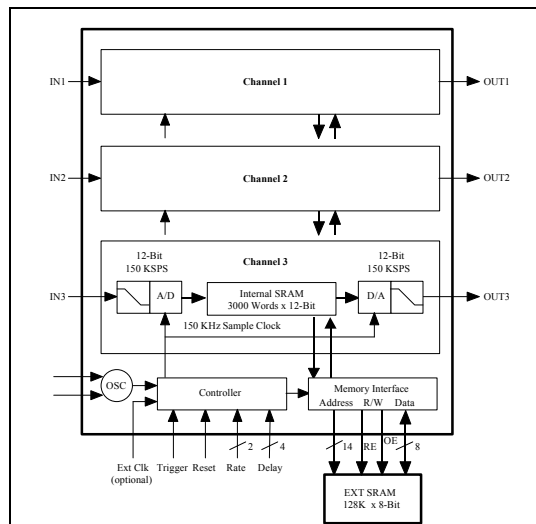


Figure 8: The Delay/Repeater ASIC

The input is fed into three independent 12 bit analog-to-digital (A/D) converters, which are used to sample the signal waveform at a sample rate of 150 KSPS. This rate is sufficient to meet the Nyquist criteria of the signal bandwidth and to allow for anti-alias filter rolloff. The outputs of the A/D converters are bussed to the internal memory (3 channels x 12 bits x 150 KSPS x 0.02 s = 108 Kbits) or to the external memory interface.

For the external interface, on alternate clock cycles, data is written to and read from memory, with the waveform time delay corresponding to the offset between the write and the read addresses. After the data is read from memory, it is fed into three independent D/A converters for signal reconstruction. Output filters remove spurs generated by the D/A converter.

Programming the Delay/Repeater Chipset is done with discrete signals that are set using dip switches and/or jumpers to provide the input control signals. The delay/repeat mode is controlled via a dip switch/jumper. If the dip switch is set to “on”, then that channel will be in delay mode, otherwise the channel will be in repeat mode. The delay is set for all channels and only one delay value can be set. Since the ranges for the delay are set from 0 to 175 milliseconds, values are encoded in four dip switches/jumpers.

## CONCLUSION

SPEC's mixed-signal approach to the Digital FDM DAC implements the same functions as a traditional analog system, but with increased capabilities by performing all the modulation and summing in the digital domain. This allows more flexibility to be built into the chip, including programmable center frequencies, programmable bandwidths, programmable pre-emphasis, and cascading of the ASICs to increase the number of channels.

Together, the Digital FDM DAC and the Delay/Repeater DAC provide the instrumentation community with more options and capabilities than current systems at lower cost, less power, and smaller size.

The Digital FDM DAC and Delay/Repeater DAC should be available in the first quarter of calendar year 2000.

## SELECTED RELEVANT LITERATURE

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