HARDWARE PERFORMANCE FOR BINARY GMSK WITH BT=1/5

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ABSTRACT

The design, implementation, and performance of a digital modem employing Gaussian minimum shift keying (GMSK) is described. The GMSK modem is implemented in field programmable gate array (FPGA) chips, and a laboratory test setup was developed to validate its performance for a signal BT value of 1/5. The measured spectrum of the GMSK modem and its bit error rate (BER) performance, which are found in very close agreement with those of theory and simulation, are presented in this paper.

KEY WORDS

GMSK, CPM, Data Pre-coding, Tracking Loops, BER.

INTRODUCTION

The GMSK signal with BT=1/5 exhibits a very good trade-off between power and bandwidth efficiency. The compact spectrum of this signal makes it a very promising waveform to use for future space system applications with a constrained channel bandwidth. Due to the smoothness of the signal, the demodulation and the tracking functions for the GMSK signal are also more complex to implement than a conventional phase modulation waveform [2]. The Aerospace Corporation has bread-boarded a BT=1/5 GMSK modem and has obtained its measured BER performance with and without the tracking loop functions via a laboratory hardware test setup, as an attempt to address the question: Can a GMSK digital modem be implemented with a reasonable amount of hardware, and how good will the performance be? The purpose of this paper is to describe the implementation details of this modem and compare its performance to that obtained by software simulation. Specifically, both the pre-coded binary GMSK modulator and the demodulator with symbol time and carrier phase tracking loops for BT=1/5, implemented in XILINX FPGA chips, are discussed. The gate count of the circuits will be described. This paper is organized as follows: a detailed design of the modulator and the demodulator is described in the next section, followed by a description of the laboratory setup. Then measured performance results of this modem are presented and conclusions are advanced.

MODULATOR DESIGN

The GMSK BT=1/5 baseband modulator, shown in Figure 1, converts the incoming data streams into I (in phase) and Q (quadrature phase) analog waveforms. All the circuits are digital except the digital-to-analog (D/A) converters. Every symbol has 8 samples. On the left-hand side of Figure 1, the pre-coded incoming data continuously shifts into the 5-bit shift register at the symbol rate which is 1 Mb/s. It can be thought of as a 5-bit moving window on the data stream. The 5 data bits in the register determine via "$\Delta\phi$ Table" the frequency of the baseband waveform for the symbol period. The frequency is then added to the current phase of the baseband waveform, then producing the next phase sample of the waveform. The digital phase value is fed to the sine and cosine lookup table to produce the digital I and Q values. The baseband I and Q are then generated using the two D/A converters.

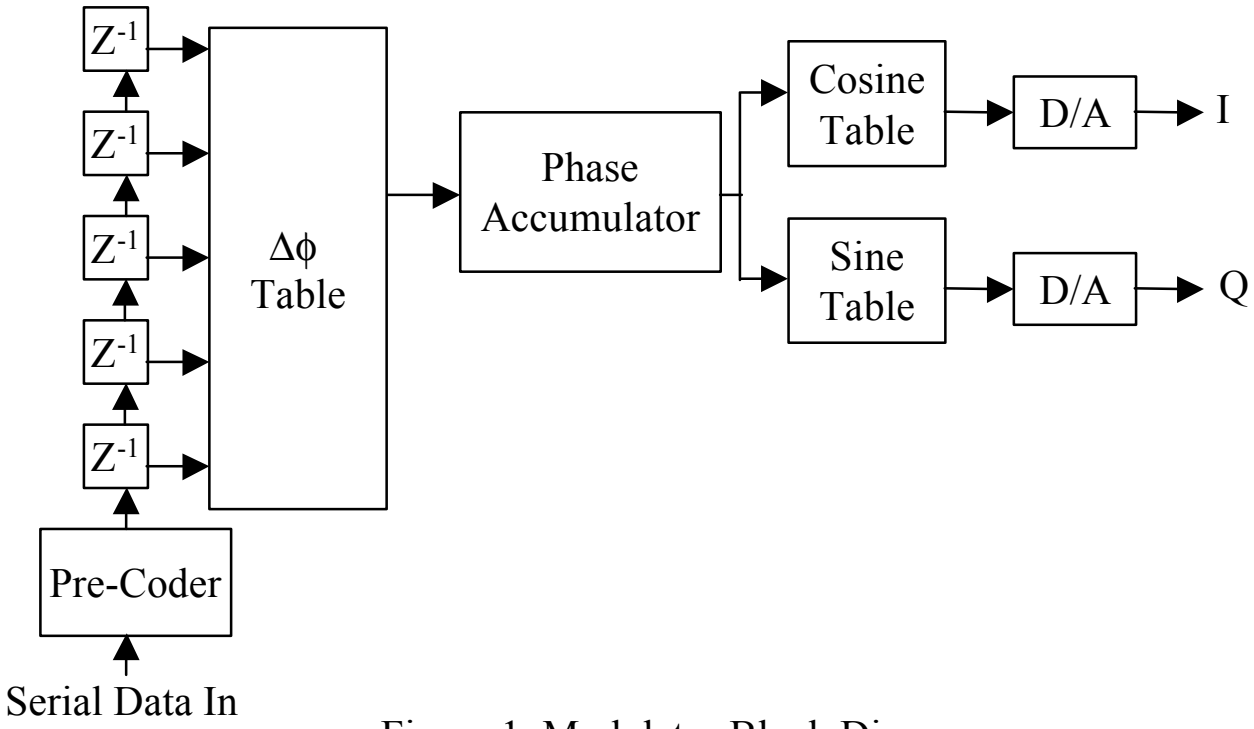

Figure 1, Modulator Block Diagram

DEMODULATOR DESIGN

The digital GMSK demodulator with data-aided symbol time and carrier phase tracking for pre-coded signals, as described by Lui and Tsai [2], has been implemented. The digital GMSK demodulator, shown in Figure 2, processes the digitized I and Q baseband signals and outputs the demodulated data bit. The symbol pulse and sampling clock generator at the top right corner controls and synchronizes all the blocks in Figure 2. One symbol pulse is generated for every 8 sampling clocks. The digitized I and Q signals first

go through a phase rotation according to the phase correction signal, which is generated by the carrier phase tracking loop. Both of the rotated I and Q signals are fed into two FIR filters and an early late gate, which can also be mechanized as a FIR filter, with the first 23 tap coefficients equal to 1. The 24th tap coefficient is 0, and the last 24 tap coefficients are –1. The two 48 tap FIR filters in the middle of Figure 2 are h_0 filters [2]. The two 32 taps FIR filters are h_1 filters [1]. All the FIR filters in addition to the early and late gates are clocked at the sampling rate, but their outputs are sampled at the symbol rate. The multiplexer receives the two inputs at the symbol rate and then alternately outputs the inputs at the symbol rate. The sequence of output for the even-odd multiplexer is the opposite of that of the odd-even multiplexer. The even-odd-alternated output of the two h_0 filters is sent to a 1-bit hard limiter, which produces the serially demodulated data bit [3]. The data bit is multiplied with the top even-odd-alternated output of the two early late gates to produce the timing error signal. It goes through a second-order feedback loop filter to generate the time correction signal to the symbol pulse and sampling clock generator. The serially demodulated data bit is multiplied with the output of the odd-even-alternated output of the h_0 filters to produce the phase error signal. It goes through another second order feedback loop filter to generate the phase correction signal to the phase rotation circuits. The outputs of the two bottom even and odd multiplexers are sent to the trellis demodulation circuits which produces the trellis-demodulated [3] data bit. The trellis demod circuits consist of 4 states and 8 stages. The two second-order feedback loop filters and the trellis demodulator operate at the symbol rate.

MODULATOR AND DEMODULATOR FPGA CHIPS AND CIRCUITS BOARD

Both the digital modulator and the digital demodulator circuits are built using the SPW HDS model. The SPW VHDL RTL LINK generates the VHDL code of the circuits. The SYNOPSYS FPGA EXPRESS generates the netlist file from VHDL code and XILINX ALLIANCE software produces the final bit file for the XLINX FPGA chip. The modulator occupies less than 10% of one XC40150 chip's resources. The demodulator occupies about 60% of two XC40150 chips' resources. The modulator also uses two static RAMs. All of them are mounted on an APTIX MP3 board. The two XC40150 chips of the demodulator and another static RAM are mounted on an APTIX MP3A board. The SYNOPSYS DESIGN COMPILER generates the two netlist files for the two APTIX boards from the VHDL codes, which come from SPW VHDL RTL LINK. First the APTIX's EXPLORE software downloads the netlists to the two APTIX boards, then the XILINX ALLIANCE software downloads the bit patterns into all the XILINX chips. Hence the modulator circuit board and demodulator circuit board are ready to operate.

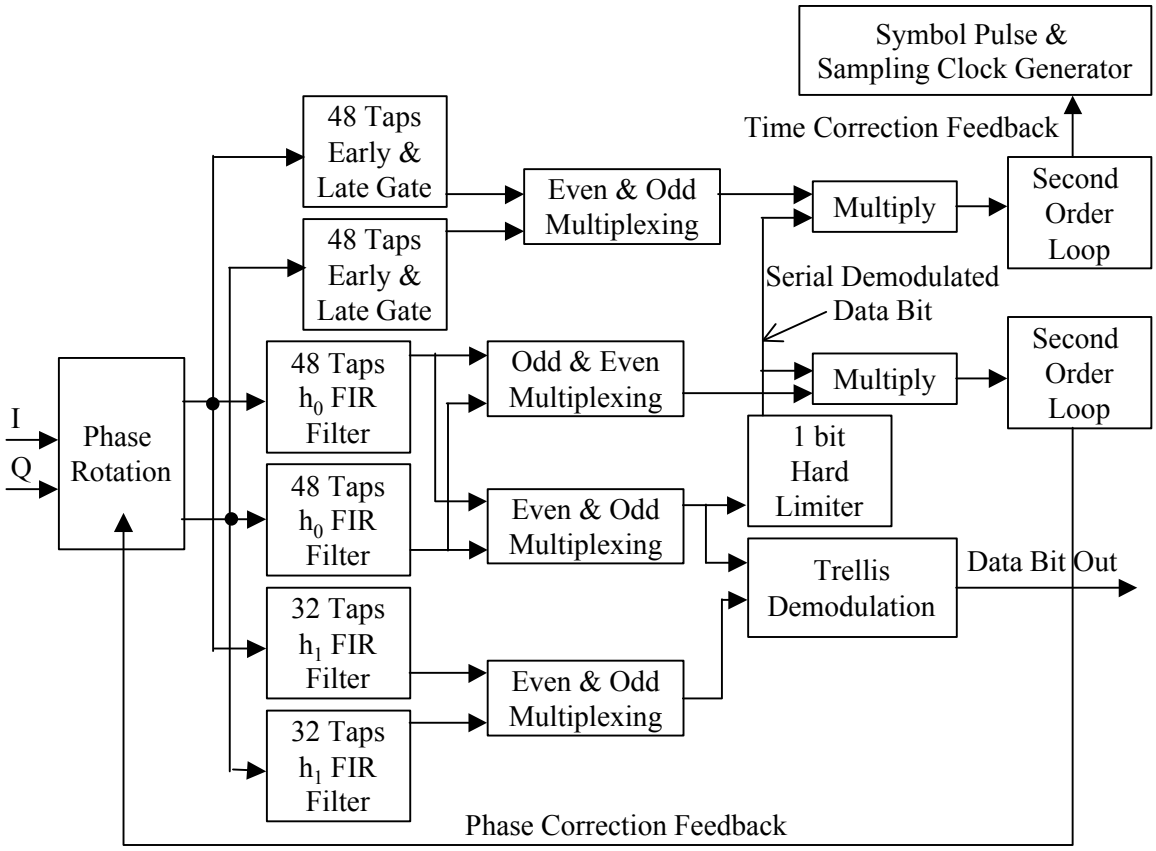

Figure 2, Demodulator Block Diagram

TEST SETUP

The modulator and the demodulator were first tested with hard-wired (ideal) symbol time and carrier phase tracking loops. The test setup is shown in Figure 3. The bit error rate tester generates a pseudorandom data bit stream. The GMSK modulator and the two D/A converters convert the data stream into baseband I & Q signals. The HP 8780A up-converts the signals to a 118 MHz IF signal. The IF signal, combined with noise, goes through a bandpass filter, an amplifier, and a power divider. One output of the power divider goes to the spectrum analyzer, which is used to measure the spectrum of the signal and to measure the signal-to-noise ratio. The other output of the power divider goes through a downconverter, of which the outputs are the baseband I & Q signals. The digitized I & Q are sent to the GMSK demodulator that produce recovered data bit stream. The BER tester compares the received data bits with the transmitted data bits and then displays the bit error rate. The UN-modulated 118 MHz IF signal of the HP 8780A up converter is used by the I/Q converter so that the received I & Q signals are at 0 frequency. It enables the demodulator to operate without the phase tracking loop. The modulator and the demodulator also share the same system clock so that they can work without the time tracking loop.

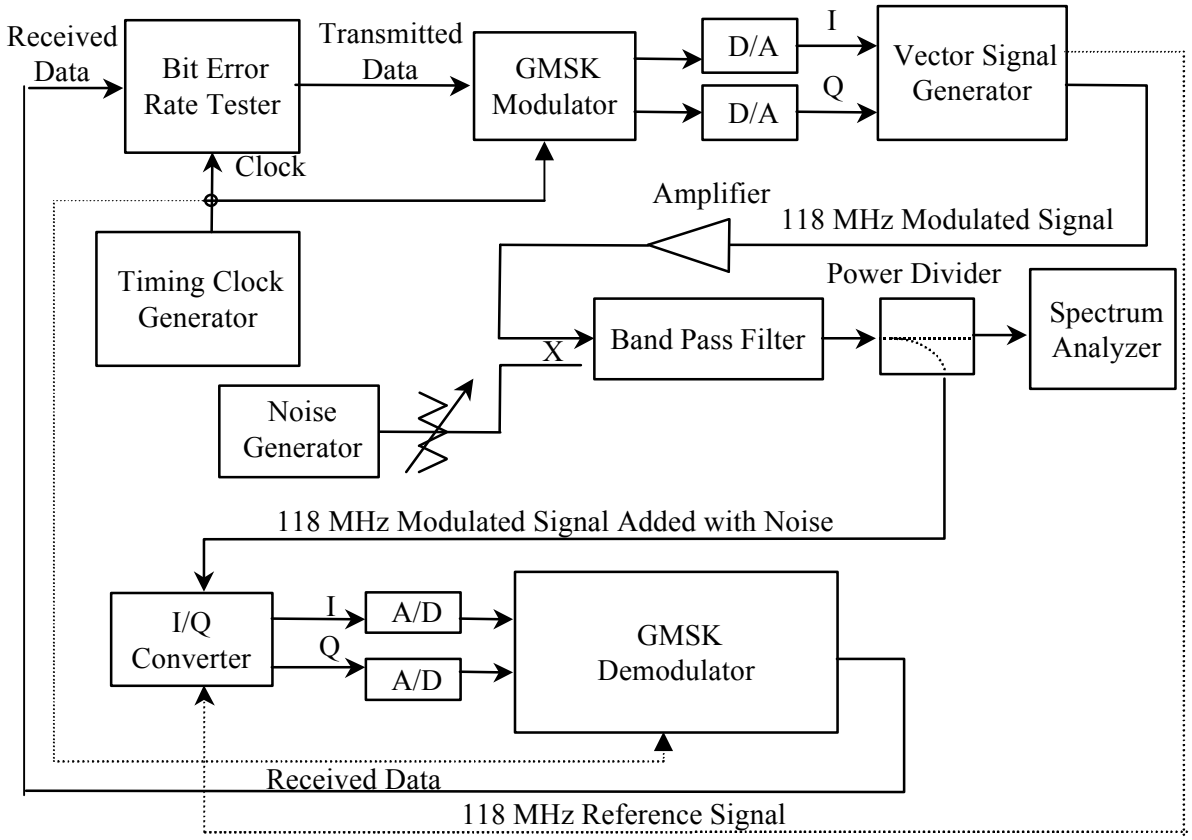

Figure 3, GMSK Modulator and Demodulator with Ideal Time and Phase

The measured spectrum is shown in Figure 4, and the theoretical spectrum is shown in Figure 5. The difference between the two figures is mainly on the level of the noise floor. The bit error rate curves are shown in Figure 6. The difference between the measured and the simulated values indicates less than 0.5 dB degradation due to implementation.

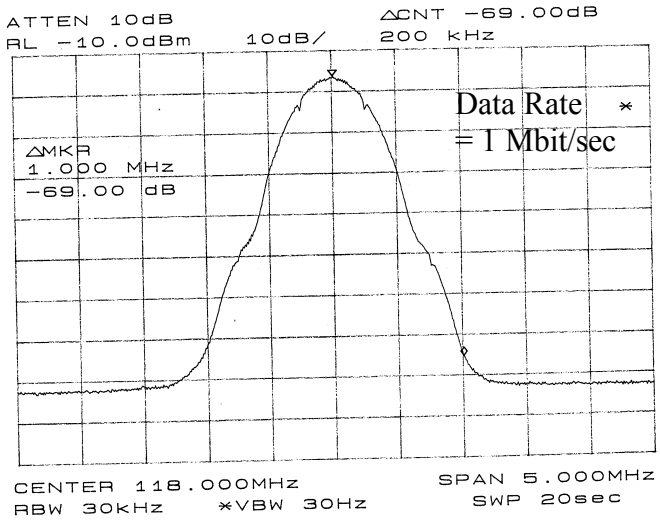

Figure 4, Measured GMSK Spectrum, BT = 1/5

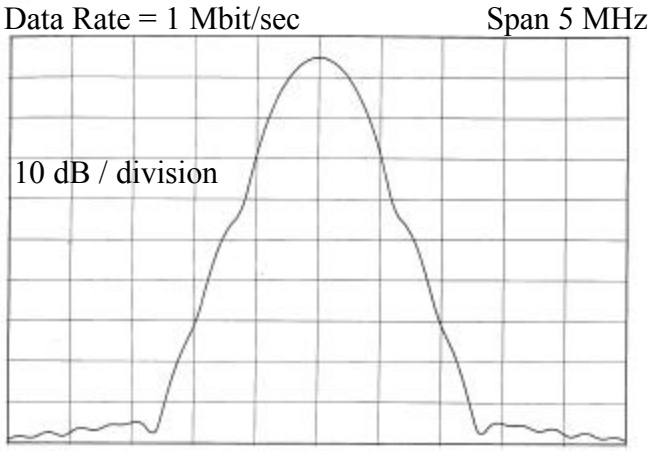

Figure 5, Theoretical GMSK Spectrum, BT = 1/5

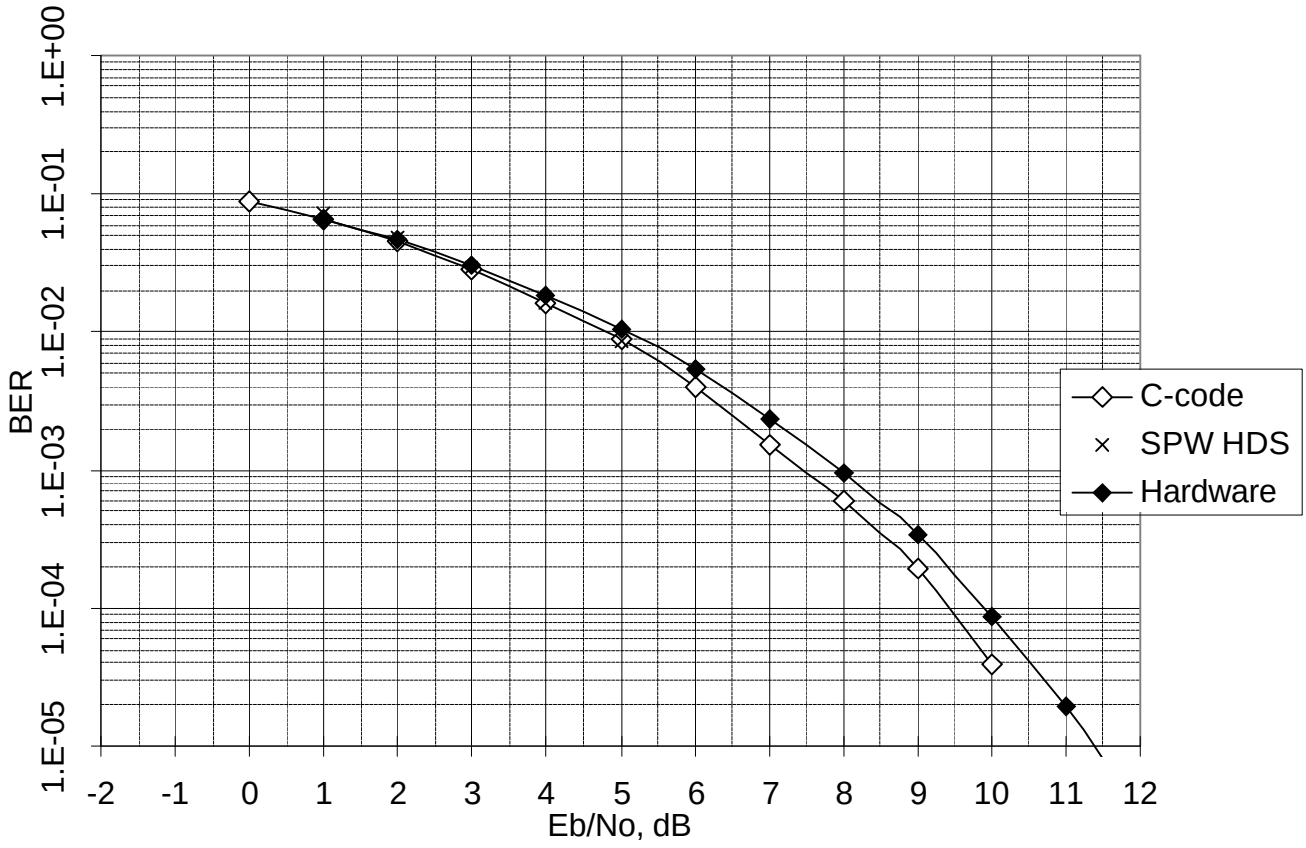

Figure 6, GMSK BT=1/5 Bit Error Rate versus Signal-to-Noise-Ratio

The modulator and the demodulator will be tested with both symbol time and carrier phase tracking in place. The test setup is shown in Figure 7. In comparison to Figure 3, the demodulator clock generator and the downconverter's frequency source are independent with respect to those of the modulator.

CONCLUSION

A digital hardware design and implementation of the binary GMSK modem with time and carrier phase tracking loops as proposed by Lui and Tsai [2] has been presented. It was shown that the measured spectrum and BER performance of this modem are in close agreement with those of theory and simulation. At the time of this writing, BER performance of this modem for the case with both time and carrier phase tracking is being measured; we hope to discuss these results in the conference. In passing it should be noted that although the current design is developed for BT=1/5, extending it to other signal BT values is straightforward.

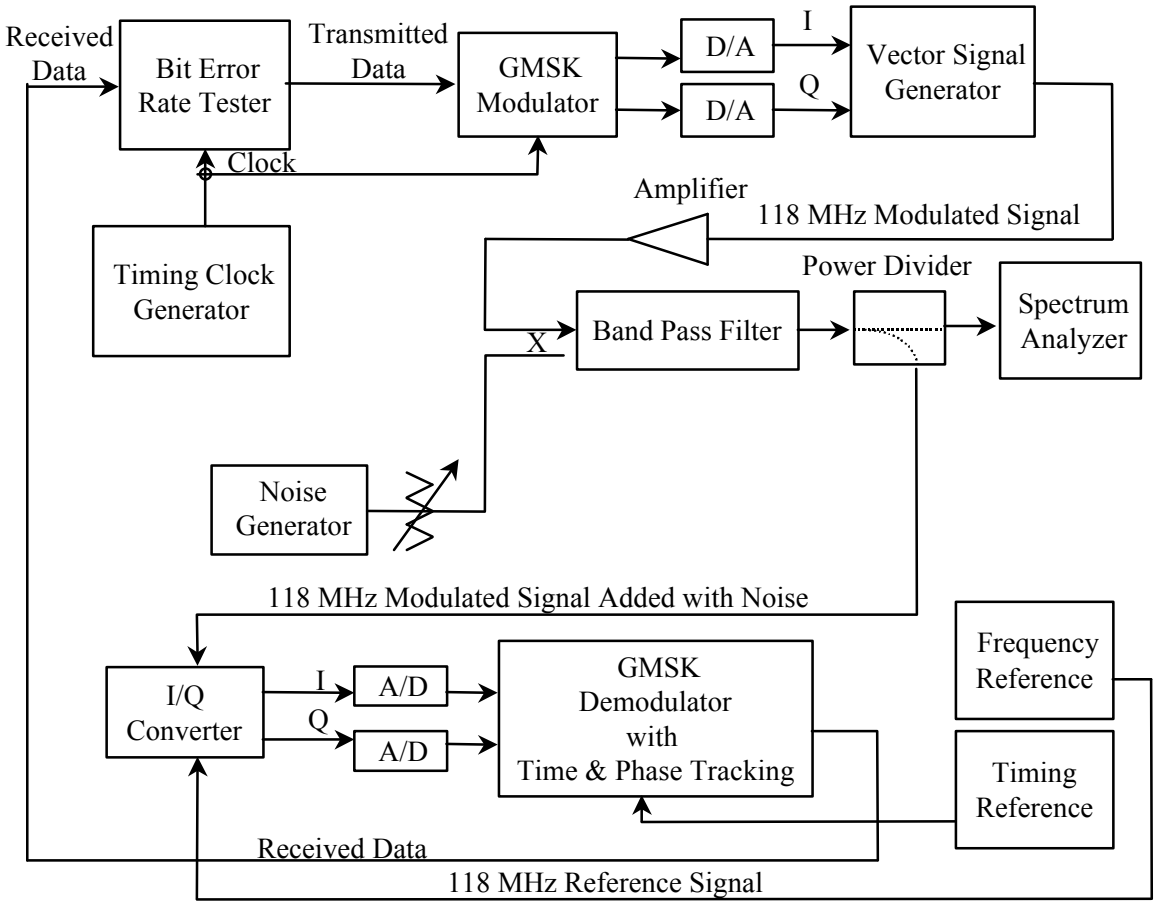

Figure 7, GMSK Modulator and Demodulator with Time and Phase Tracking

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