VIDEO SCAN RATE CONVERTER

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ABSTRACT

A simple technique to convert 675 and 875 line video to the more common 525 line rate is presented. The higher density 875 and 675 videos are stored and rescanned at the 525 line rate to produce a video signal that is essentially the same video signal that would have originally been generated by a 525 line video sensor (camera).

BACKGROUND

Military aircraft use special video display formats for cockpit video presentations. For example, on a particular aircraft, 675 and 875 line rates are used in addition to the more common 525 line rate. Also, there is a need to encrypt and transmit these videos to ground stations during tests, however, this capability exists only for the 525 line video. This paper presents a simple technique to convert 675 line and 875 line video into a 525 line format. This allows the 675 and 875 line video to be encrypted and transmitted to ground stations over the same data links that are used for the 525 line video.

The described circuit will operate in a scenario where it will be subjected to 525, 675 or 875 line video at 1 volt peak-to-peak across 75 ohms with an interlaced 60 field/30 frame format. The circuit must automatically detect the scan rate; if it is 525, the video is to be passed through without change; if it is 675 or 875, it must be converted to 525. (Note: the amplitude of aircraft video may be defined to be something other than 1 volt peak-to-peak across 75 ohms.)

The presented technique for converting 675 and 875 line video into 525 line video is to store the input picture at the input scan rate and then to rescan the stored picture at a 525 line rate to generate the output picture.
ANALYSIS

An input 525 line video will bypass the scan rate converter circuitry and is not considered in this analysis; the 525 line video referred to herein is the desired 525 line video generated from 675 or 875 line input video.

The interlaced 60 field/30 frame format, being common to all three videos, dictates that the output 525 line vertical scan time, top to bottom of picture, must be identical to the input vertical scan time of either the 675 or 875 line input. Consider the input line ratios as compared to 525.

\[
\frac{525}{675} = \frac{7}{9} \quad \text{and} \quad \frac{525}{875} = \frac{3}{5}.
\]

Therefore, to maintain the vertical scan rate, for each 9 lines of 675 line video input there must be 7 lines of 525 line video output; for each 5 lines of 875 line video input there must be 3 lines of 525 video output. Since the vertical scan time of each of the 3 videos is identical, only the horizontal scan rates can be a variable. The implication is that it should be feasible to build a scan converter circuit that uses the same vertical scan rate but different horizontal scan rates for storing and retrieving a picture.

If the input video signal is sampled with an Analog to Digital (A/D) converter and stored in a Random Access Memory (RAM), there must be an integer number of samples per line for both the input and output video to preclude any impact on the leading edge of the sync pulses. (Herein, each sample will be referred to as a pixel.) And, if there is to be an equal number of pixels per line stored for both input cases (675 and 875), then a common denominator must be considered. The common denominator for 7/9 and 3/5 is 45. Therefore, any multiple of 45 pixels per line can be used for converting both 675 and 875 line video into 525 while maintaining an integer number of pixels per line.

Refer to the simplified block diagram of Figure 1. The video will be digitized by the A/D converter, stored in RAM, retrieved from RAM and restructured into video by the Digital to Analog (D/A) converter. The design will use 2 RAMs swapping between the data in and data out modes while using an address scheme in which the scan line number is common to both memories, but, the pixel address within a line increments at different rates for pixel in versus pixel out. The line number for each memory will be identical whether the pixel data is being stored or retrieved to ensure identical vertical scan rates. However, the output pixel address will increment at \(\frac{7}{9}\) the input address rate for 675 line video, \(\frac{3}{5}\) for 875 line video, to satisfy the horizontal scan rate criteria.

As an example, assume a system with an 875 line raster and 5 pixels per line. Table I presents the relative counting sequences for the input and output pixel addresses for such a
system. There are 5 pixels stored for each input vertical line address, but, only 3 pixels are output during the same period. Further, the output pixel address cycles exactly 3 times while the input pixel address cycles 5 times.

**TABLE I. INPUT PIXEL ADDRESS VERSUS OUTPUT PIXEL ADDRESS CYCLES**

<table>
<thead>
<tr>
<th>VERTICAL LINE ADDRESS</th>
<th>INPUT PIXEL ADDRESS</th>
<th>OUTPUT PIXEL ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12345</td>
<td>123</td>
</tr>
<tr>
<td>2</td>
<td>12345</td>
<td>451</td>
</tr>
<tr>
<td>3</td>
<td>12345</td>
<td>234</td>
</tr>
<tr>
<td>4</td>
<td>12345</td>
<td>512</td>
</tr>
<tr>
<td>5</td>
<td>12345</td>
<td>345</td>
</tr>
<tr>
<td>6</td>
<td>12345</td>
<td>123</td>
</tr>
<tr>
<td>7</td>
<td>12345</td>
<td>451</td>
</tr>
<tr>
<td>8</td>
<td>12345</td>
<td>234</td>
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</tbody>
</table>

Figure 2a depicts 5 lines of the example system with respect to storing pixels in and retrieving them from memory. The slanted dash line represents the 875 line raster. Each block shows a pixel as it is stored in memory. The slanted solid line represents a 525 line raster and passes through those pixels that will be selected for restructuring the video. The shaded pixels are ignored and not used for generating the output video. Note the exact correlation with Table 1. The identical phenomena will occur in the actual system except there will be more pixels per line. A similar example can be shown for 675 line input video where 7 lines of output video will be generated from 9 lines of input video.

It is important to note that any particular output line does not contain the exact pixels that were generated by any one input line. This design will generate 7 output lines from 9 input lines of 675 line video and 3 from 5 or 875 line video. Therefore, approximately 22% of the 675 line pixels and 40% of the 875 line pixels are discarded. Further, as each frame of video is regenerated, the same pixels with respect to memory location are discarded.

In a normal video picture, any particular pixel is nearly identical to its adjacent pixels. The scheme described herein has the effect of stretching the pixels in the vertical direction to fill in for the missing pixels. The effect is a decrease in the vertical resolution with no
impact in the horizontal resolution as shown in Figure 2b. The same result would be obtained if the picture were to be originally generated with a 525 line sensor.

CIRCUIT SYNTHESIS

In the presented circuit, the incoming sync signals will be digitized and reconstructed in the D/A converter along with the video portion of the signal. There will be 8 bits of data per pixel or 256 levels available. The sync will use approximately 75 levels leaving roughly 175 levels for gray scale resolution. And, since it takes longer to clock out the data than to clock in the data, the sync pulses will be stretched by a factor equal to the clock-in/clock-out ratios. As a future enhancement, it should be possible to strip the sync prior to the A/D conversion and dedicate all 256 levels to gray scale resolution and then to restore the sync pulses after the D/A conversion.

The input and output clock pulses used by the circuit will be generated via HC4046A phase lock loops (PLL). It is desirable to have more than 500 pixels per line for this circuit, therefore, the maximum frequency of the HC4046A (18MHz) must be considered. Experience has shown satisfactory results while operating these devices in the 16 to 17 MHZ range. The highest PLL frequency will be encountered while entering the 875 line input data. (In the following calculations, 30 is the number of fields per second.)

\[
\frac{16 \times 10^6}{(875 \times 30)} = 609.5 \text{ (approximate pixels per line) use - 610.}
\]

\[
\frac{610}{45} = 13.6 \text{ (approximate multiplication factor) - use 14.}
\]

\[
45 \times 14 = 630 \text{ pixels per line.}
\]

\[
630 \times 30 \times 875 = 16,537,500 \text{ Hz.}
\]

This satisfies the maximum frequency criteria for the HC4046A.

The correlating output frequency will be

\[
16,537,500 \times \frac{3}{5} = 9,922,500 \text{ Hz.}
\]

For 675 line video the input clock rate will be

\[
630 \times 30 \times 675 = 12,757,500 \text{ Hz.}
\]
and the output clock will be

\[ 12,757,500 \times \frac{7}{9} = 9,922,500 \text{ Hz.} \]

As a check

\[ 630 \times 30 \times 525 = 9,922,500 \text{ Hz.} \]

Remember that for 675 line video there are exactly 7 lines output at the same time there are exactly 9 lines input (3 and 5 for 875). Therefore, the RAMs need only be deep enough to store 9 lines worth of data. The addressing line counter will reset after 9 lines of 675 data (5 for 875), and with each counter reset, the data store/retrieve functions of the memories will be swapped. This scheme will cause a total input to output time delay equivalent to 9 lines for 675 input video and 5 lines for 875 input video.

The amplitude (amplifier gain) and the passing of 525 line input video directly to the output (analog multiplexer) are insignificant from an analysis/design standpoint and are not considered herein.

**CIRCUIT BLOCK DIAGRAM**

The Block Diagram for the Scan Converter can be broken into 2 sections. Figure 3a shows the Timing, Addressing and Control functions and is an expansion of the Timing and Address block of Figure 1. Figure 3b shows the Video Processing and is an expansion of the remainder of Figure 1.

Refer to Figure 3a. These circuits process the input video to generate pixel input and pixel output clocks, the control signals for memory 1 and memory 2, line addresses, pixel input and pixel output addresses, and the signal to control the output mux.

The processing is started by stripping the composite and vertical sync signals form the input video. The scan rate is then determined by counting the number of composite sync pulses between the vertical sync pulses. If 525 line video is detected, the Scan Rate Detector selects the input video to be output by the Analog Mux and the scan rate conversion is bypassed. If 675 or 875 line video is detected, the input video will be processed by the Scan Rate Converter to generate 525 line video.

The Line Address Generator cycles through address 0 to 8 (9 lines) for 675 line video and from 0 to 4 (5 lines) for 875 video. The control lines, Cont 1 and Cont 2, are slaved to the line addresses and are used to control the Read/Write functions of the two memories. The
675/875 signal tells the Horizontal PLL and the Pixel Out PLL the input line rate. The Line Reset signal is used to synchronize the Pixel Out Address Generator to the Line Address Generator.

In the initial design case for this circuit, the 675 line video contained no equalizing pulses, whereas the 875 line video did. The Equalizing Pulse Stripper removed the equalizing pulses form the 875 line composite sync and the Horizontal PLL inserted the missing horizontal pulses into the 675 line composite sync. The Pixel In PLL multiplies the horizontal sync rate by a factor of 630 regardless of the input line rate to provide the Pixel In Clock. The Pixel In Addresses are taken directly from the counters in the Pixel In PLL. The Pixel Out Address Generator is a set of counters designed to follow the same counting pattern as the pixel input counters, however, they are clocked at the rate required to generate 525 line video. The multiplication factor of the Pixel Out PLL is dependent on the input scan rate. It multiplies the horizontal sync by a factor of

\[ 630 \times \frac{7}{9} = 490 \] for 675 line video,

\[ 630 \times \frac{3}{5} = 378 \] for 875 line video,

thereby, satisfying the output clock frequencies determined in the Analysis section.

Figure 3b shows the video processing section of the block diagram. If the input is 525 line video, it is passed directly to the Analog Mux without processing. If the input is either 675 or 875 line video, it is amplified to 3.5 volts peak-to-peak and is clocked through the A/D Converter by the Pixel In Clock. Cont 1 and Cont 2 control the two memories and their input and output buffers to alternately write to memory 1 while reading from memory 2 and vice versa on a continual basis. The buffers are required for tri-stating purposes.

The buffers and memories are controlled such that exactly 9 lines of input video are stored for 675 line video (5 for 875) before their Read/Write functions are swapped. While one memory is storing 9 lines of 675 line video (5 of 875) the other is retrieving 7 lines (3 lines) of 525 line video. The Line Address to the two memories are always identical, whereas the Pixel In Address and Pixel Out Address are controlled by Cont 1 and Cont 2 via Address Mux 1 and 2, respectively. The data from the Output Buffers is then fed to the D/A Converter to generate an analog signal which is 525 line video with an amplitude to 1 volt peak-to-peak. The Analog Mux selects the appropriate input signal, input 525 line video or restructured 525 line video, which is then amplified by a factor of 2 to become the output video.
RESULTS

The described circuit was designed, built and tested with excellent results. The quality of the restructured output video when dealing with “camera type” video was equivalent to that produced with a 525 line camera. There was minimal degradation when scan converting faces, landscapes, buildings, machinery, etc. But, when dealing with computer generated symbolic video such as crosshairs and lettering, the discarded video could have a significant impact on the symbol. Portions of video lines are missing and if the symbol had a horizontal line component, e.g., the letter T, the symbol could be difficult to interpret.

The Scan Converter operates from aircraft 28 Volts DC and is packaged into a box approximately 1.5" x 5" x 6". The Scan Rate converter is now an integral part of a flight instrumentation set.
FIGURE 2. SCAN CONVERTER MEMORY CONCEPT
FIGURE 3. SCAN RATE CONVERTER BLOCK DIAGRAM